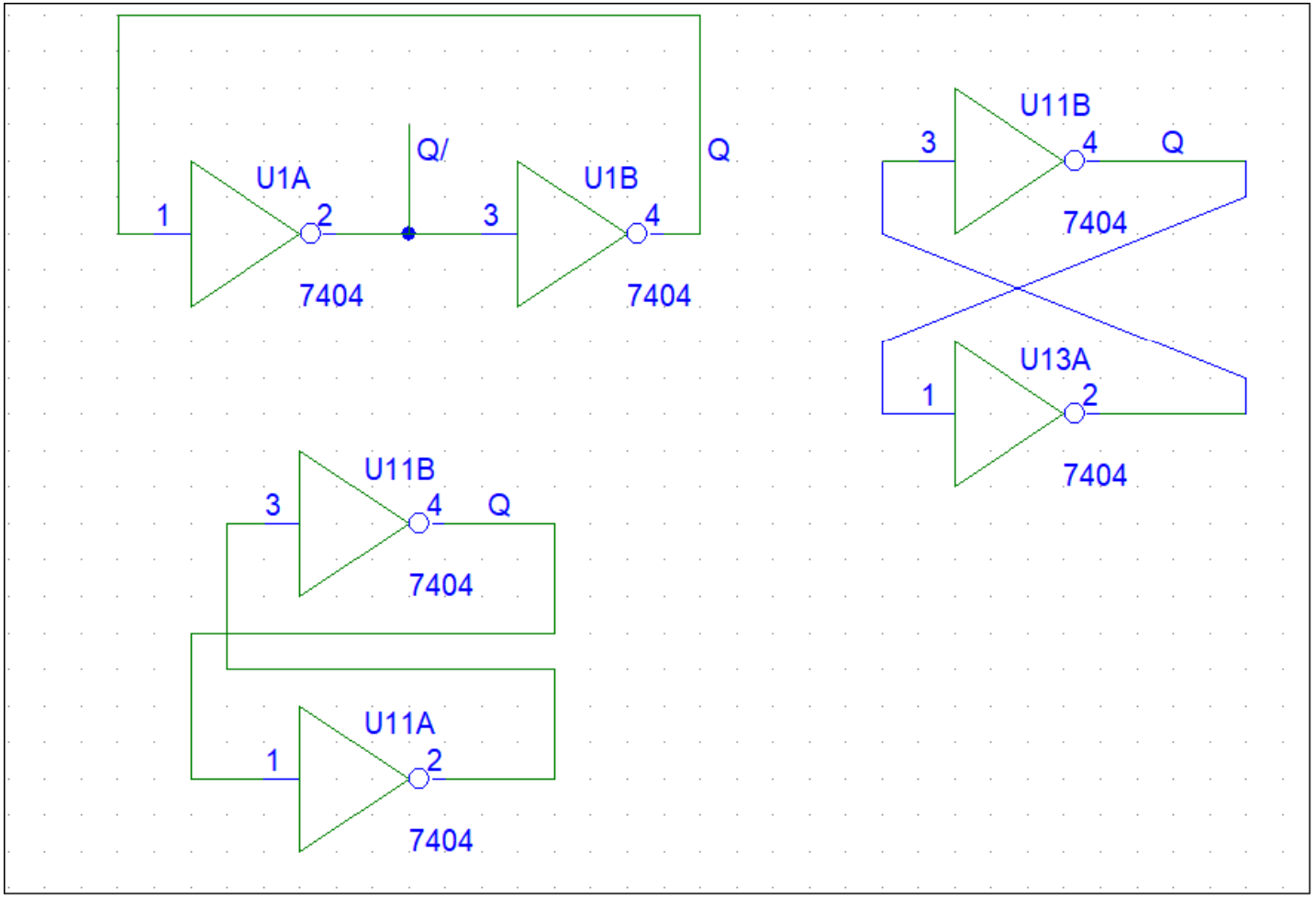
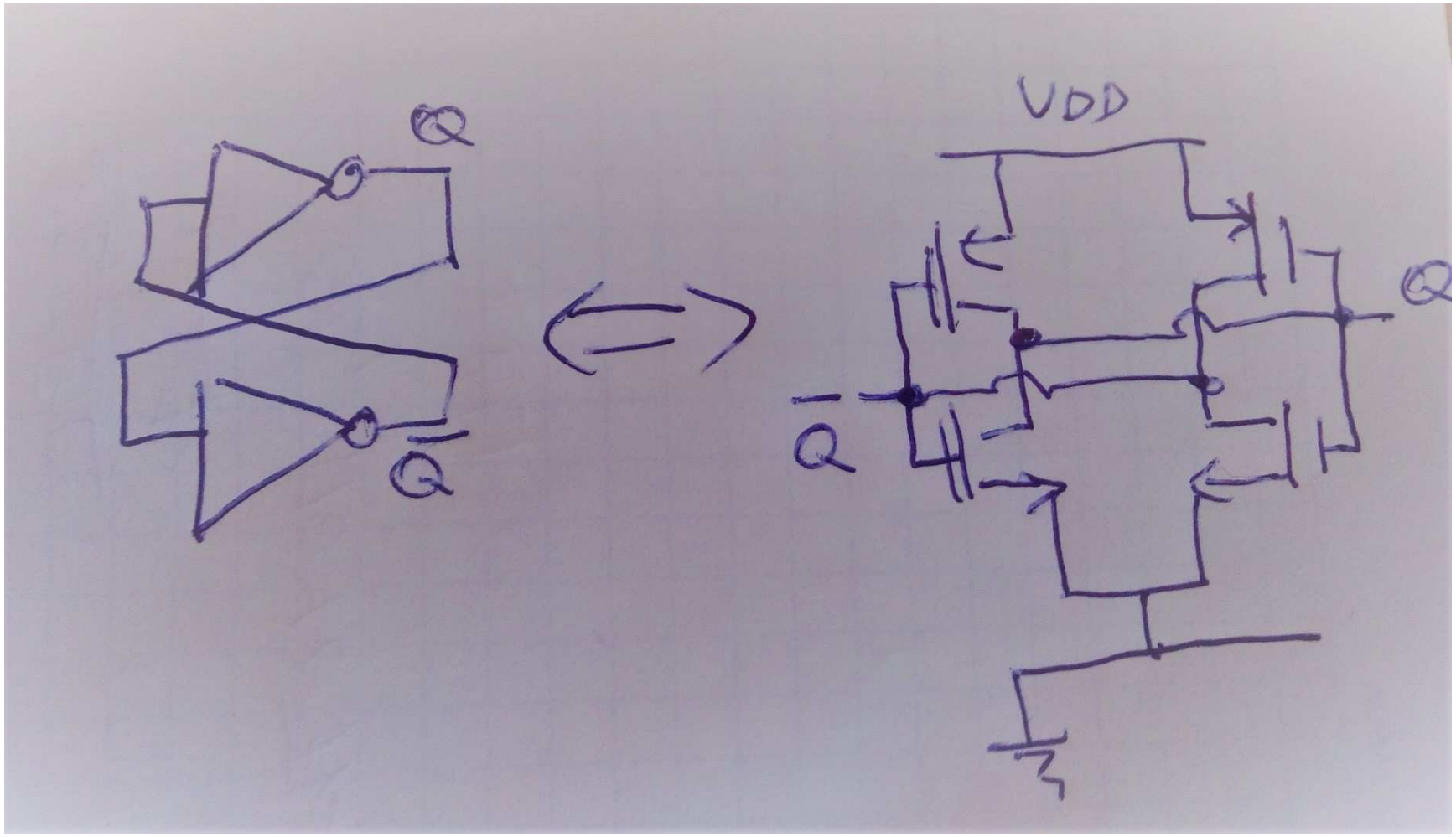
Bistabilna kola
Leč kolo
Flip-Flop

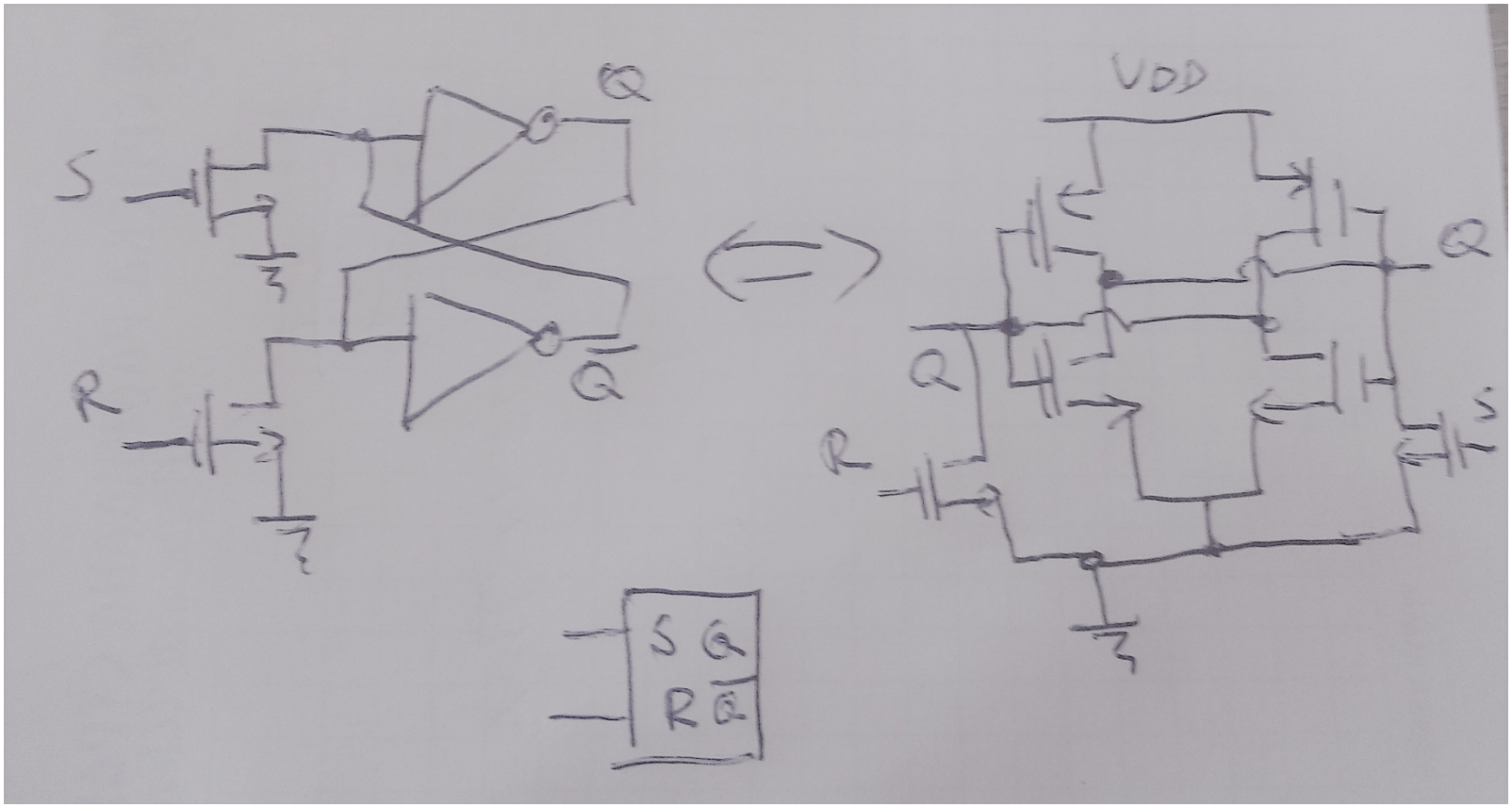
Standard sequential circuits – SR latch



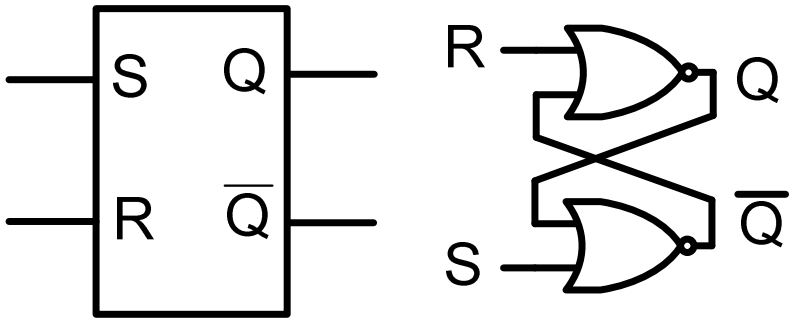
Standard sequential circuits – SR latch



Standard sequential circuits – SR latch

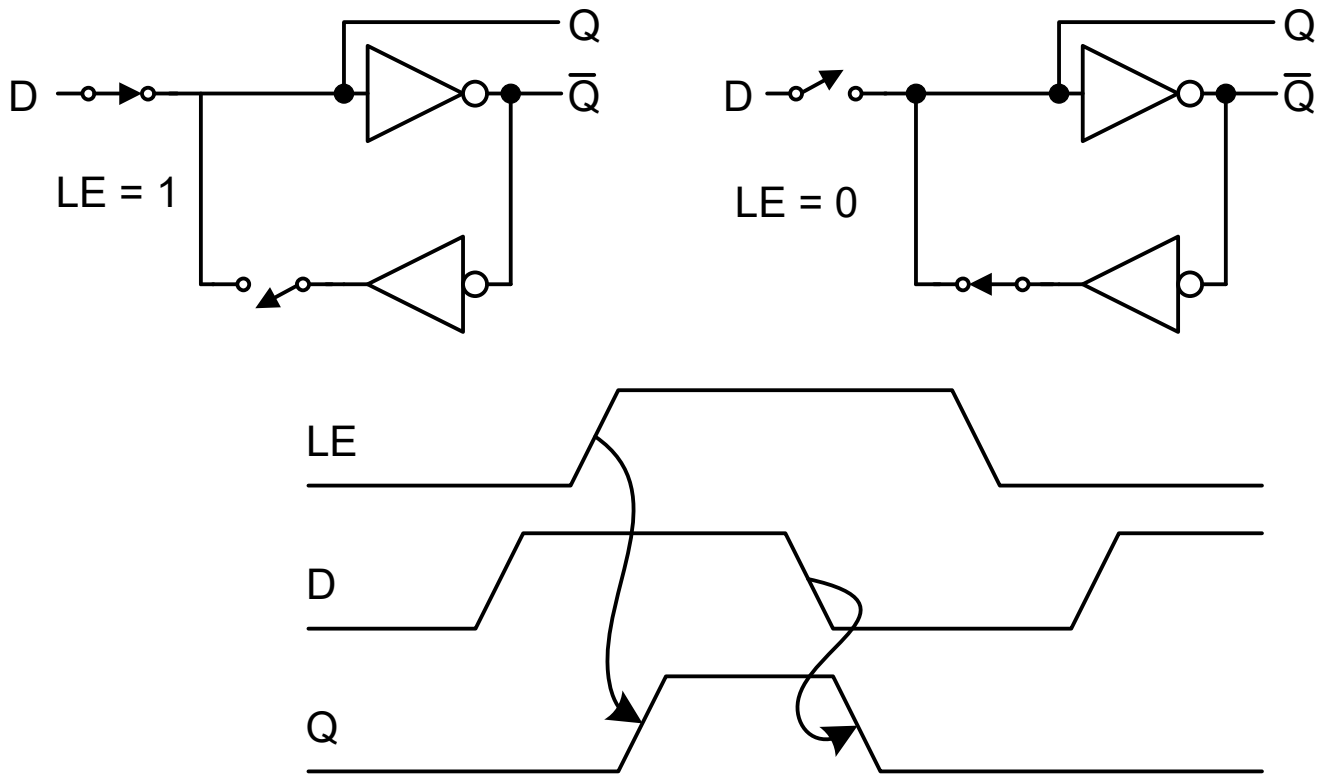


Standard sequential circuits – SR latch

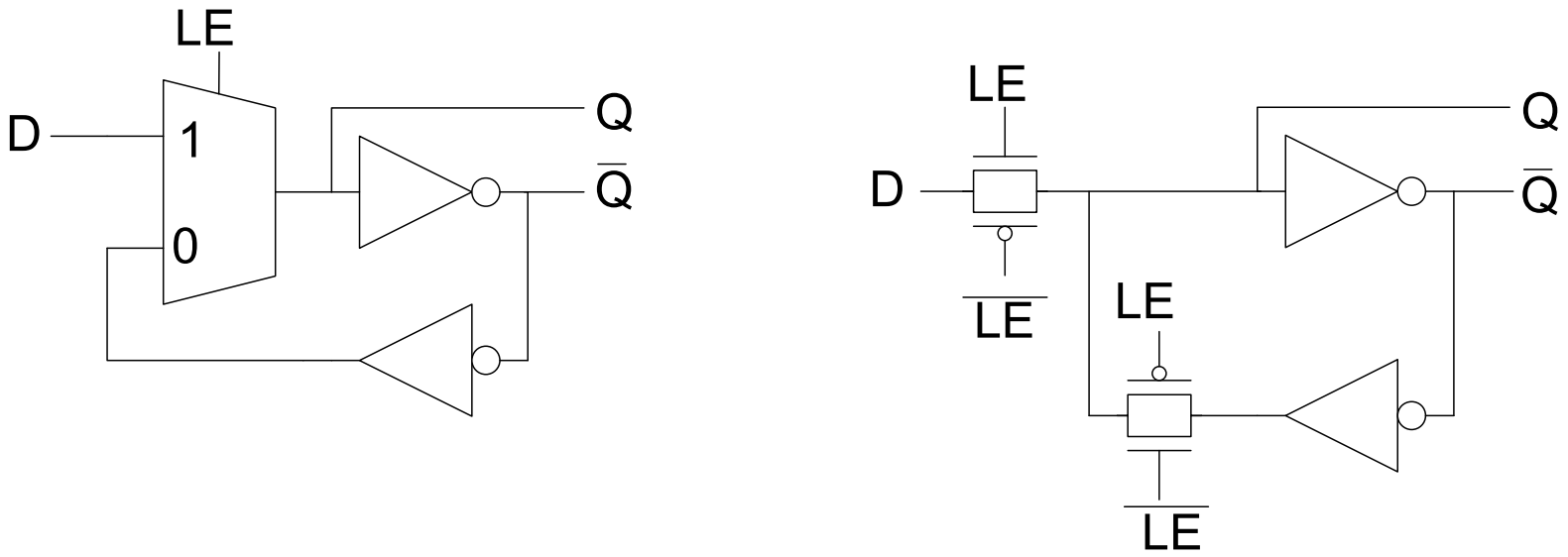


R	S	Q[n+1]
0	0	Q[n]
0	1	1
1	0	0
1	1	?

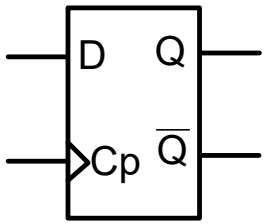
Standard sequential circuits – D latch

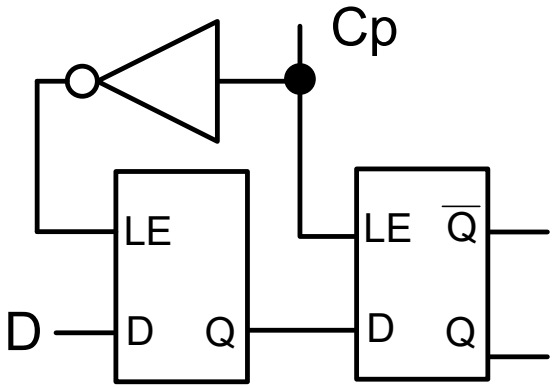


Standard sequential circuits – D latch



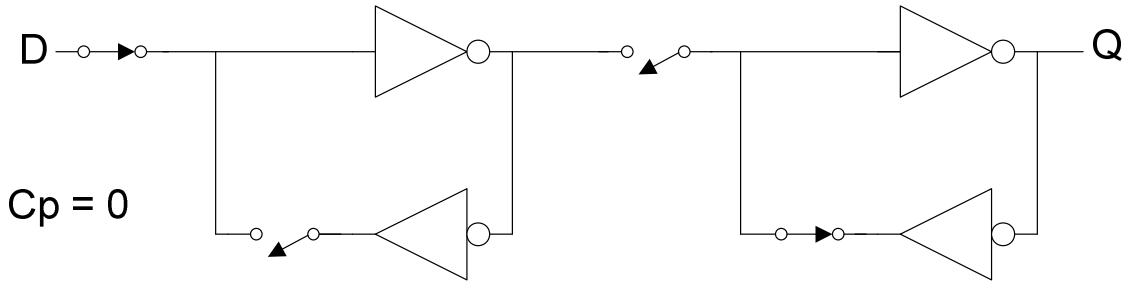
Standard sequential circuits – D FF

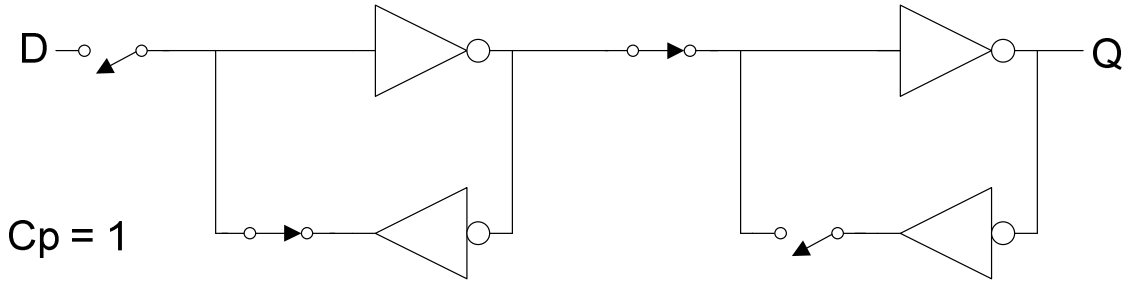


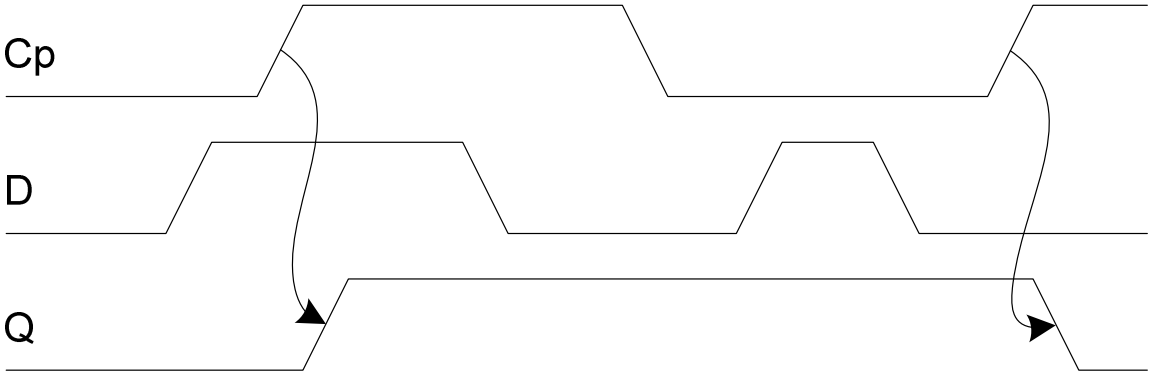


D	Cp	Q[n+1]
x	0	Q[n]
0	0→1	0
1	0→1	1
x	1	Q[n]

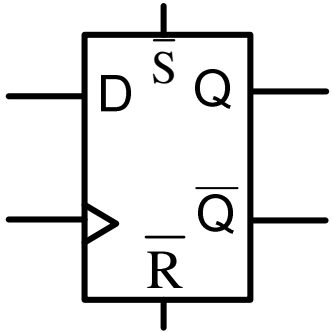
D FF master-slave operation

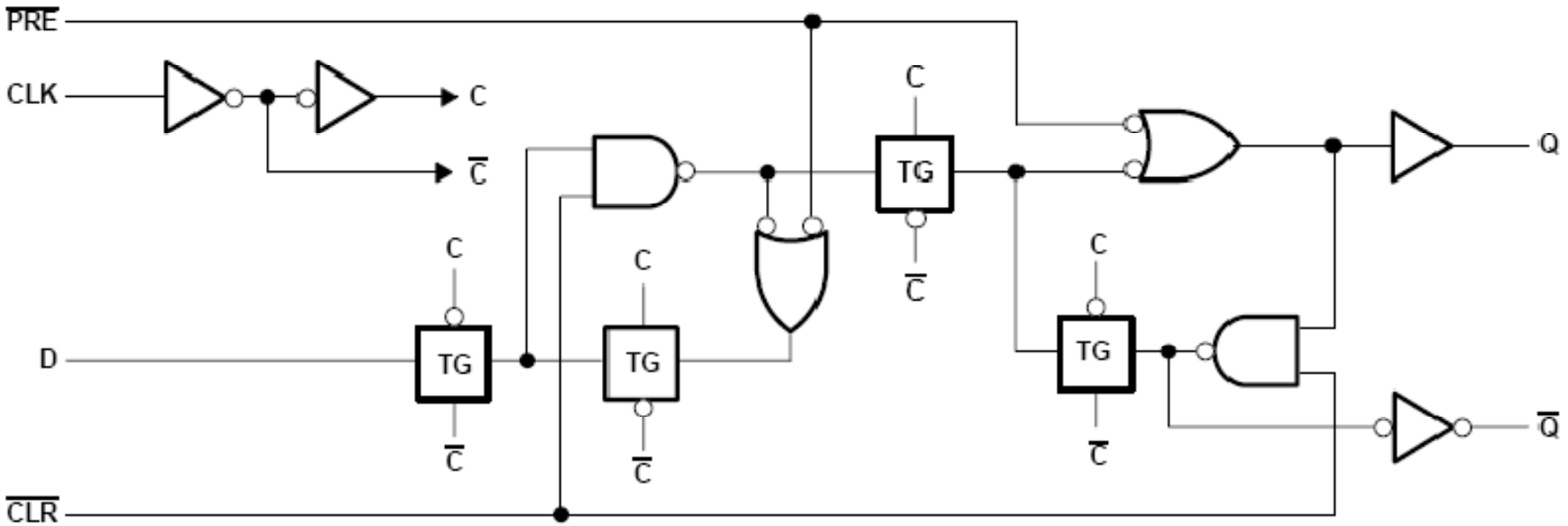




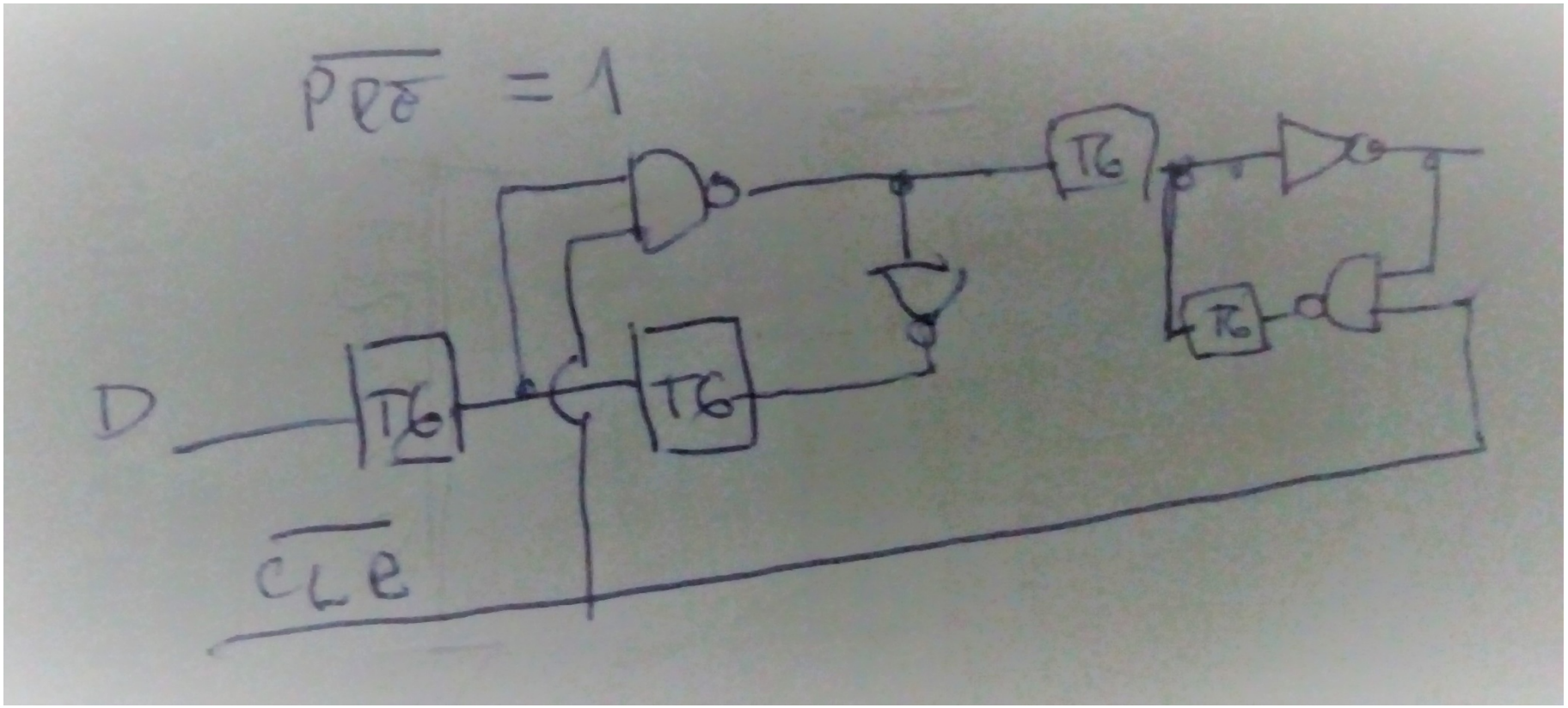


D FF with /preset and /clear



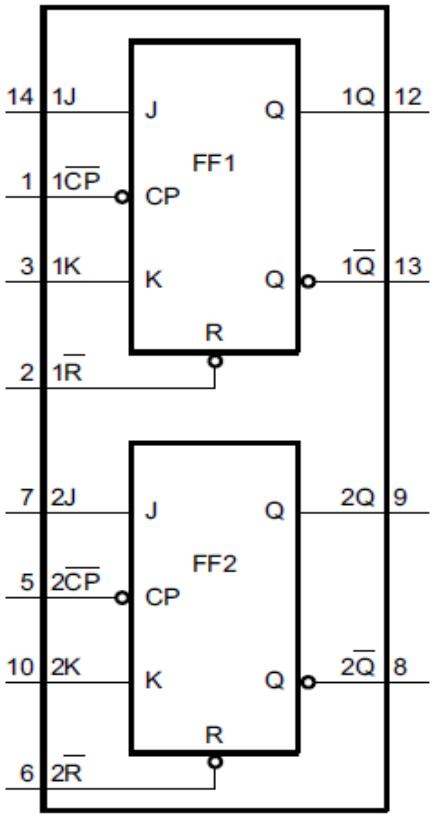


D FF with /preset=1 and /clear



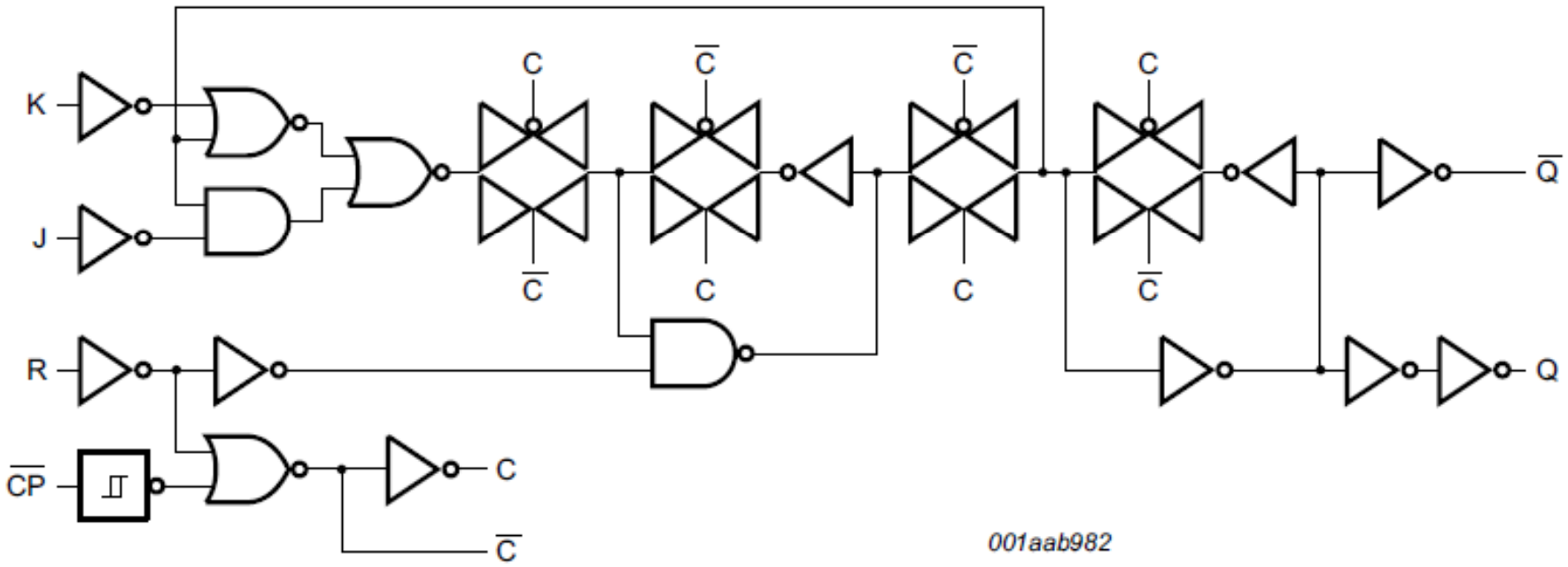
74HC73

JK flip-flop with reset; negative-edge trigger

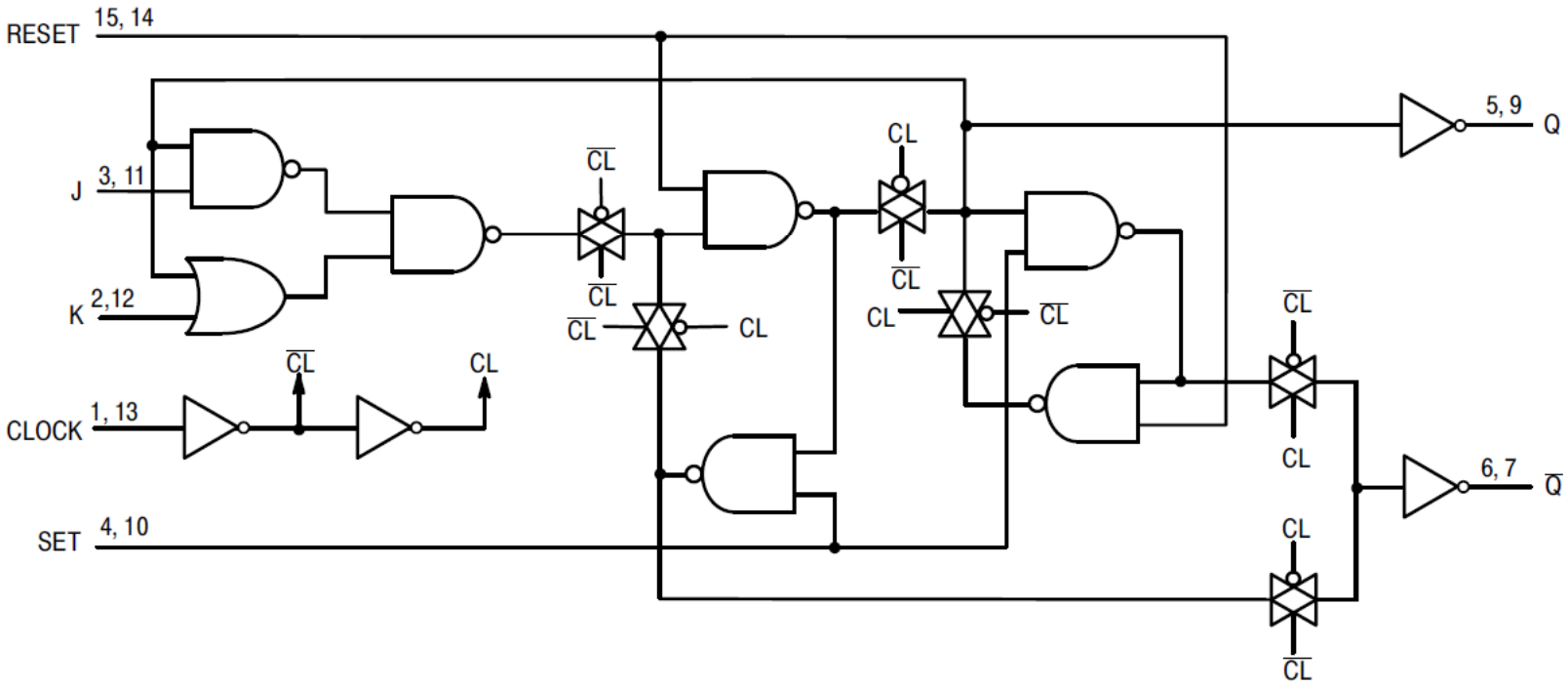


74HC73

JK flip-flop with reset; negative-edge trigger

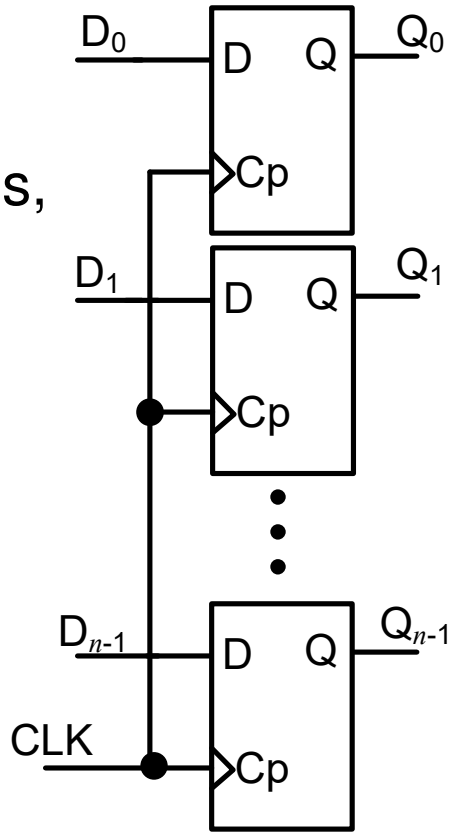


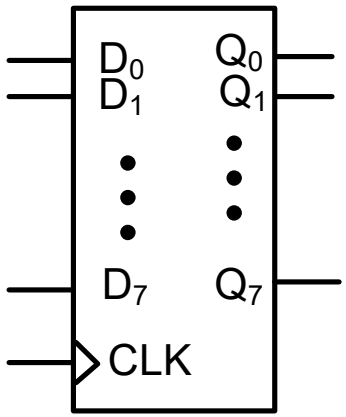
Dual J-K Flip-Flop with Set and Reset



Registers

- n-bit register is a set of n D flip-flops, one per bit
- Data inputs are D_0, D_1,…,D_{n-1}
- Data outputs are Q_0, Q_1,…,Q_{n-1}
- Common Clock for all flip-flops
- Optional preset or clear

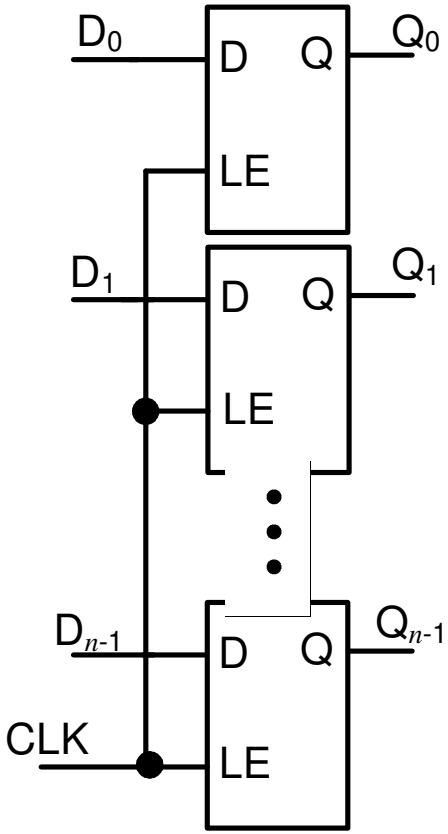


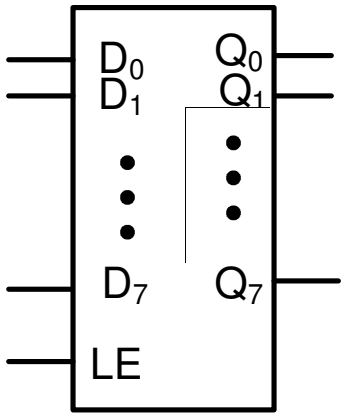


8-bit register

n bit latch

- n-bit latch is a set of n single bit latches, one per bit
- Data inputs are D_0, D_1,…,D_{n-1}
- Data outputs are Q_0, Q_1,…,Q_{n-1}
- Common LE for all latches
- Optional preset or clear





8-bit latch

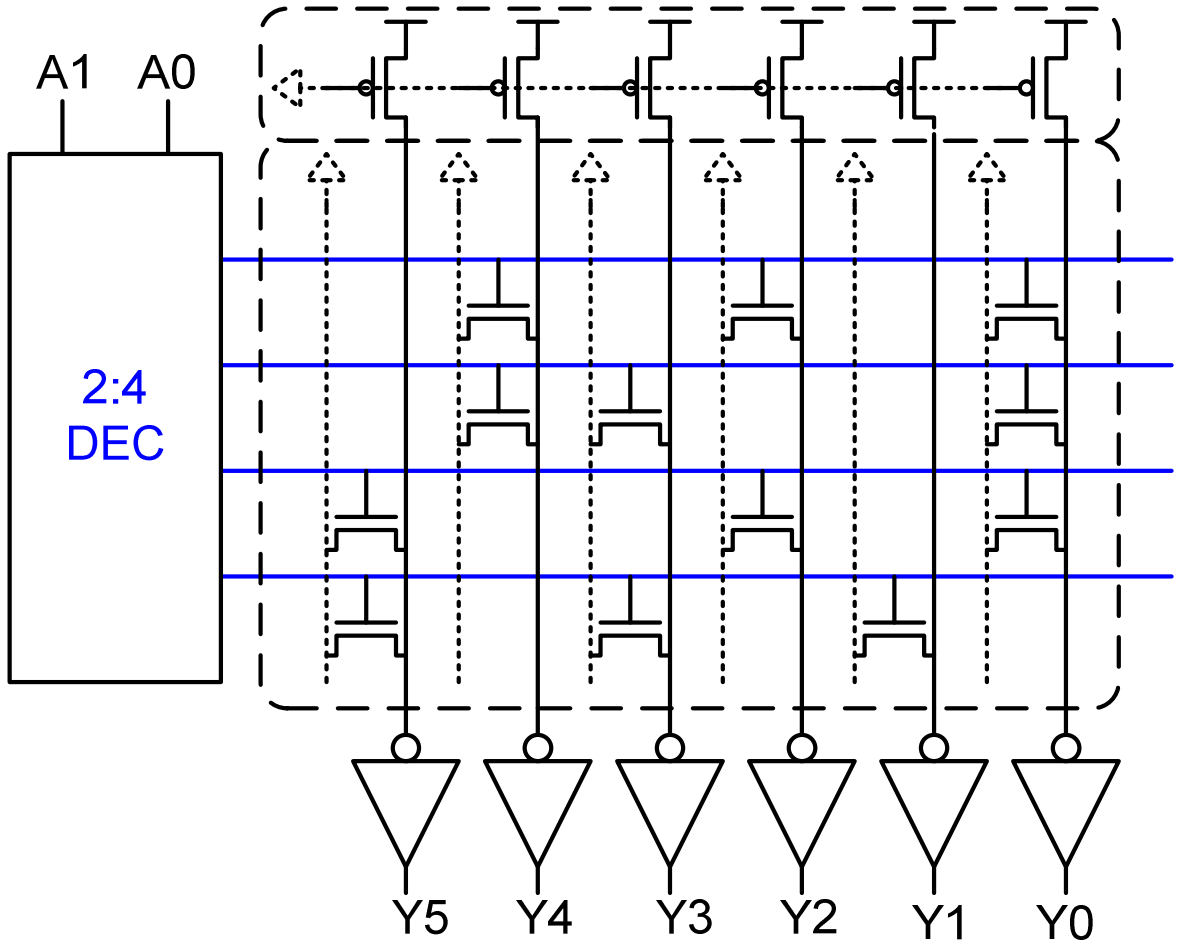
ROM 4×6bit

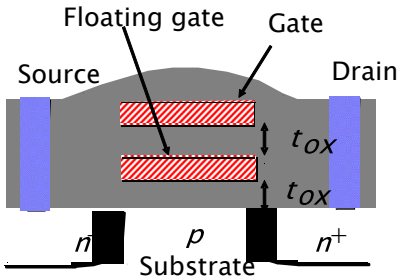
Word 0: **010101**

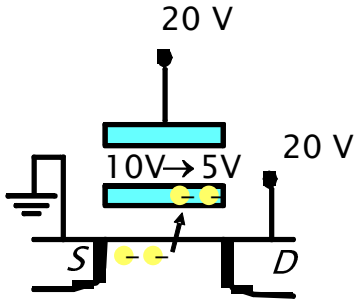
Word 1: **011001**

Word 2: **100101**

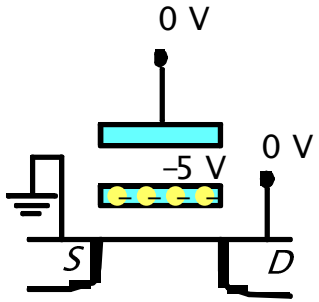
Word 3: **101010**



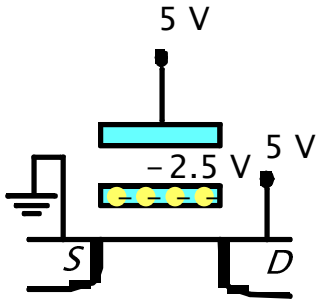




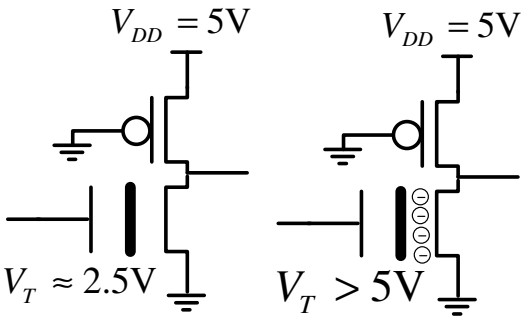
Avalanche injection.



Removing programming voltage leaves charges trapped

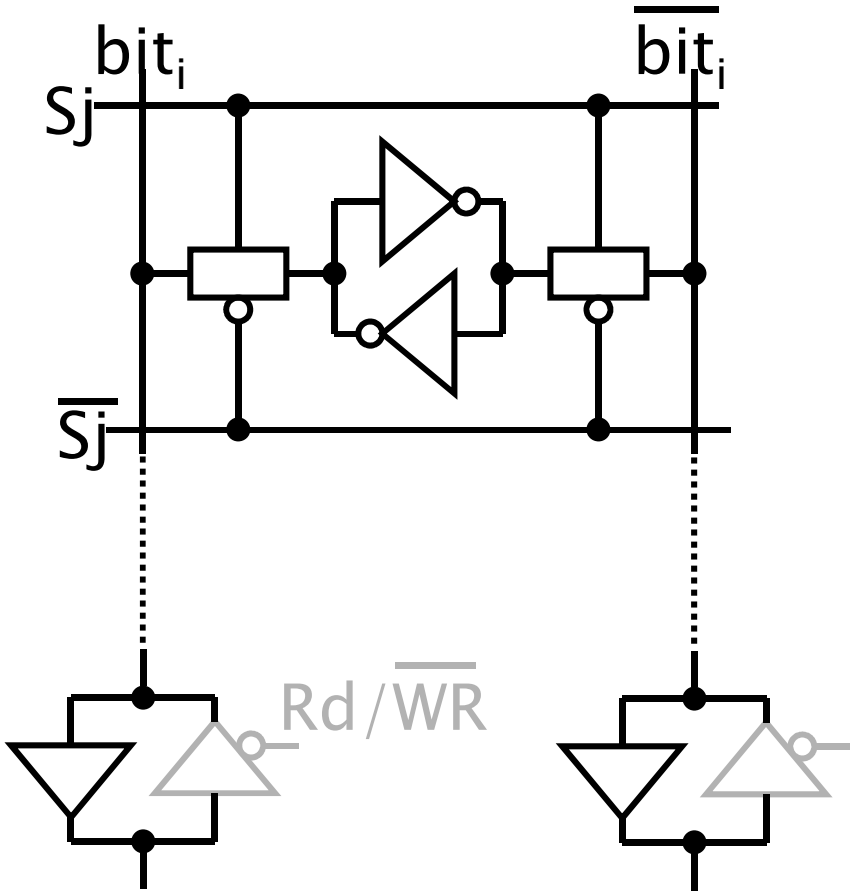


Programming results in higher V_T



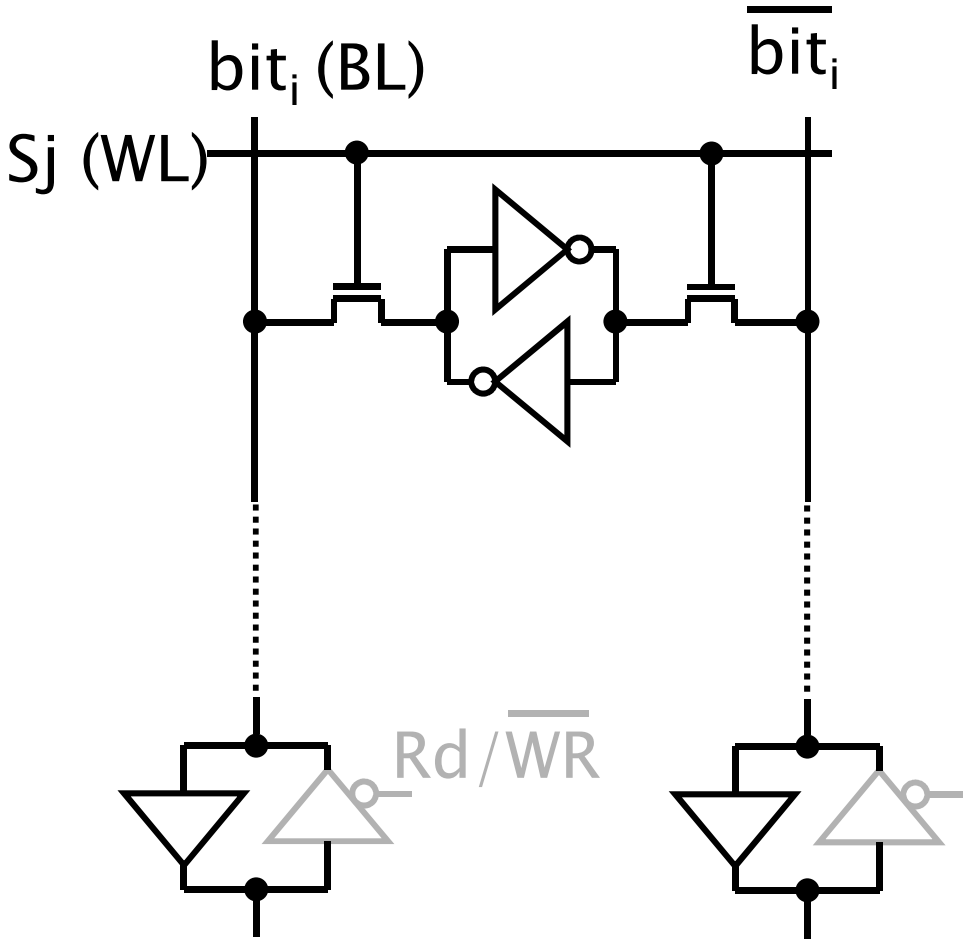
Memory Cell: Static RAM (8 transistors)

- 8-transistor cell
  - Bit_i is the data bus
  - Sj is the word line
- Bus drivers
  - Sense Amplifier (inverter with high gain) used for fast switching
  - Make sure inverters in cell are weaker than the combination of "write buffer" and pass transistor



Memory Cell: Static RAM (6 transistors)

- 6-transistor cell
  - Must adjust inverters for input coming through n-type pass gate
- Bus drivers
  - Must adjust senseAmp for input coming through n-type pass gate
  - Harder to drive 1 than 0 through write buffer (high resistance via n-transistor)
  - One side is sending 0 anyway (bit or bit') ➔ written correctly

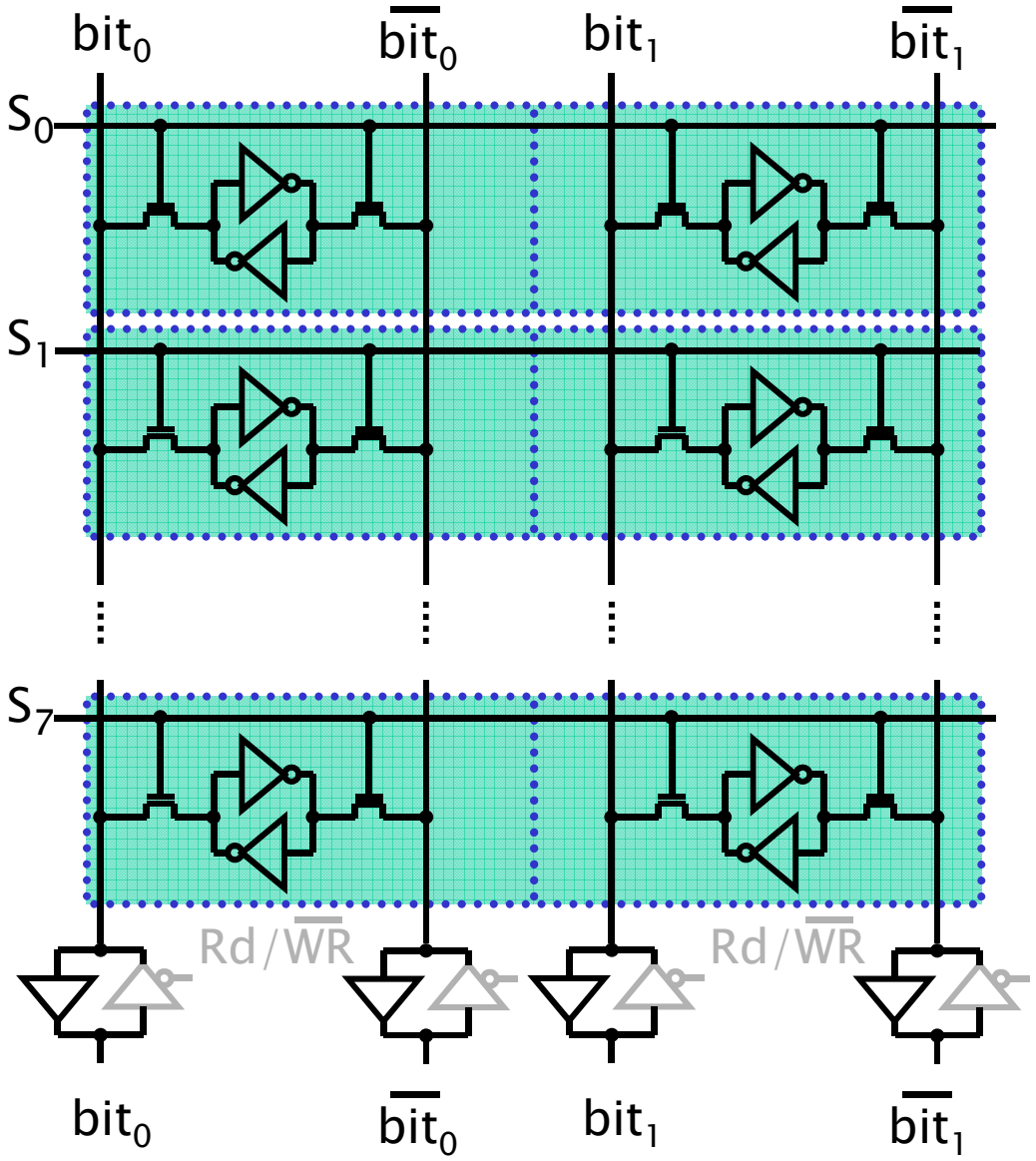


6-Transistor Memory Array

- 8 words deep RAM,
  2 bits wide words

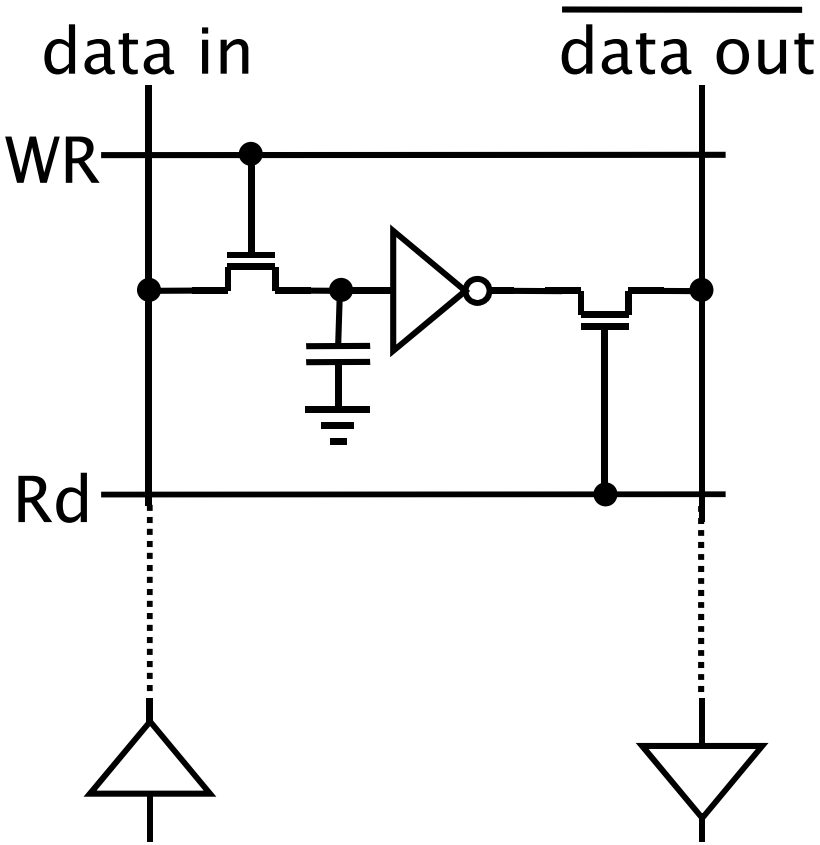
- To write to word j:
  - Set S_j=1, all other S lines to 0
  - Send data on the global bit_0, bit_0', bit_1, bit_1'

- To read word k:
  - Set S_k=1, all other S lines to 0
  - Sense data on bit_0 and bit_1.



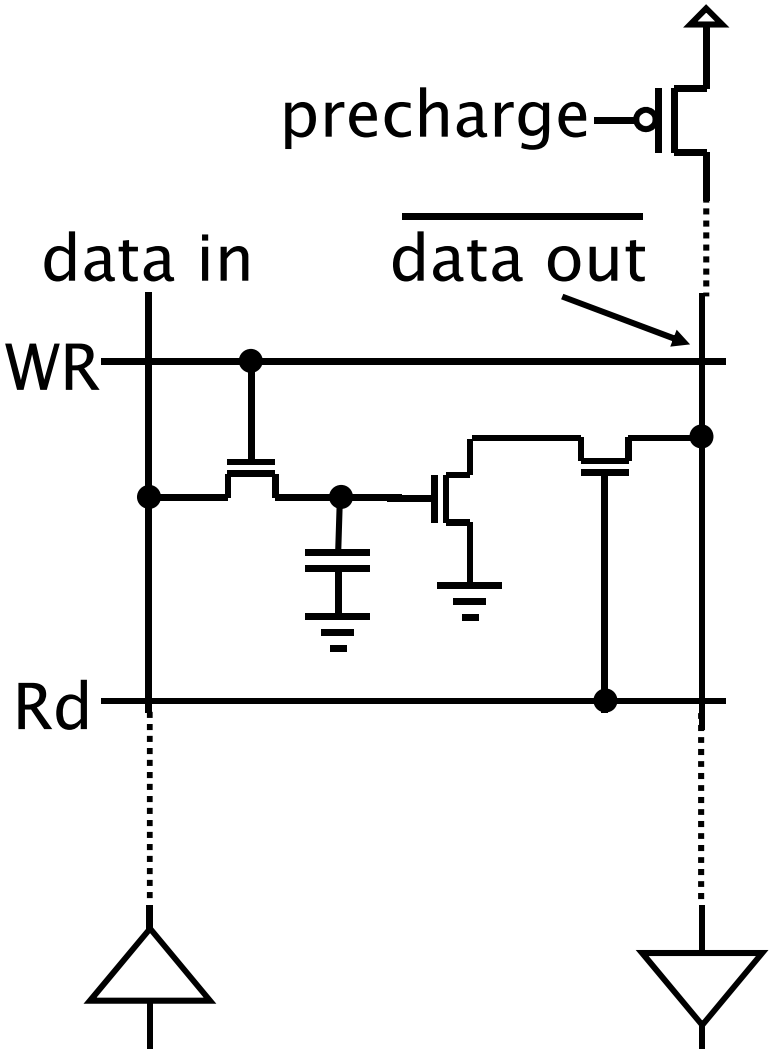
Dynamic RAM 4-Transistor Cell

- 4-transistor cell
- Dynamic charge storage must be refreshed
- Dedicated busses for reading and writing



Dynamic RAM 3-Transistor Cell

- 3-transistor cell
  - No p-type transistors yield a very compact layout for cell
  - No Vdd connection
  - Sense Amplifier must be able to quickly detect dropping voltage



Dynamic RAM 1-Transistor Cell

- 1-transistor cell
  - Storage capacitor is source of cell transistor
  - Special processing steps to make the storage capacitor large
  - Charge sharing with bus capacitance ($C_{cell} << C_{bus}$)
  - Extra demand on sense amplifier to detect small changes
  - Destructive read (must write immediately)