Federal University of Santa Catarina
Center for Technology
Computer Science & Electronics Engineering

Integrated Circuits & Systems

INE 5442

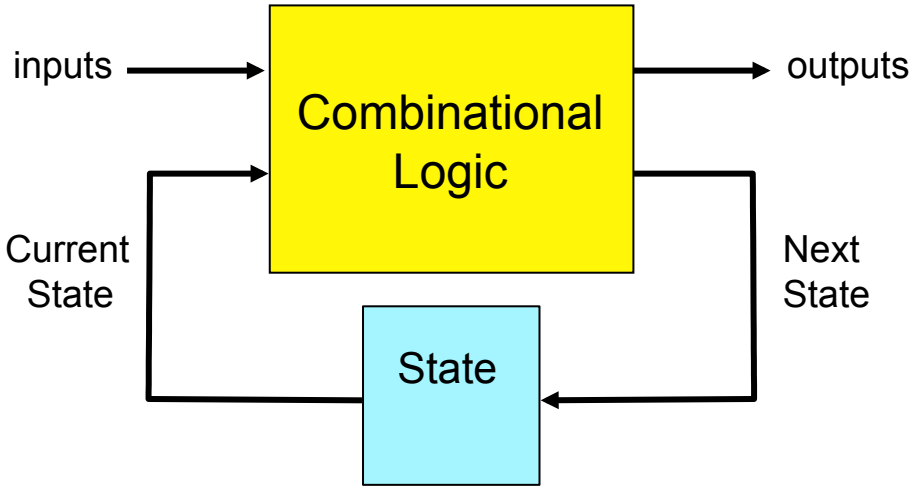
Lecture 18

CMOS Sequential Circuits - 1

Prof. José Luís Güntzel
guntzel@inf.ufsc.br

CMOS Sequential Circuits

Sequential Logic



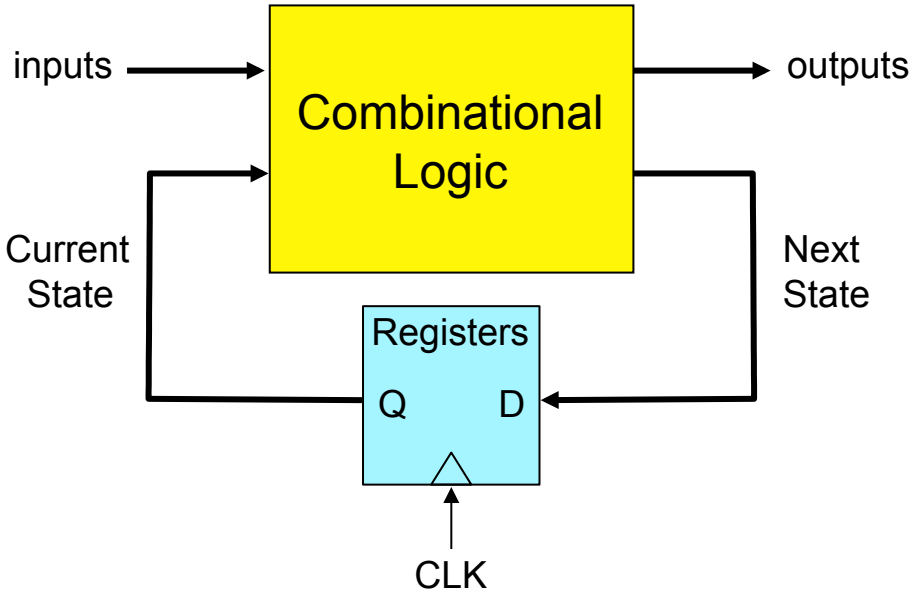
2 Storage Mechanisms:

- Positive feedback
- ~~Charge-Based~~

Source: Rabaey; Chandrakasan; Nikolic, 2003

CMOS Sequential Circuits

Sequential Logic



Positive Feedback: uses latches or registers

Naming Conventions

- **In Rabaey's IC book:**
  - A latch is level sensitive
  - A register is edge-triggered
- **Many other books:**
  - Flip-flop is an edge-triggered

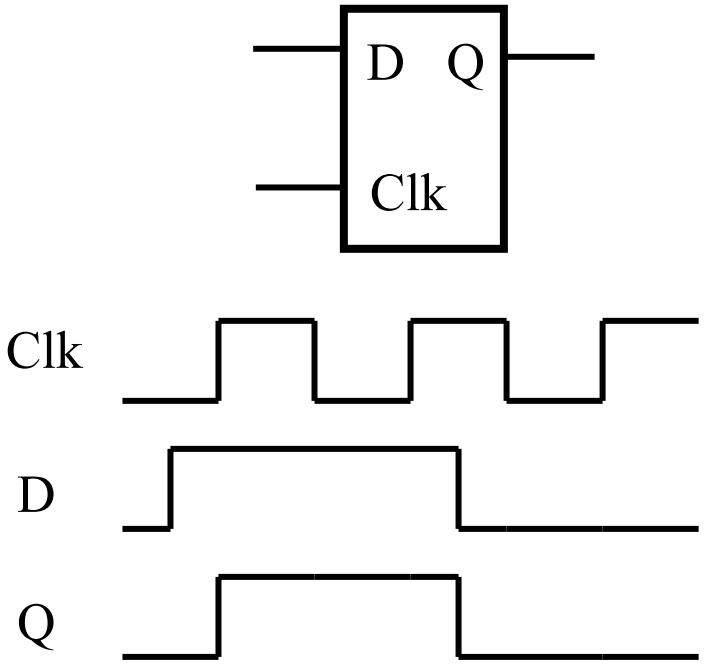
Source: Rabaey; Chandrakasan; Nikolic, 2003

CMOS Sequential Circuits

Latch Versus Register

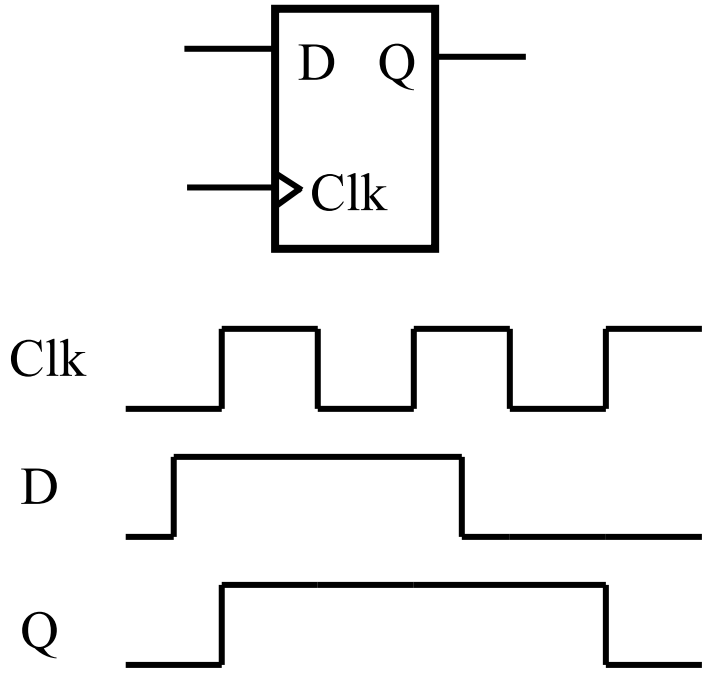
- **Latch**

  stores data when clock is low



- **Register**

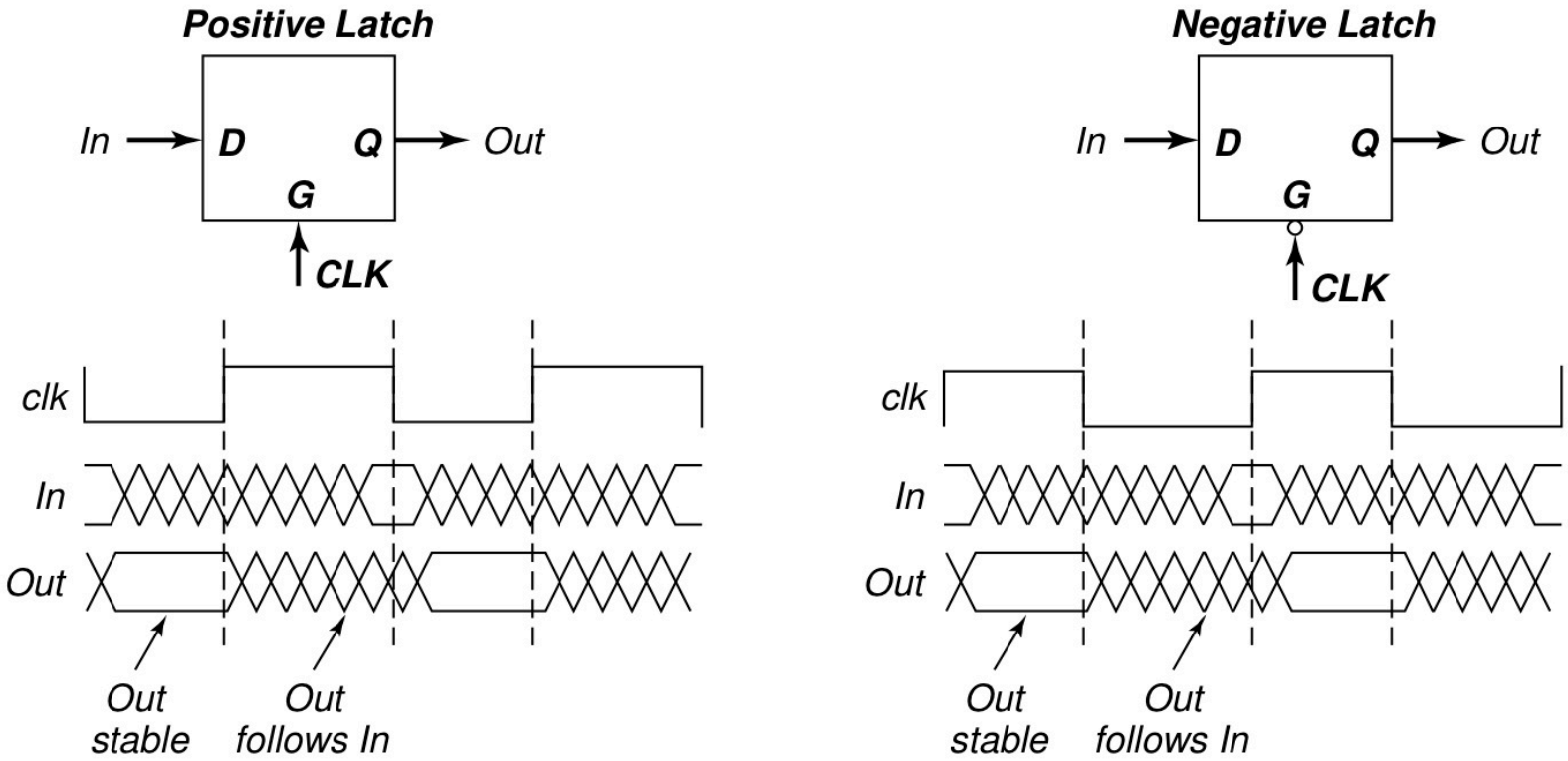
  stores data when clock rises



Source: Rabaey; Chandrakasan; Nikolic, 2003

CMOS Sequential Circuits

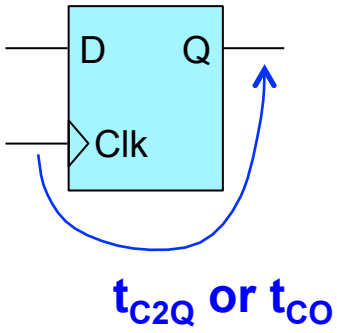
Latches



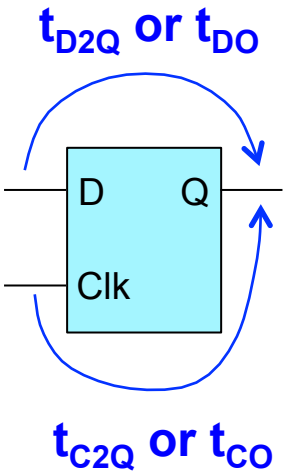
Source: Rabaey; Chandrakasan; Nikolic, 2003

Characterizing Timing

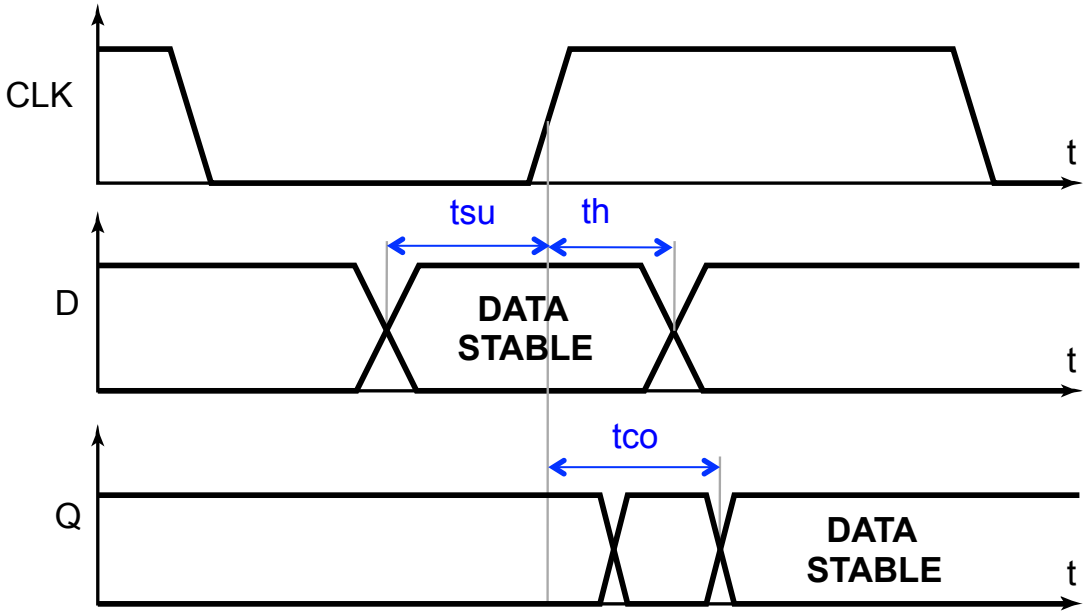
Register

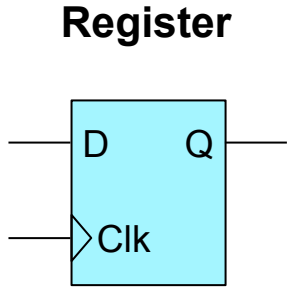


Latch



Timing Definitions





tsu = setup time

th = hold time

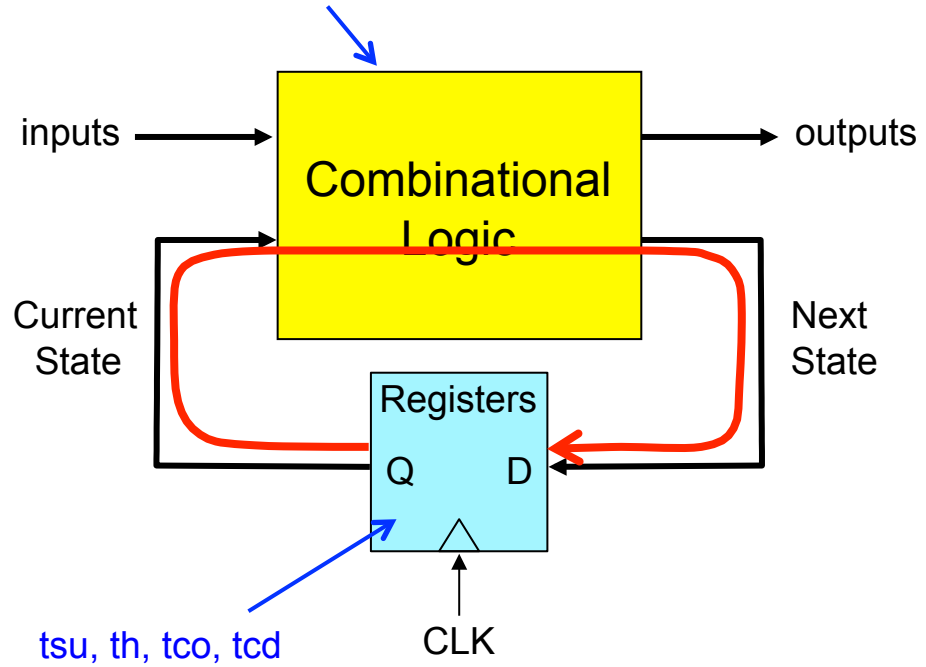
tco = tc2q = maximum propagation delay (or time from clock to output Q)

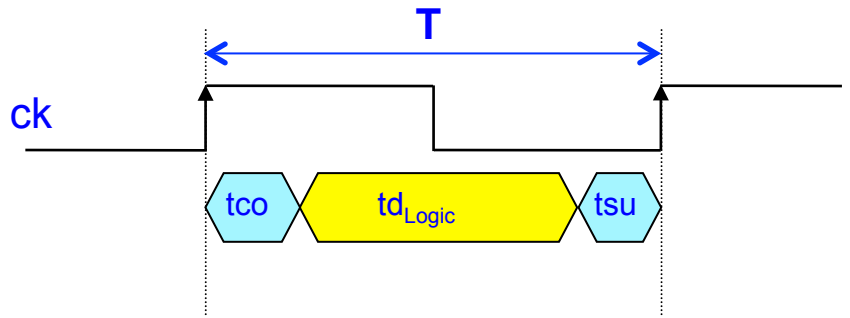
tcd = minimum propagation delay (or *contamination delay*)

Source: Rabaey; Chandrakasan; Nikolic, 2003

Maximum Clock Frequency

td_{Logic} = maximum propagation delay
tc_{Logic} = minimum propagation delay
(or *contamination delay*)



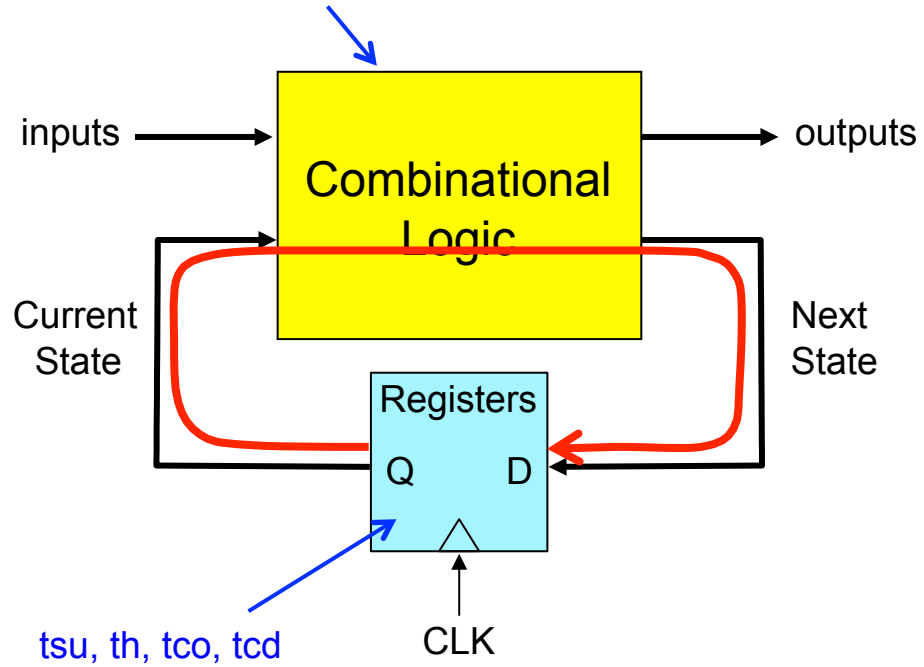


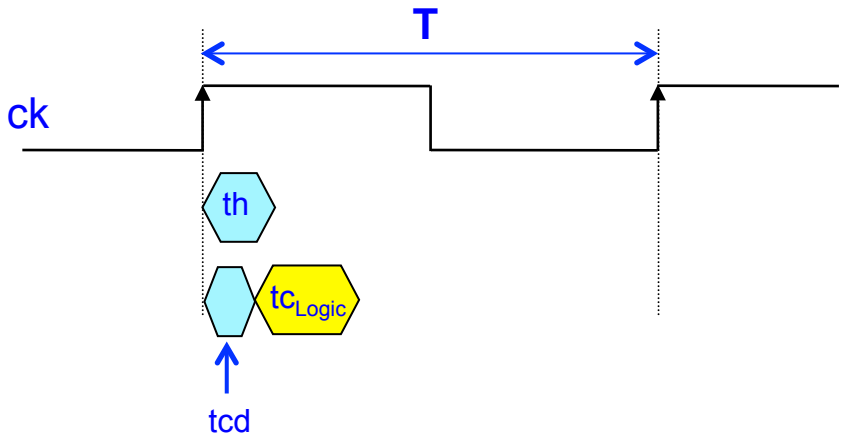
$$T \geq tco + td_{Logic} + tsu$$

$$f = 1/T$$

Avoiding Race Condition

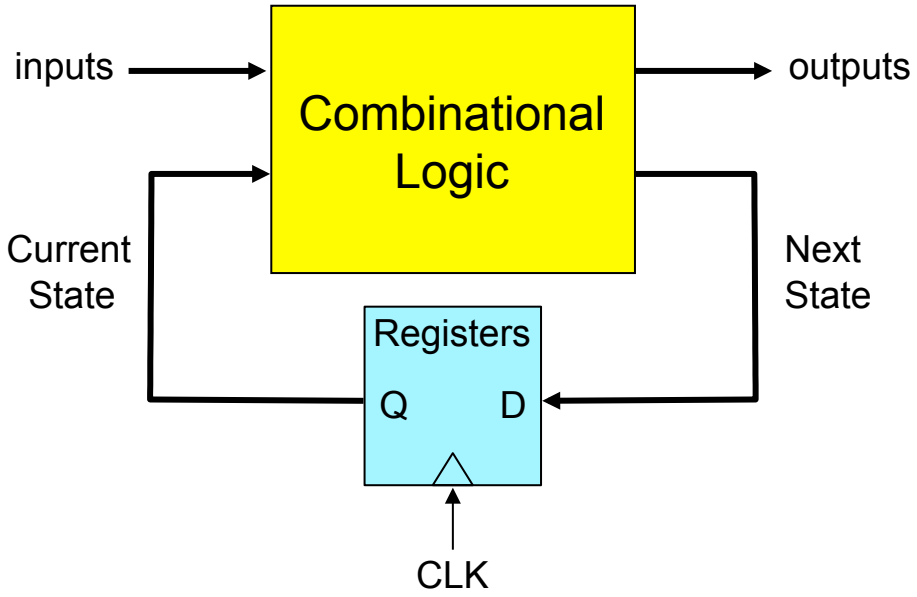
td_{Logic} = maximum propagation delay
tc_{Logic} = minimum propagation delay
(or *contamination delay*)

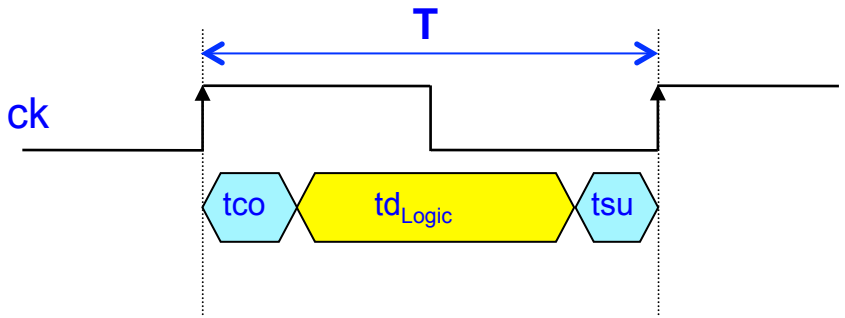




$$tcd + tc_{Logic} \geq th$$

Maximum Clock Frequency



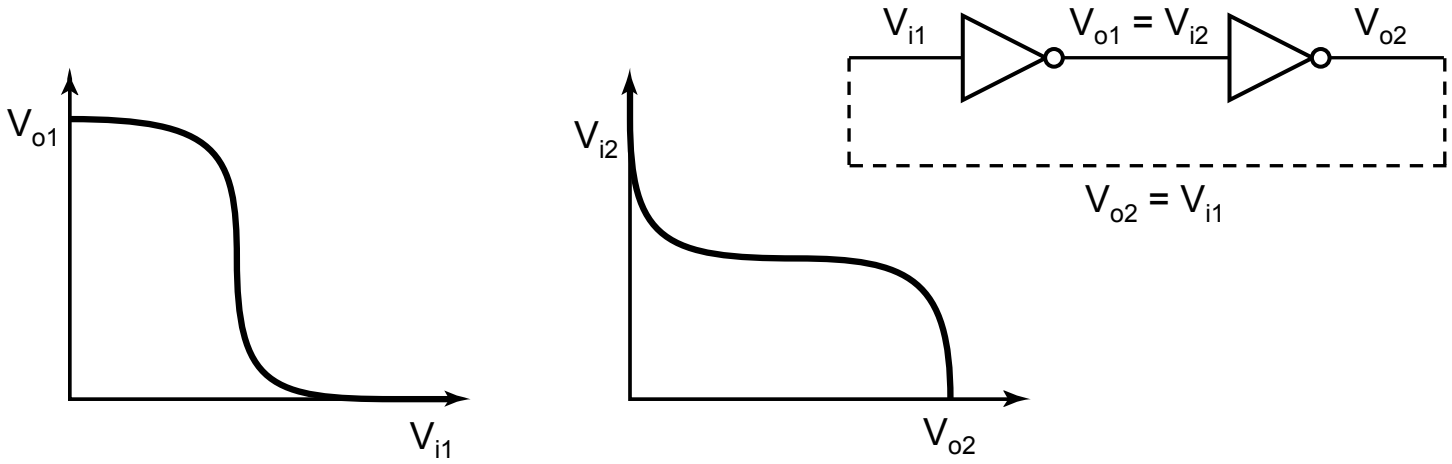


In contemporary designs:

- The maximum logic depth is around 12 gates
- Approx. 15% of the clock period is due to register overheads
- $tcd + tc_{Logic} \geq th$ is quite easy to meet if clock slew can be disregarded

CMOS Sequential Circuits

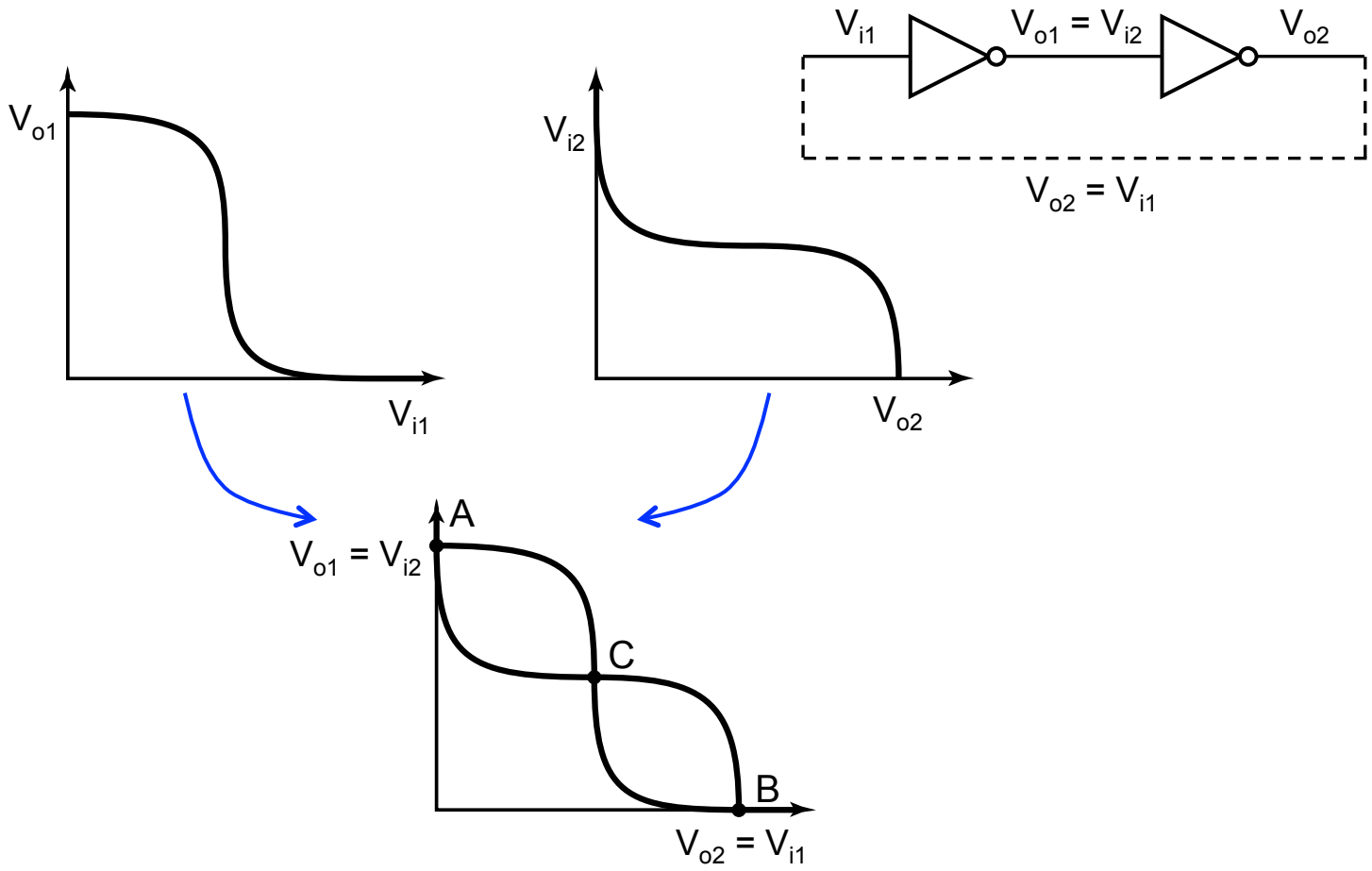
Positive Feedback: Bi-Stability



Source: Rabaey; Chandrakasan; Nikolic, 2003

CMOS Sequential Circuits

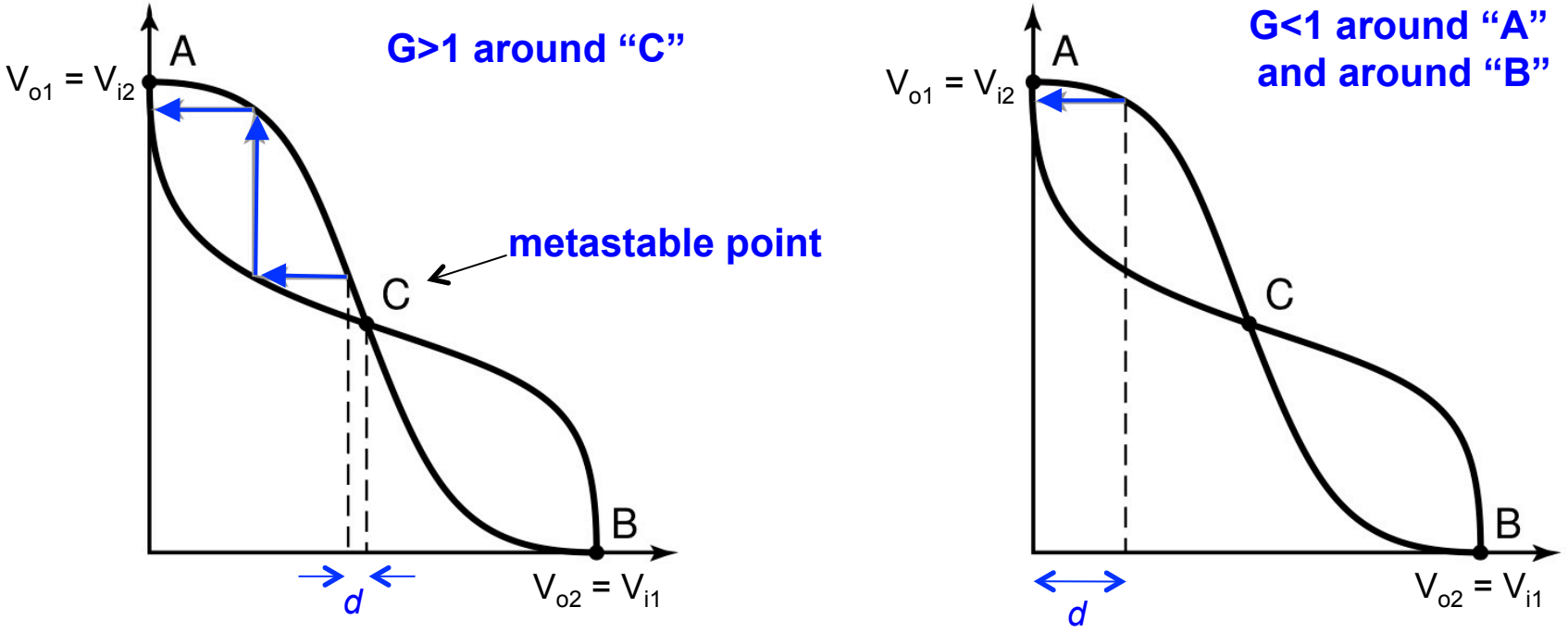
Positive Feedback: Bi-Stability



Source: Rabaey; Chandrakasan; Nikolic, 2003

CMOS Sequential Circuits

Meta-Stability

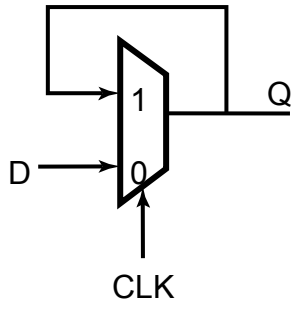


G is the loop gain

Source: Rabaey; Chandrakasan; Nikolic, 2003

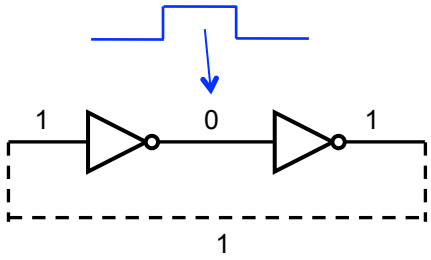
Changing the State of a Bistable

- **Cutting the feedback loop:**
  - Multiplexer-based structure
  - Once the loop is open, a new value can be easily written in
  - This is the most popular approach in today's latches



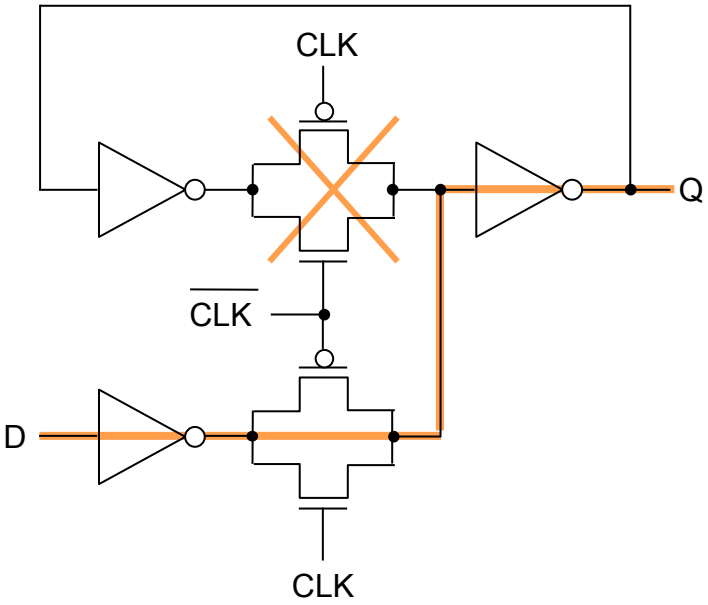
$$Q = Clk \cdot Q + \overline{Clk} \cdot D$$

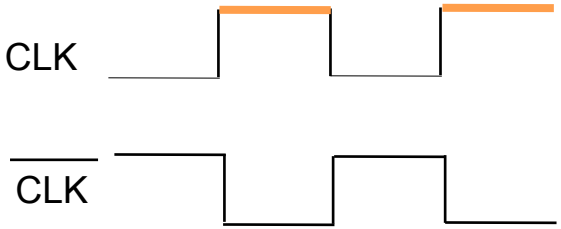
- **Overpowering the feedback loop:**
  - By applying a trigger signal at the input of the bistable a new value is forced into the cell
  - Careful sizing of the transistors in the feedback loop and trigger circuitry
  - Currently, is used to built static background memories



Writing into a Static Latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states

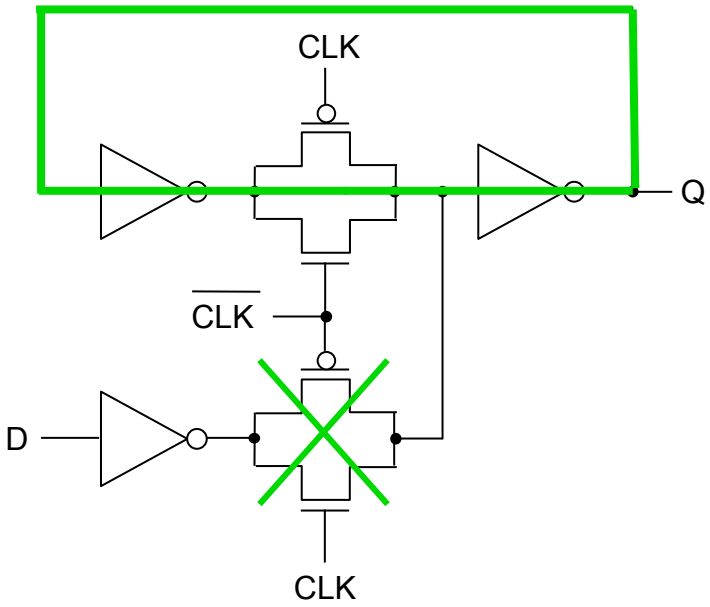


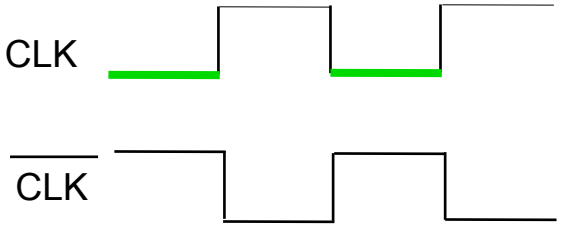


Converting into a MUX

Writing into a Static Latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states





Converting into a MUX

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Use the clock as a decoupling signal,
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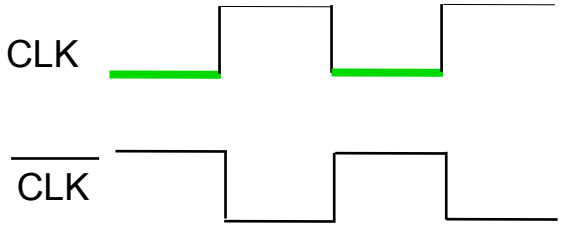
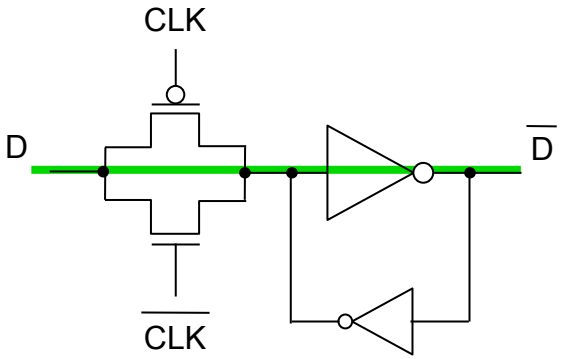


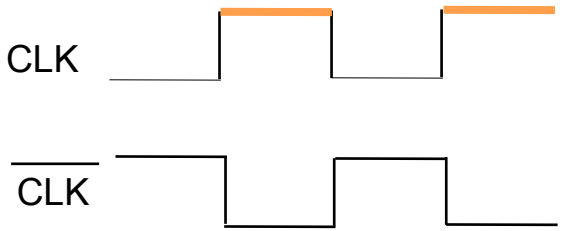


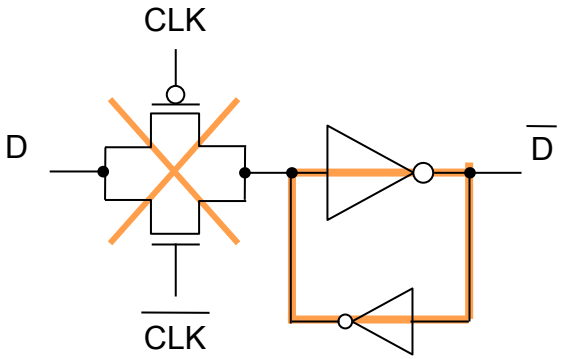
Forcing the state

If the transmission gate has minimum sized transistors, the lower inverter must be even weaker!

Writing into a Static Latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states





Forcing the state

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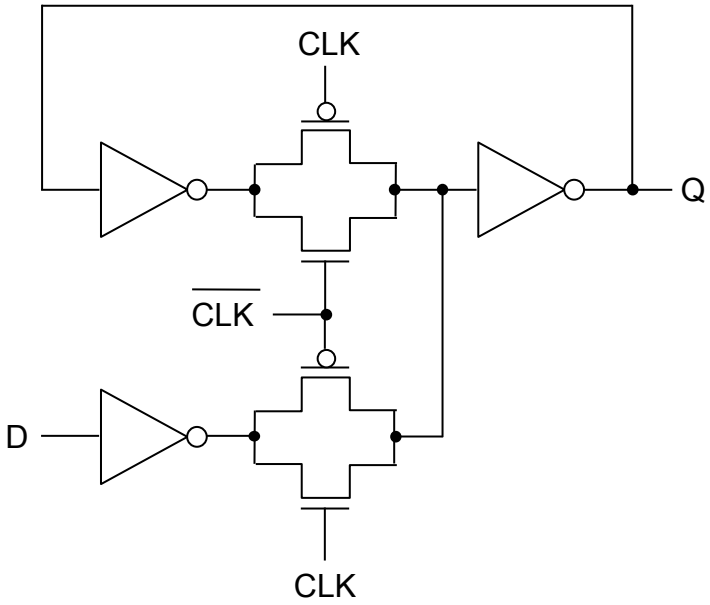
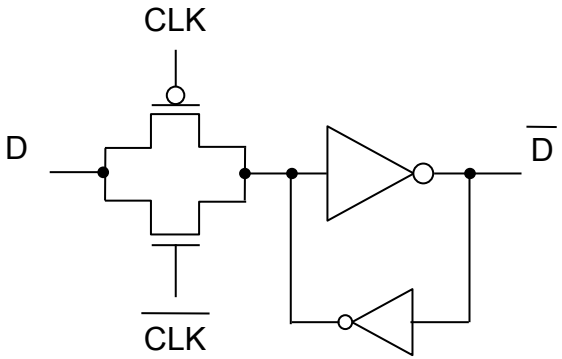
Writing into a Static Latch



Converting into a MUX

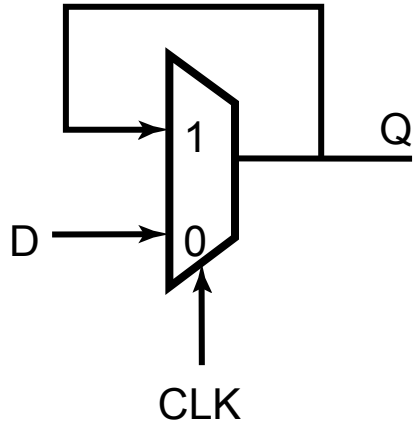


Forcing the state

CMOS Sequential Circuits

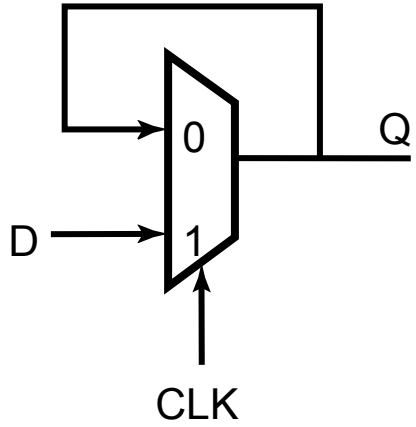
Mux-Based Latches

Negative latch (transparent when CLK= 0)



$$Q = Clk \cdot Q + \overline{Clk} \cdot D$$

Positive latch (transparent when CLK= 1)



$$Q = \overline{Clk} \cdot Q + Clk \cdot D$$

Source: Rabaey; Chandrakasan; Nikolic, 2003

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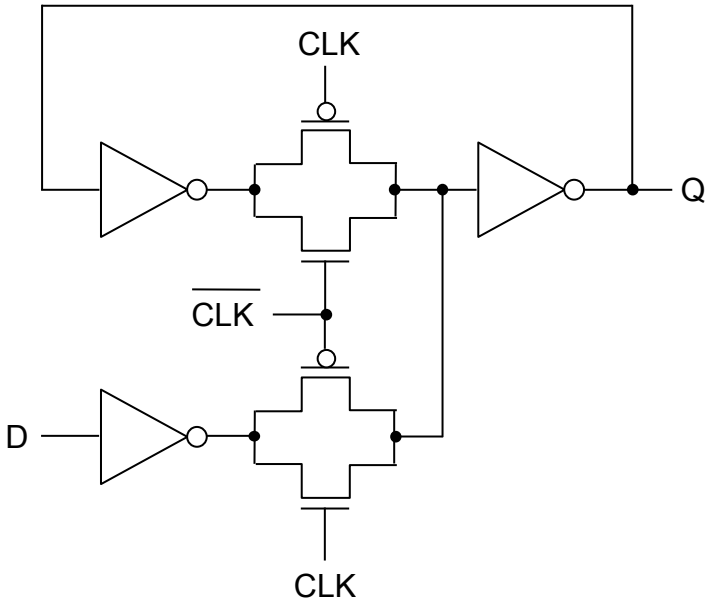
Mux-Based Latch



$$P = \alpha_{0\to1} \cdot C_L \cdot VDD^2 \cdot f$$

CLK: $\alpha_{0\to1} = 1$

How many transistor loads seen by CLK per bit?

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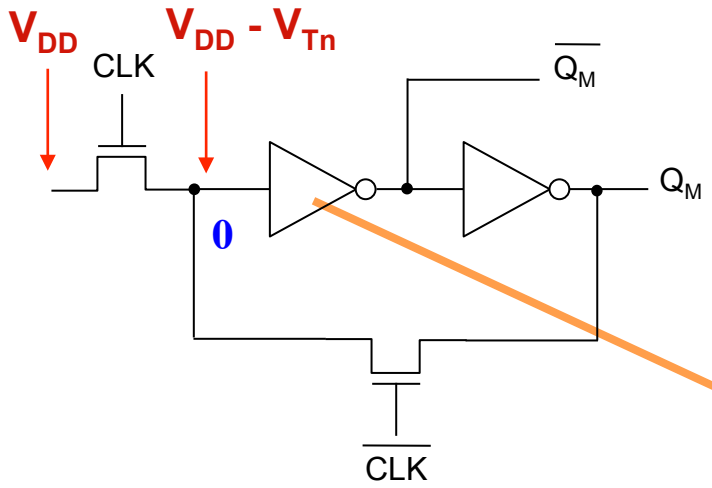
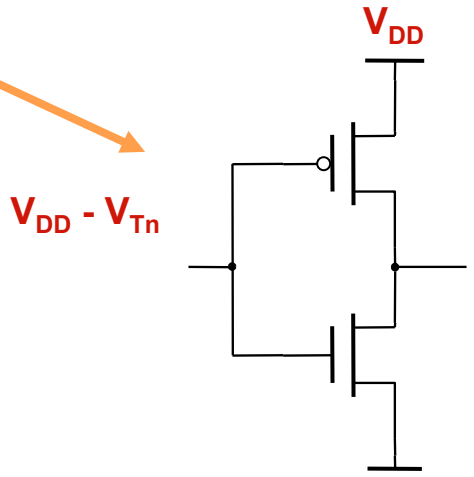
Mux-Based Latch

$V_{OH} = V_{DD} - V_{Tn}$



NMOS only

Noise margin degradation



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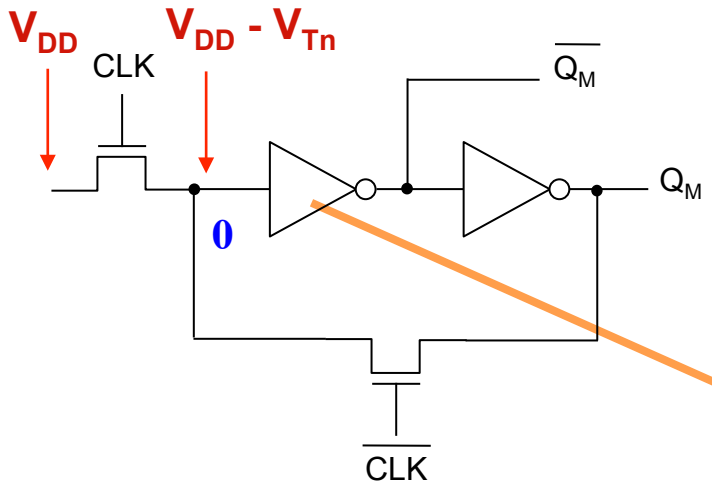
Mux-Based Latch



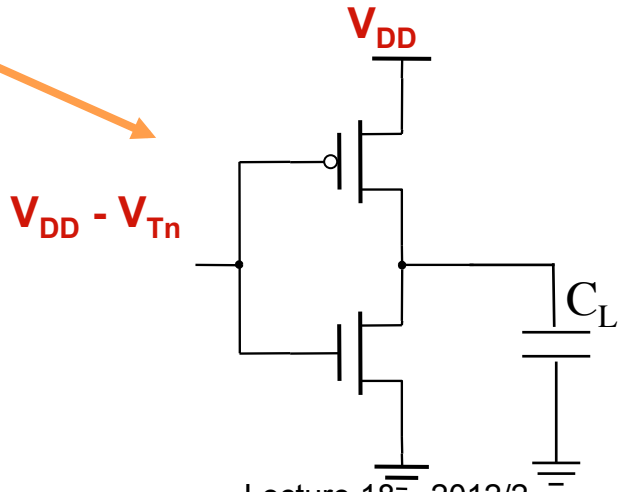
$$t_{pHL} \approx 0.69\, R_{eq\text{-}NMOS}\, C_L$$

$$R_{eq} \approx (R_{on}(t_1) + R_{on}(t_2))/2$$

$$R_{on}(t) \approx V_{DS}(t)/I_D(t)$$

$$I_D \approx \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

NMOS only



Switching performance degradation

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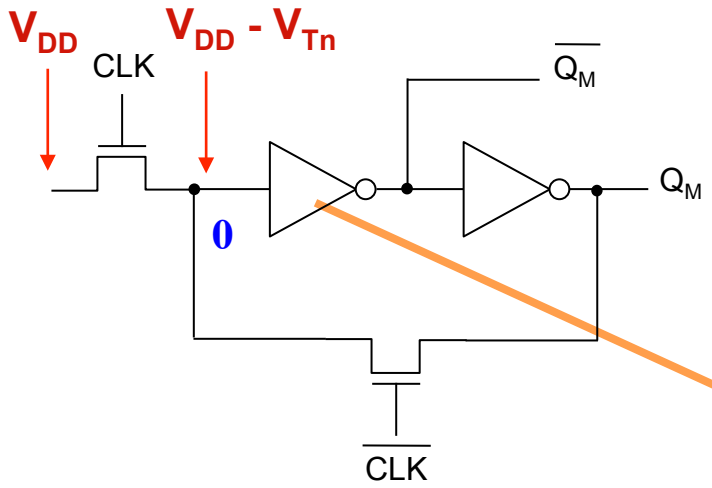
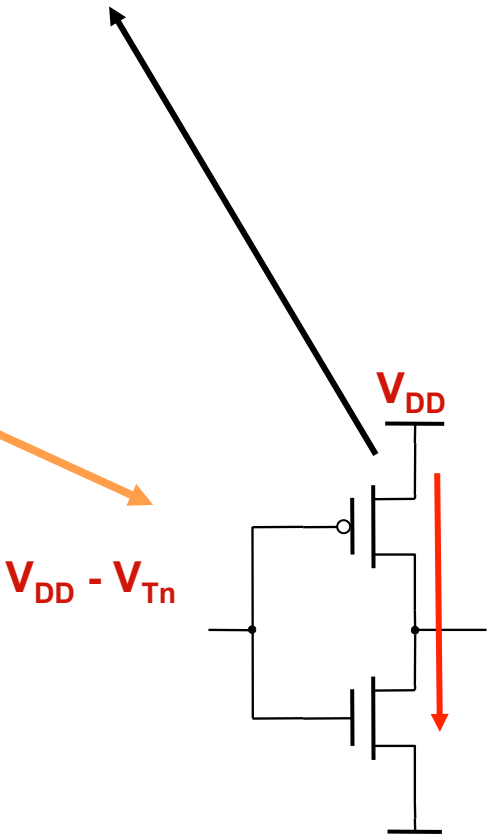
Mux-Based Latch



Not completely OFF

NMOS only



Short-circuit power increases

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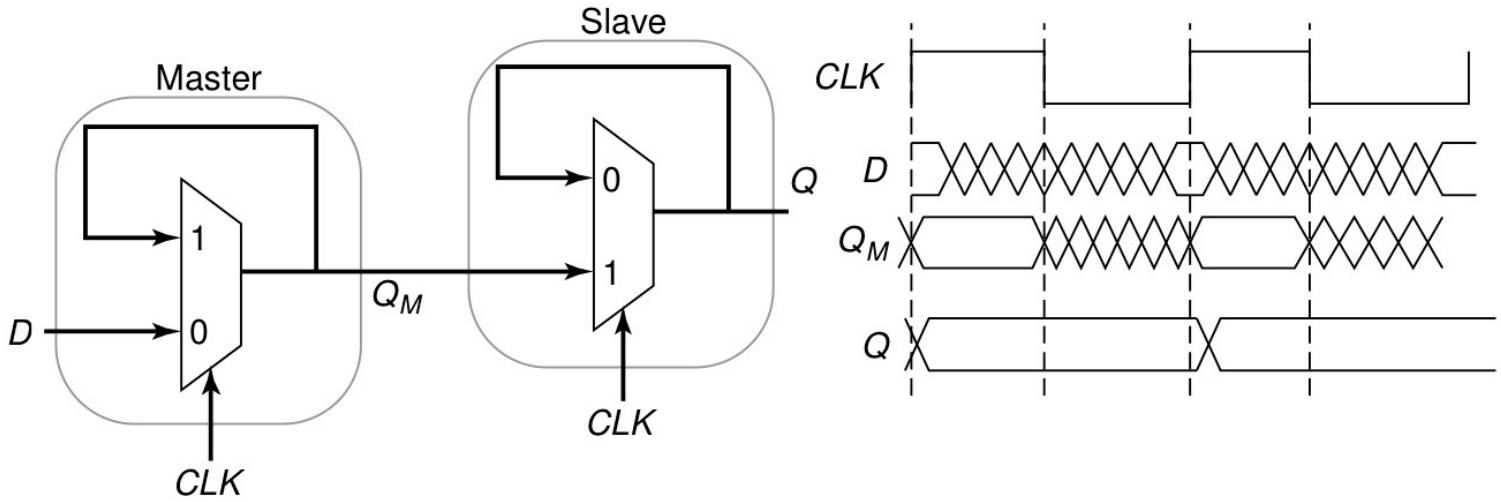
Master-Slave (Edge-Triggered) Register



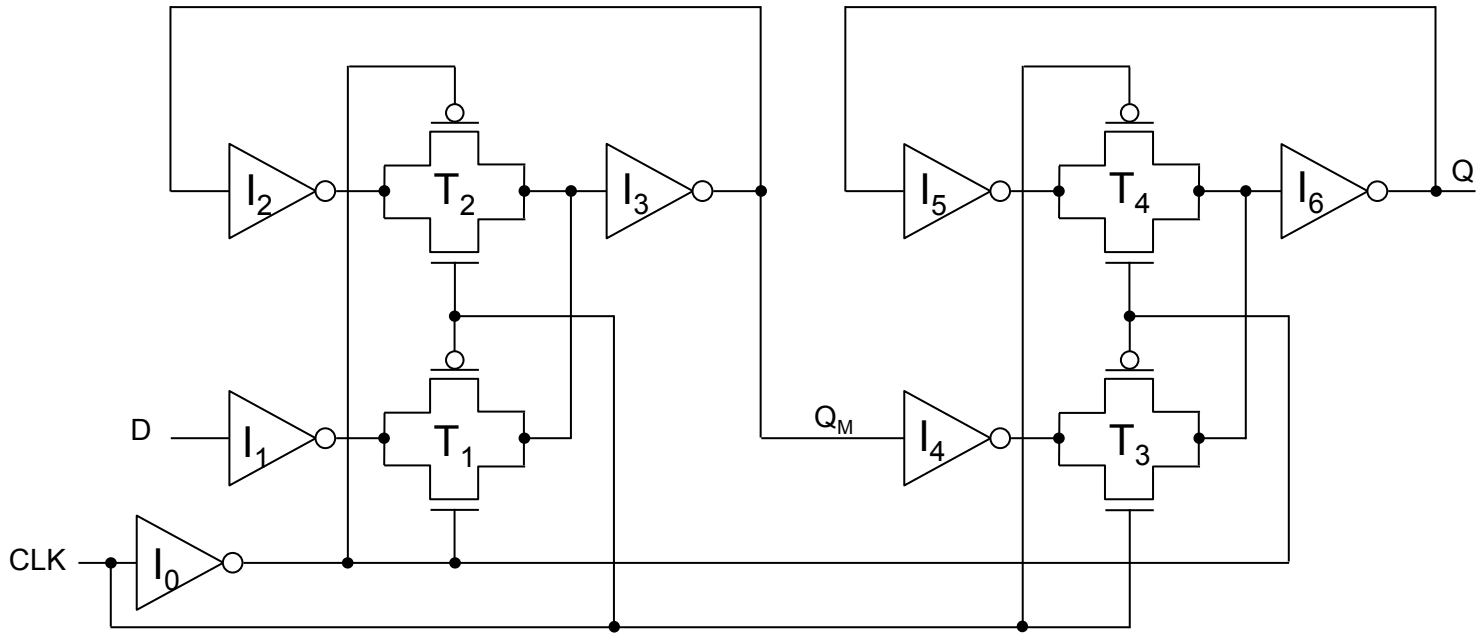
Two opposite latches trigger on edge
Also called master-slave latch pair

Source: Rabaey; Chandrakasan; Nikolic, 2003

CMOS Sequential Circuits

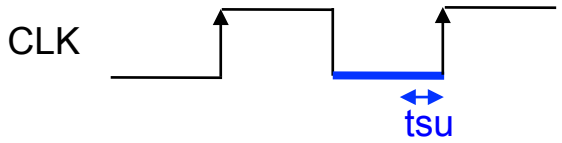
Master-Slave Register

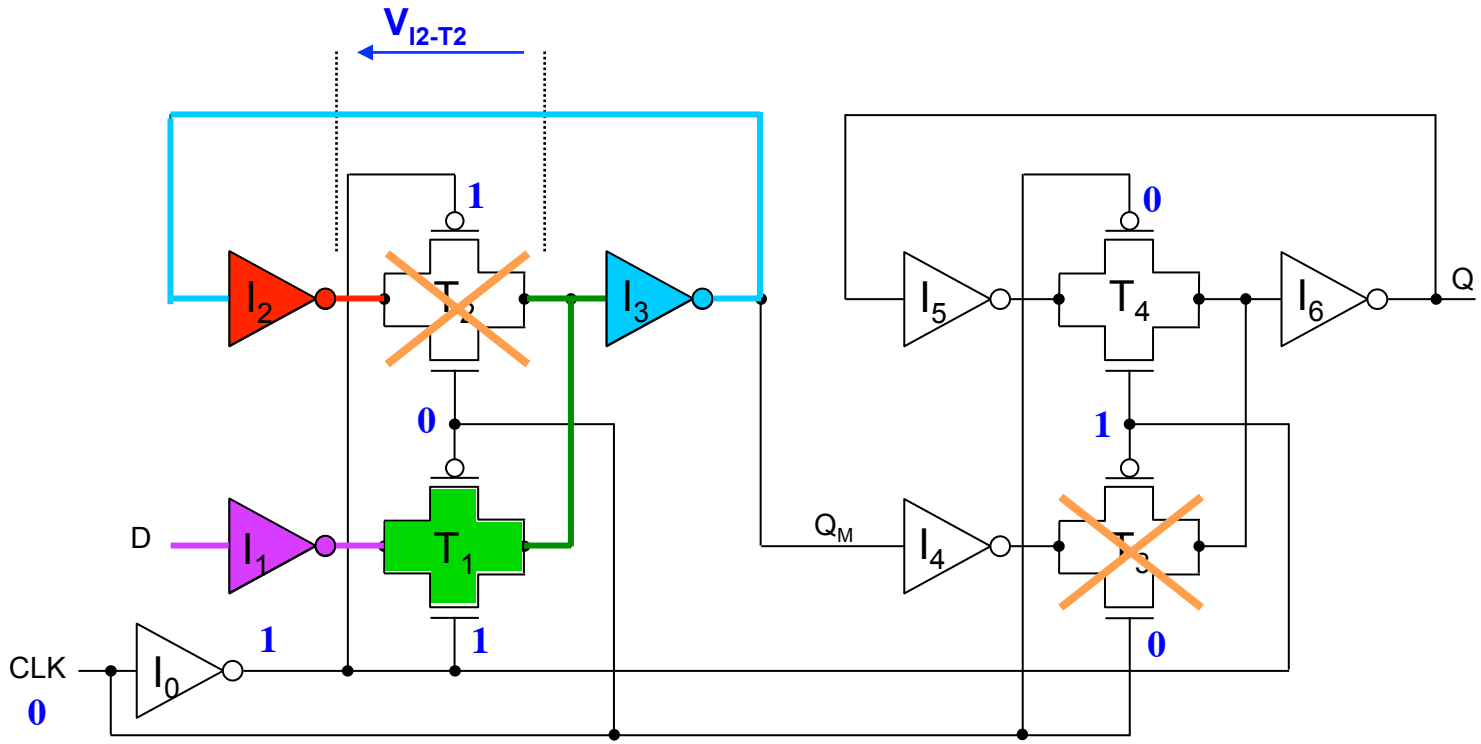
Multiplexer-based latch pair



Master-Slave Register

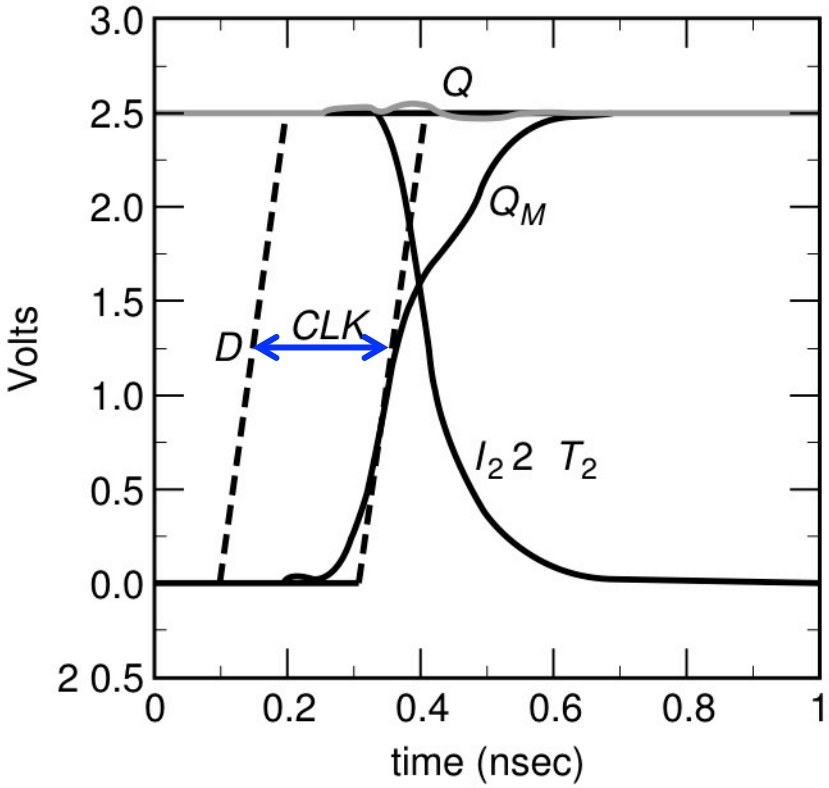
Multiplexer-based latch pair



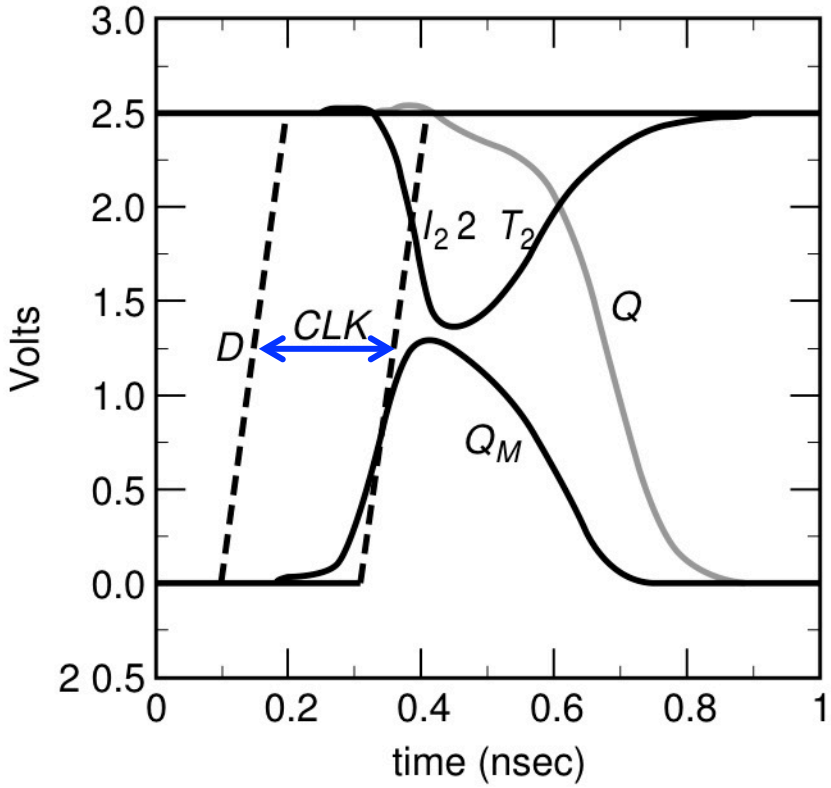


CMOS Sequential Circuits

Setup Time



tsu = 0.21 ns



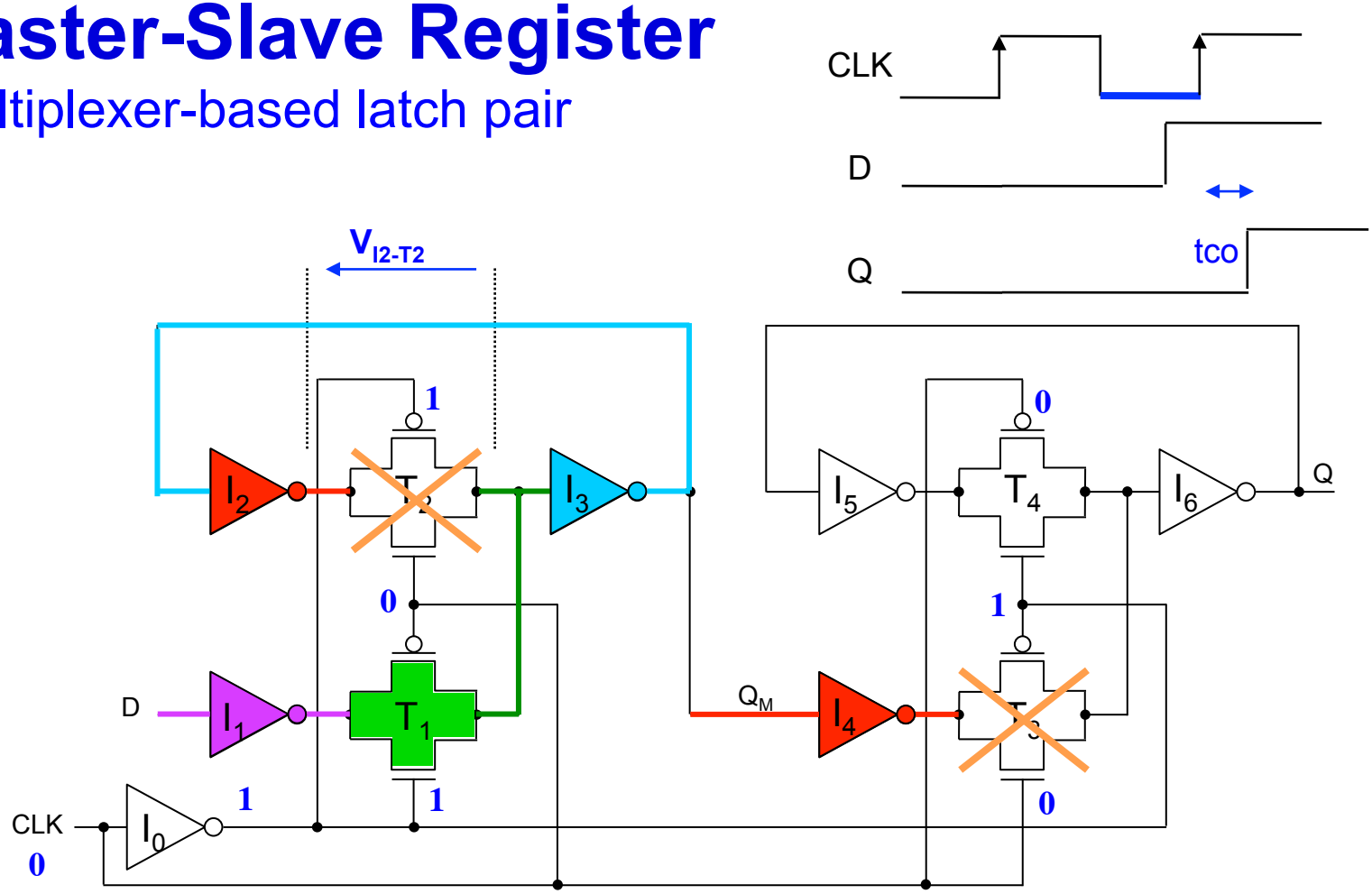
tsu = 0.20 ns

Source: Rabaey; Chandrakasan; Nikolic, 2003

CMOS Sequential Circuits

Master-Slave Register

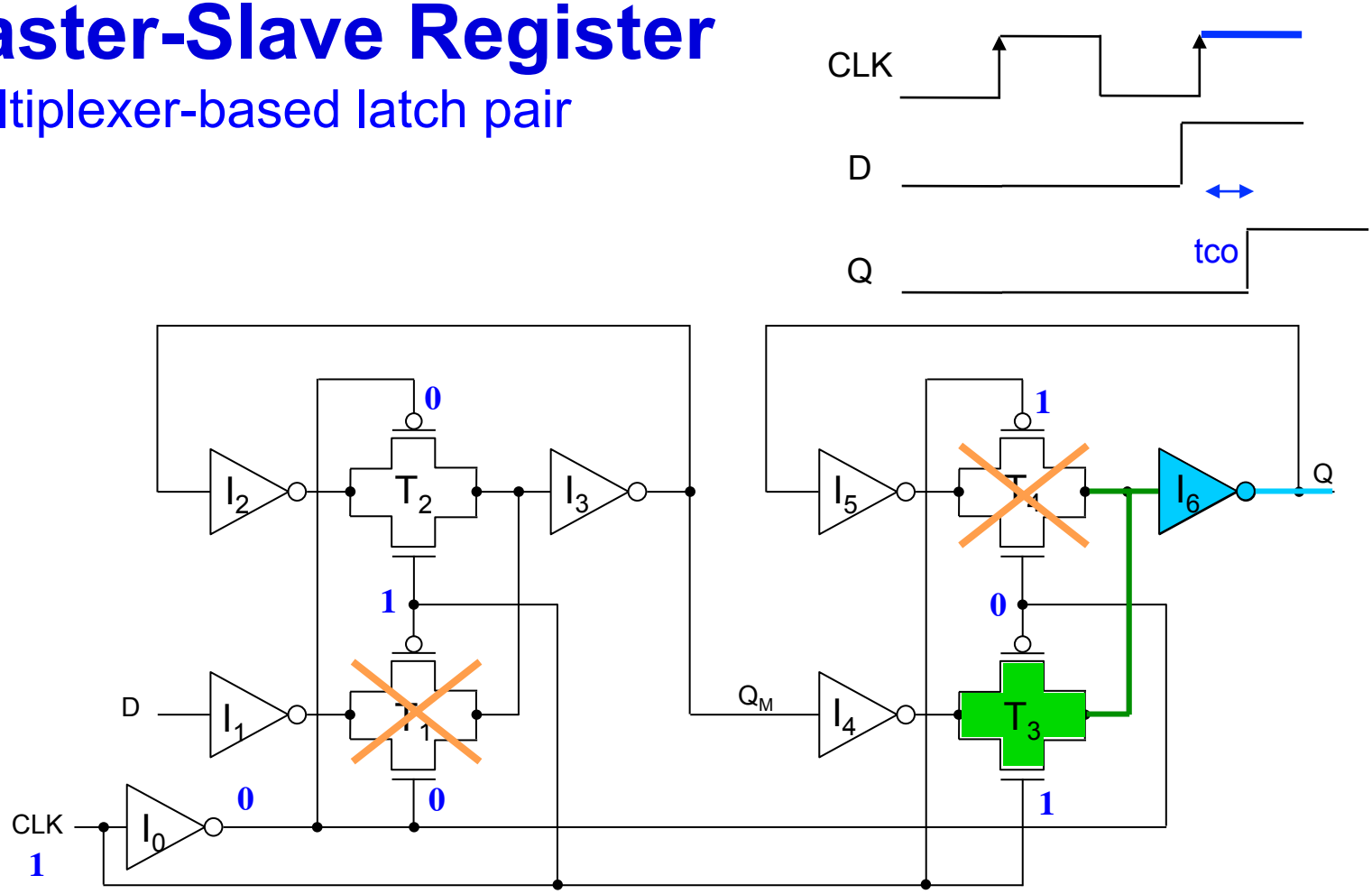
Multiplexer-based latch pair



CMOS Sequential Circuits

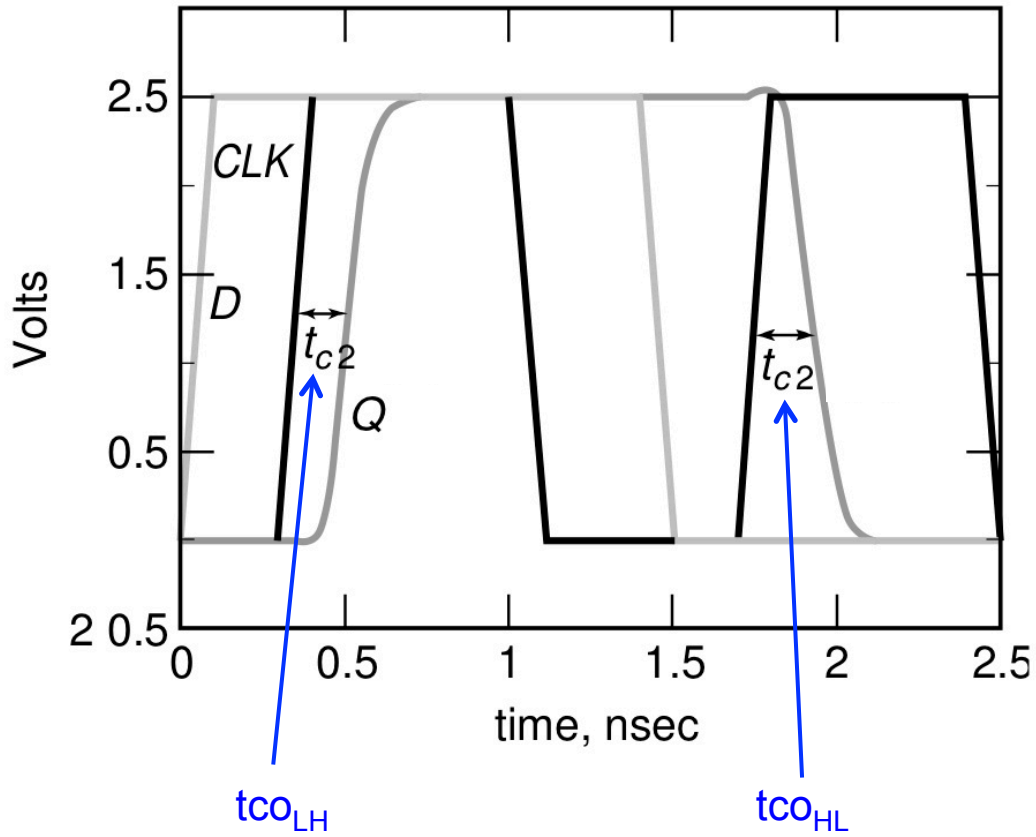
Master-Slave Register

Multiplexer-based latch pair



CMOS Sequential Circuits

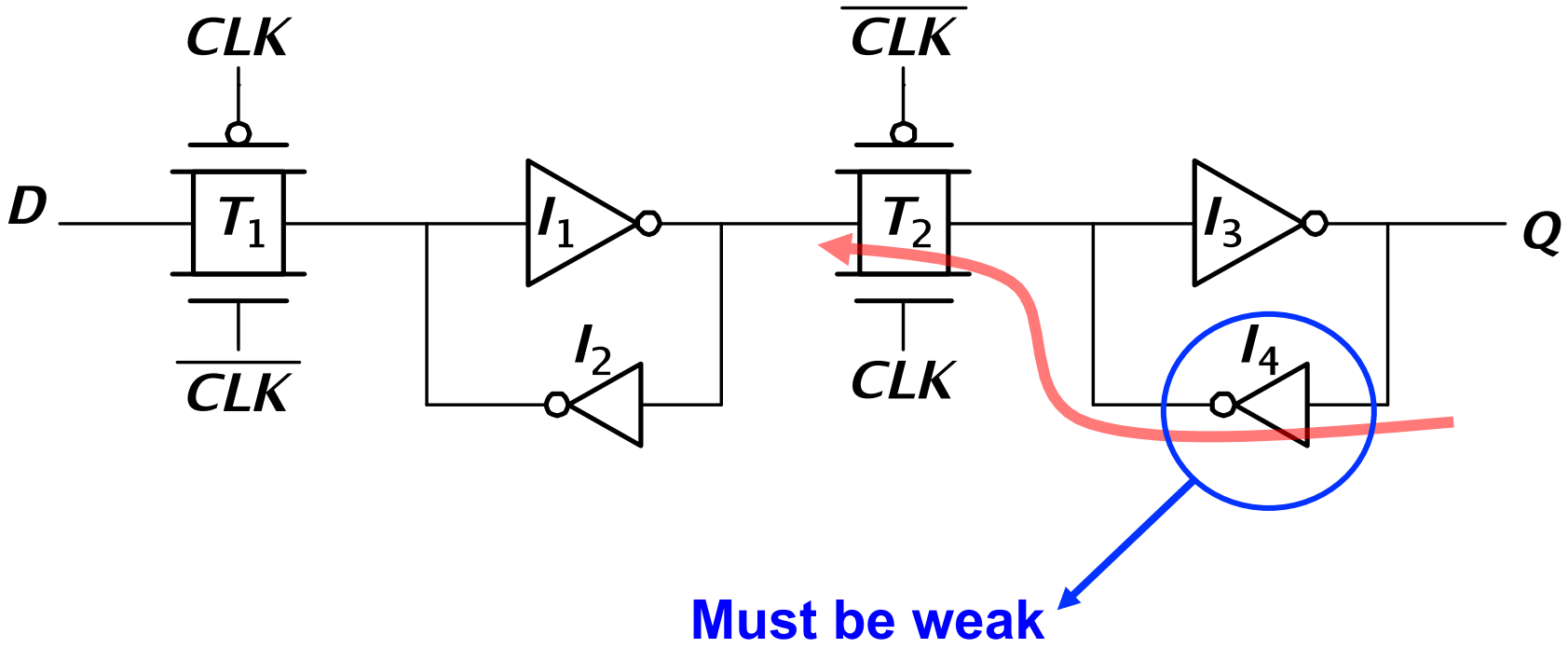
Clk to Output (Q) Delay



Source: Rabaey; Chandrakasan; Nikolic, 2003

CMOS Sequential Circuits

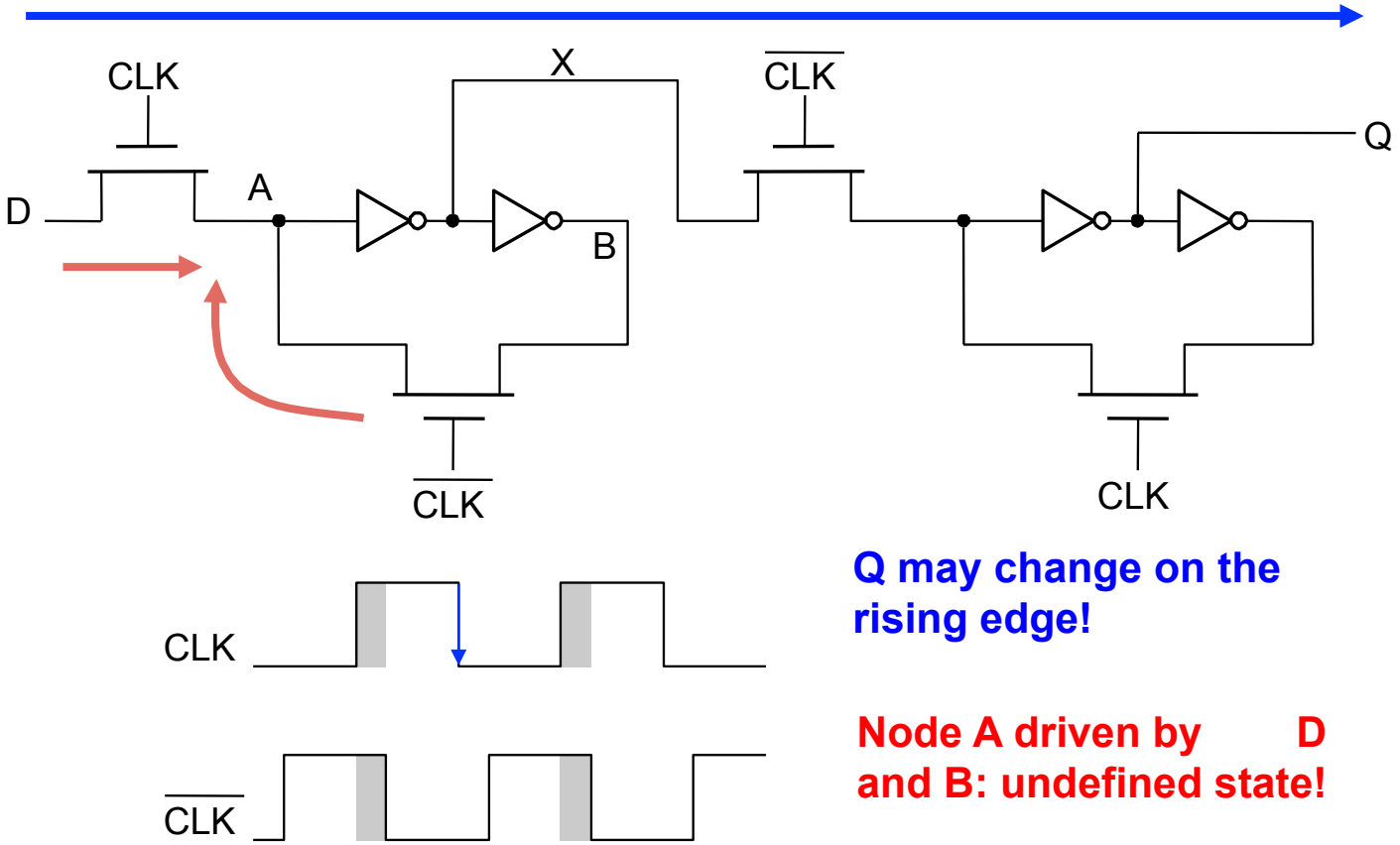
Reduced Clock Load Master-Salve Register



Source: Rabaey; Chandrakasan; Nikolic, 2003

CMOS Sequential Circuits

Avoiding Clock Overlap

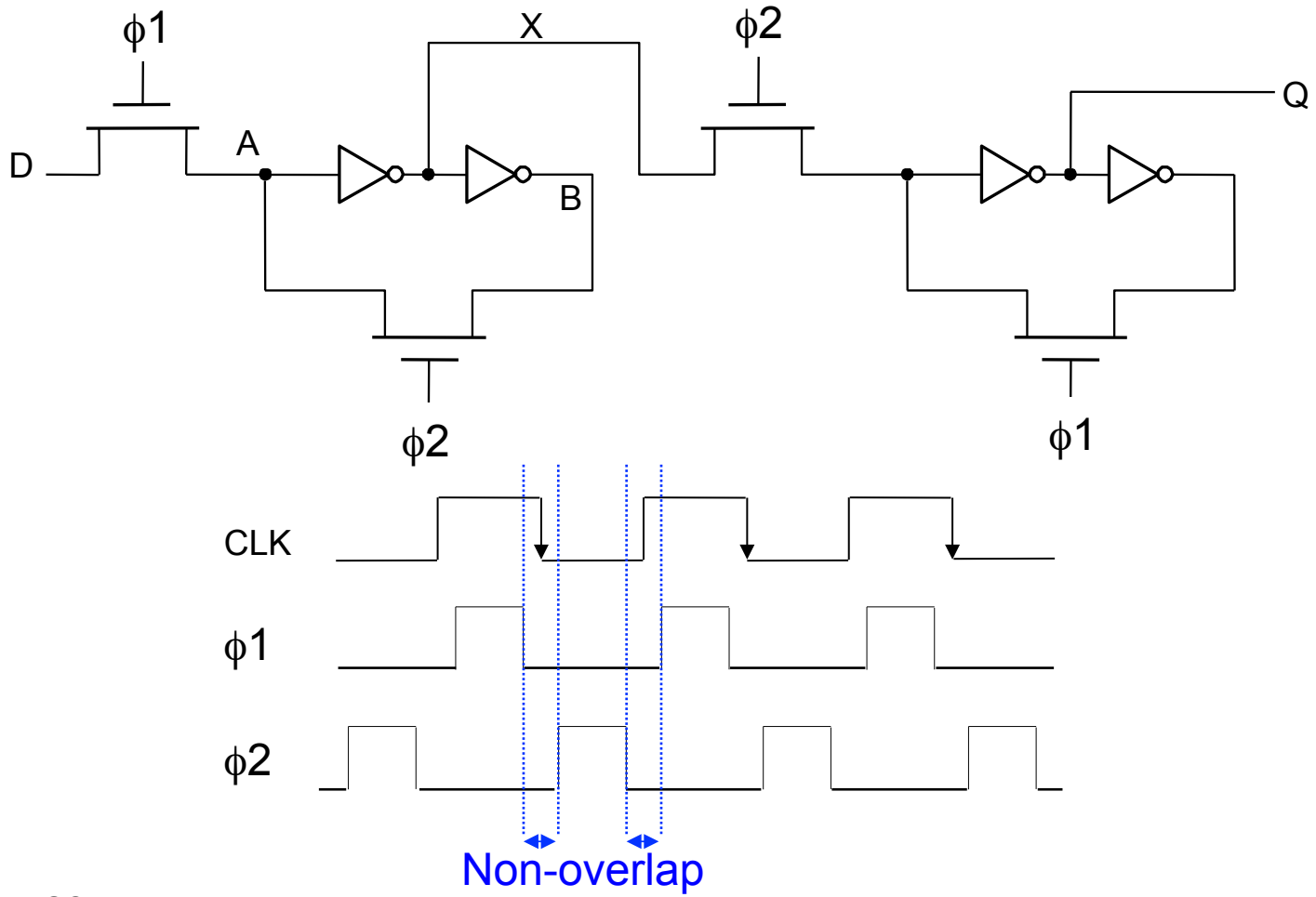


Q may change on the rising edge!

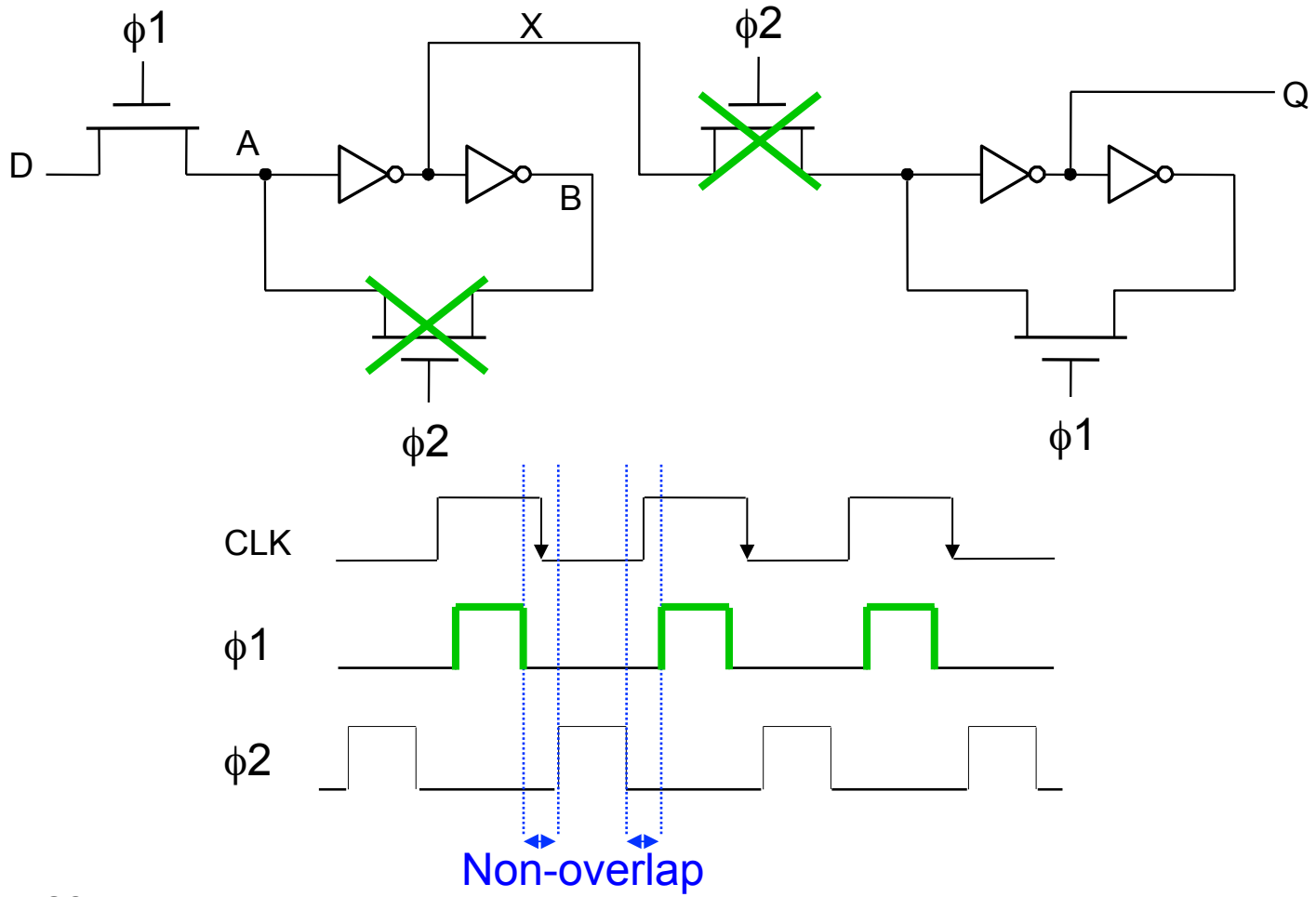
Node A driven by D and B: undefined state!

Source: Rabaey; Chandrakasan; Nikolic, 2003

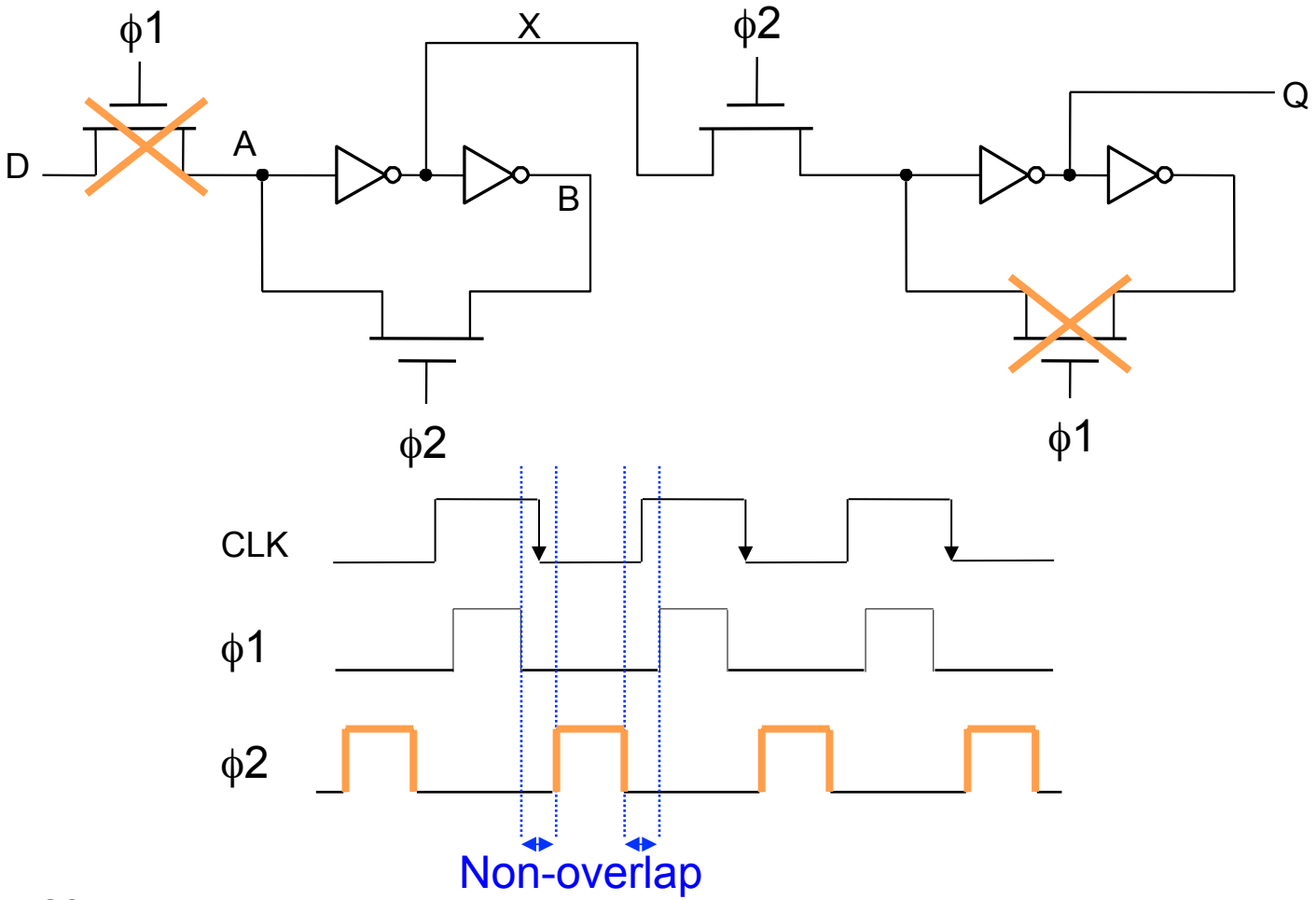
Avoiding Clock Overlap



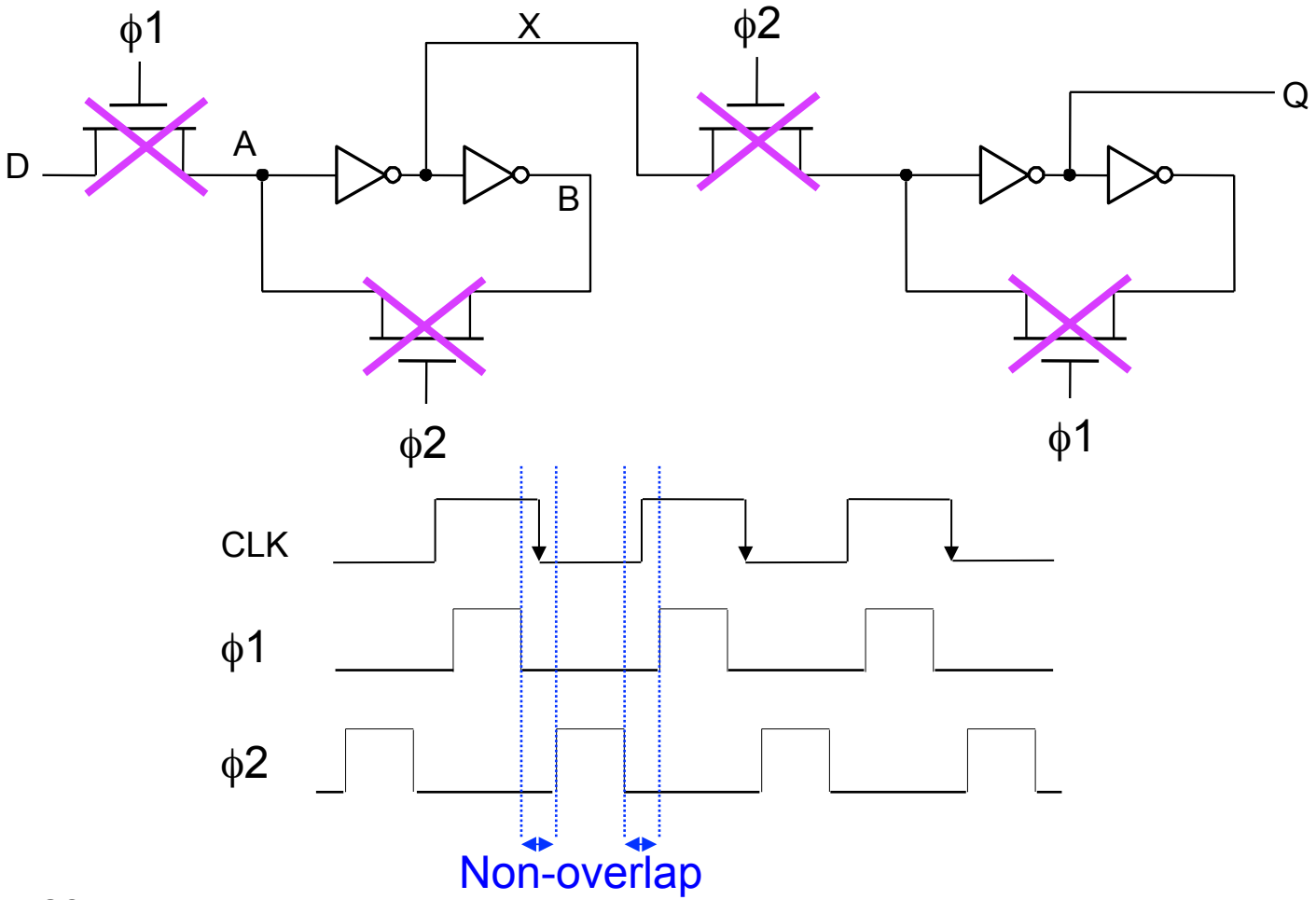
Avoiding Clock Overlap



Avoiding Clock Overlap

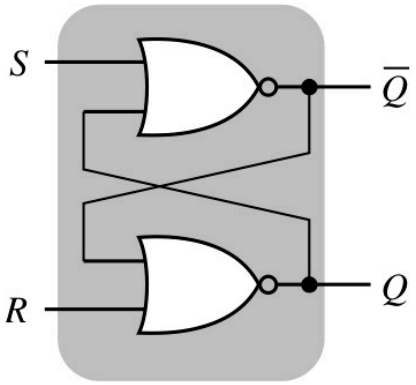


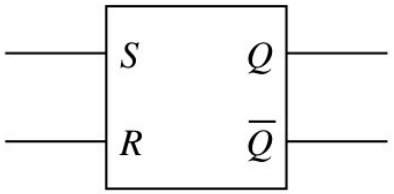
Avoiding Clock Overlap



Overpowering the Feedback Loop – Cross-Coupled Pairs

NOR-based set-reset





S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

Forbidden State

Source: Rabaey; Chandrakasan; Nikolic, 2003

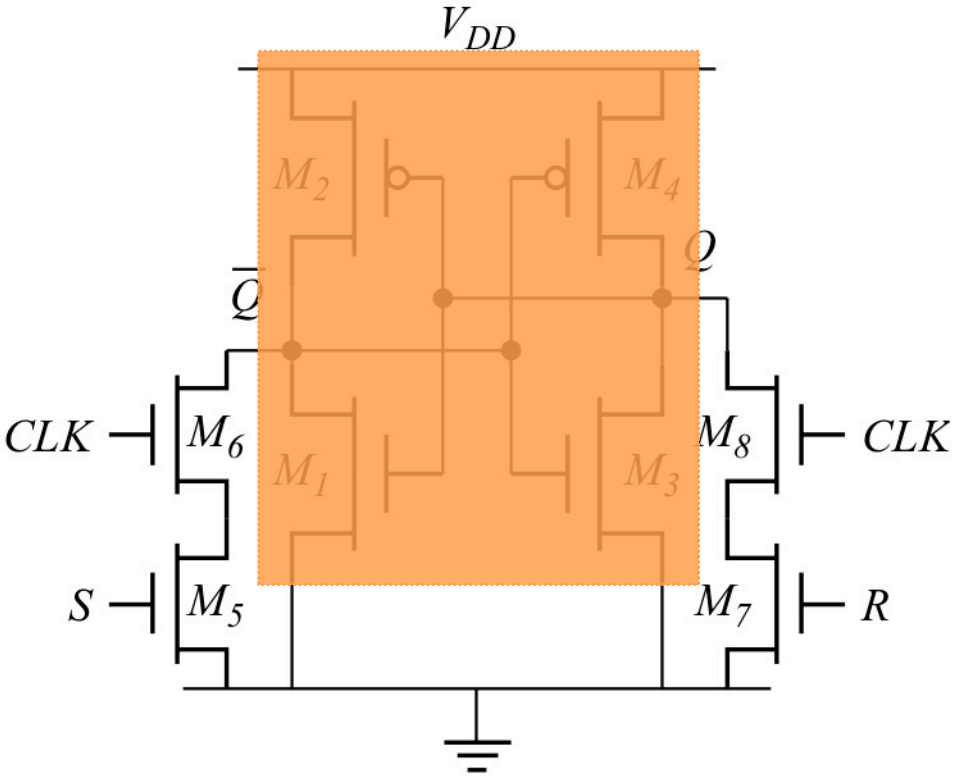
Asynchronous doesn't fit in dominant methodology!
(99% of the ICs are synchronous)

How to turn it into a synchronous circuit?

CMOS Sequential Circuits

Ratioed CMOS SR Latch

This is not used in datapaths any more, but is a basic building memory cell



$$(W/L)_{M2} = 3\,(W/L)_{M1} \qquad (W/L)_{M4} = 3\,(W/L)_{M3}$$

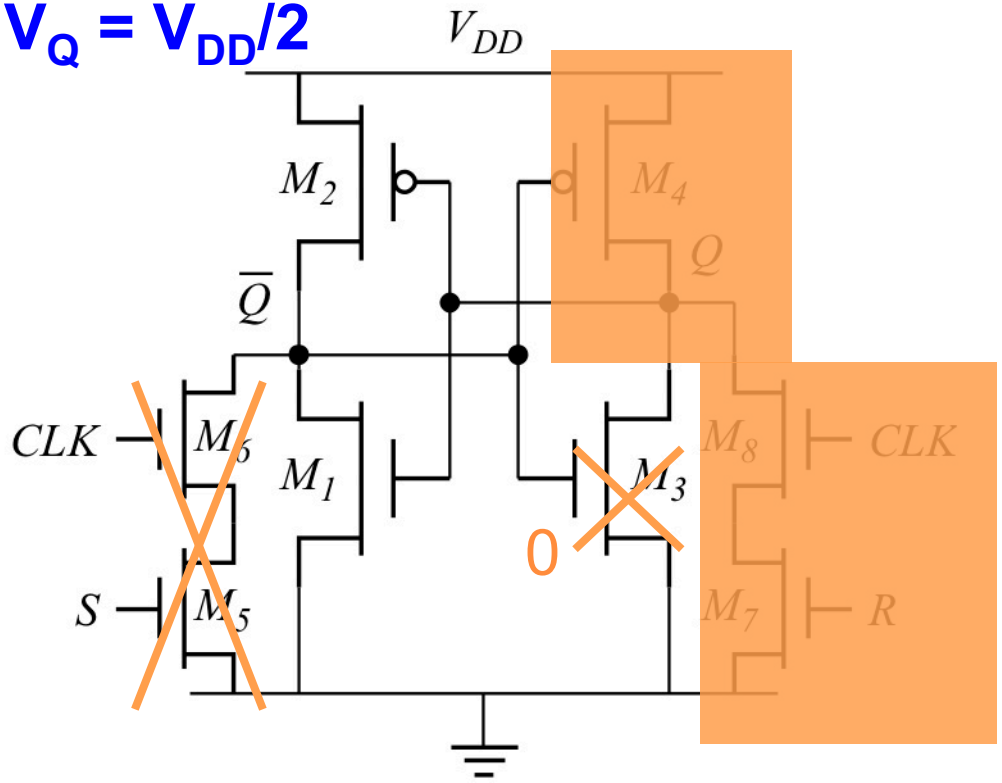
CMOS Sequential Circuits

Ratioed CMOS SR Latch

Q = 1: R = 1 @ CLK = 1 → Q = 0

$3(W/L)_{M7\text{-}M8} \approx (W/L)_{M4}$

$V_Q = V_{DD} \rightarrow V_Q = V_{DD}/2$



$(W/L)_{M2} = 3\,(W/L)_{M1}$ $\qquad$ $(W/L)_{M4} = 3\,(W/L)_{M3}$

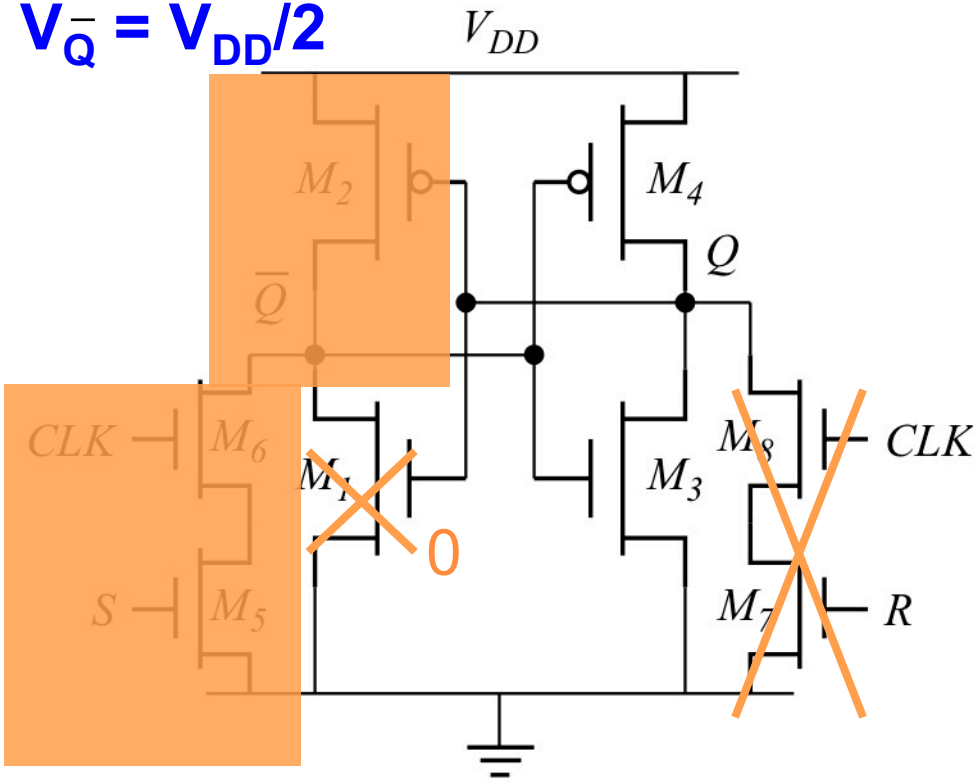
CMOS Sequential Circuits

Ratioed CMOS SR Latch

Q = 0: S = 1 @ CLK = 1 → Q = 1

$V_{\bar{Q}} = V_{DD} \rightarrow V_{\bar{Q}} = V_{DD}/2$

$3(W/L)_{M5\text{-}M6} \approx (W/L)_{M2}$



$(W/L)_{M2} = 3\,(W/L)_{M1}$ $\quad$ $(W/L)_{M4} = 3\,(W/L)_{M3}$

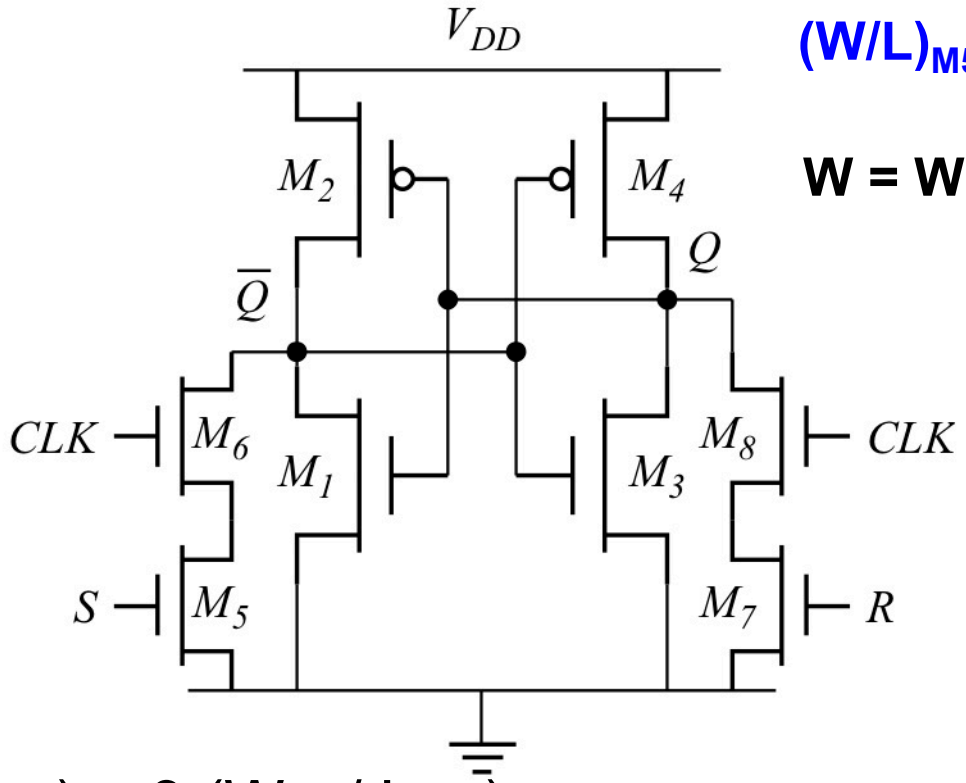
CMOS Sequential Circuits

Ratioed CMOS SR Latch

$3(W/L)_{M5\text{-}M6} \approx (W/L)_{M2} = (W_{M2}/L_{min}) = (3W_{M1}/L_{min})$

$(W/L)_{M5\text{-}M6} = W/(2\ L_{min})$

$W = W_{M5} = W_{M6}$

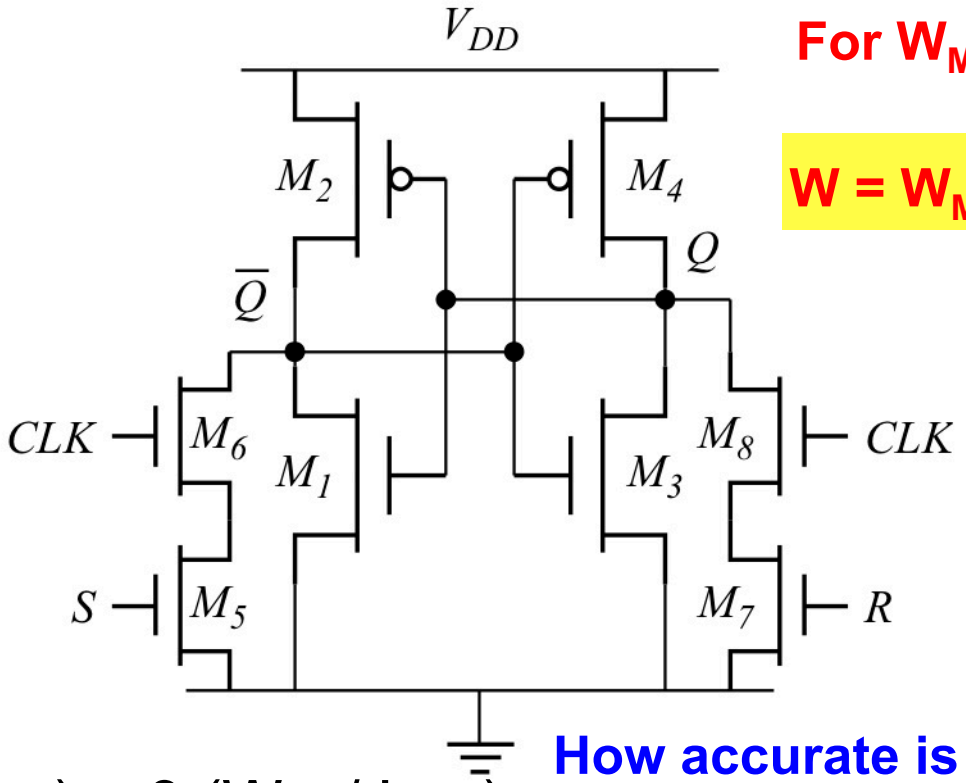


$(W_{M2}/L_{min}) = 3\ (W_{M1}/\ L_{min})$

CMOS Sequential Circuits

Ratioed CMOS SR Latch

$3(W/L)_{M5\text{-}M6} \approx 3\ W/(2\ L_{min}) = 3\ W_{M1}/L_{min}$



For $W_{M1} = 2\ L_{min}$:

$W = W_{M5} = W_{M6} \approx 4\ L_{min}$

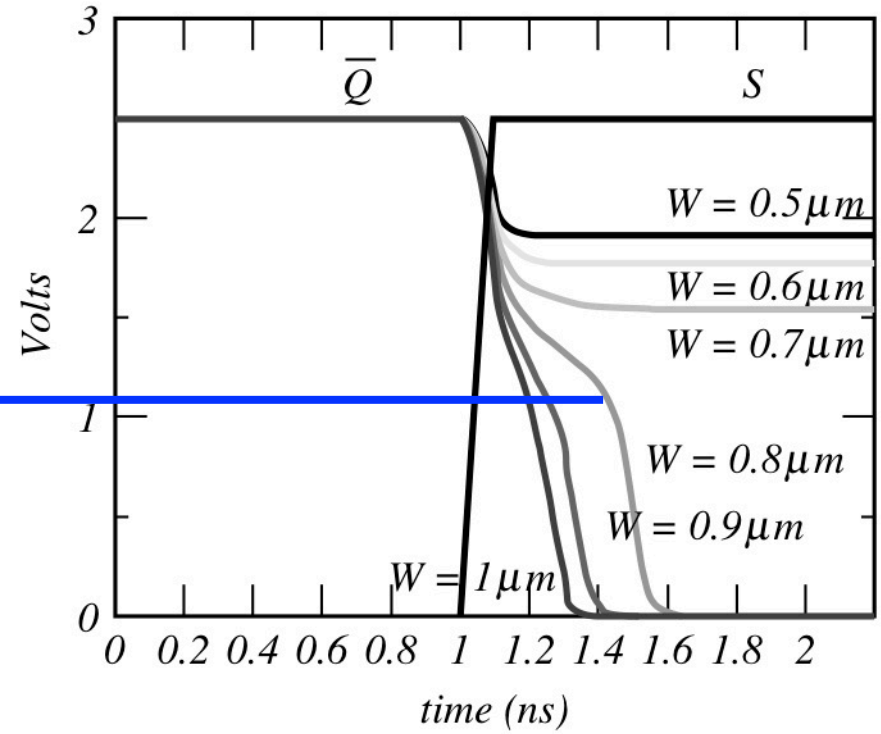
$(W_{M2}/L_{min}) = 3\ (W_{M1}/\ L_{min})$

How accurate is the value of W for $L_{min} = 0.25\ \mu$ and $W_{M1} = 0.5\ \mu$?

CMOS Sequential Circuits

Ratioed CMOS SR Latch Sizing Issues

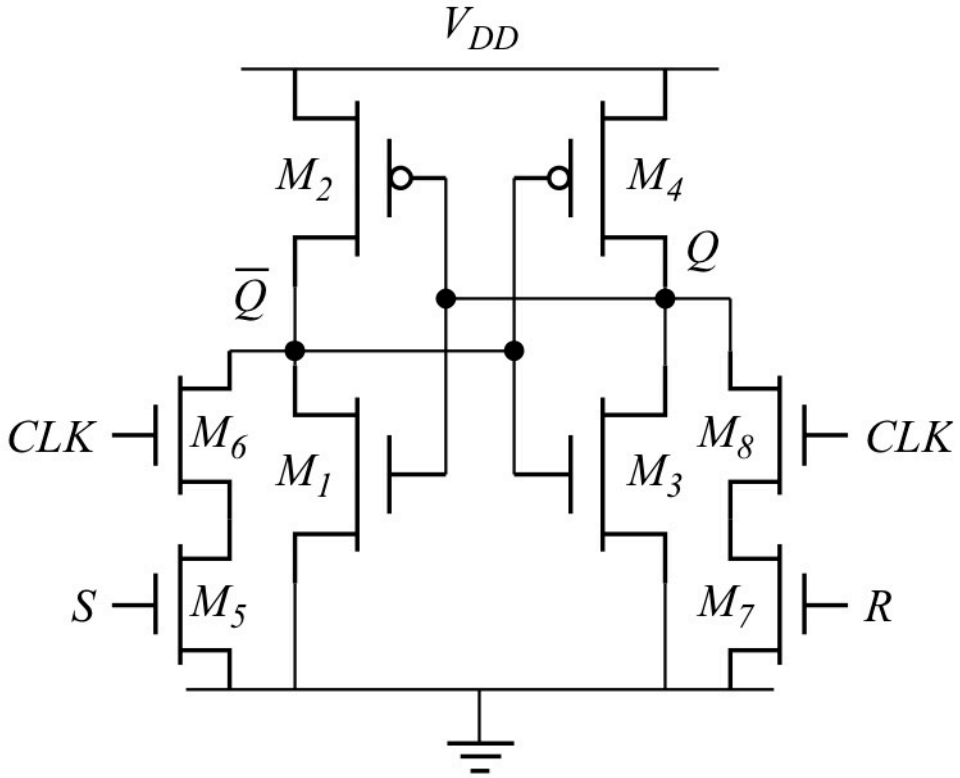
W≈3 L_{min} is enough!



Transient response

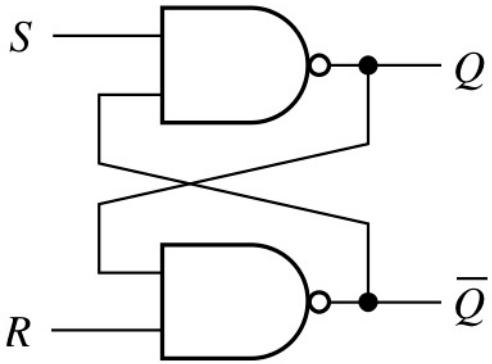
CMOS Sequential Circuits

Synchronized Cross-Coupled NAND



Requires proper transitor sizing: ratioed design.

Cross-Coupled NAND

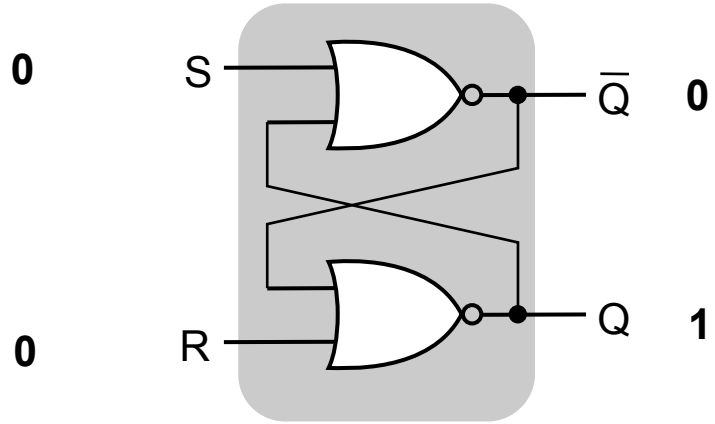


What is the corresponding truth table?

For a given tp, which requires more area synchronized cross-coupled NOR or NAND?

CMOS Sequential Circuits

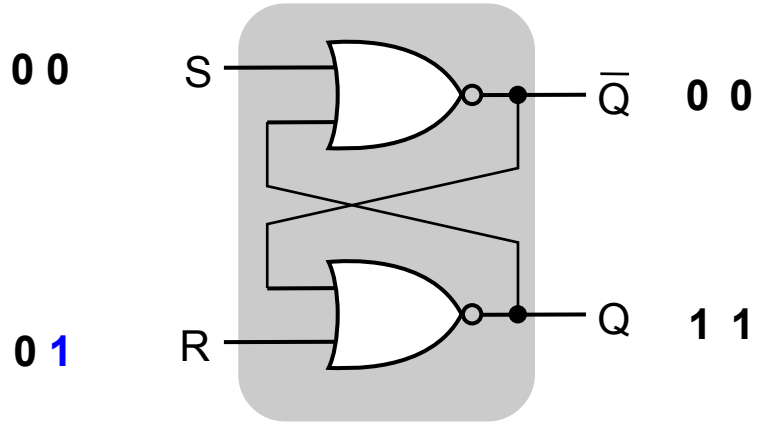
Generating Two-Phase Non-Overlapping Clock



Initial Values

CMOS Sequential Circuits

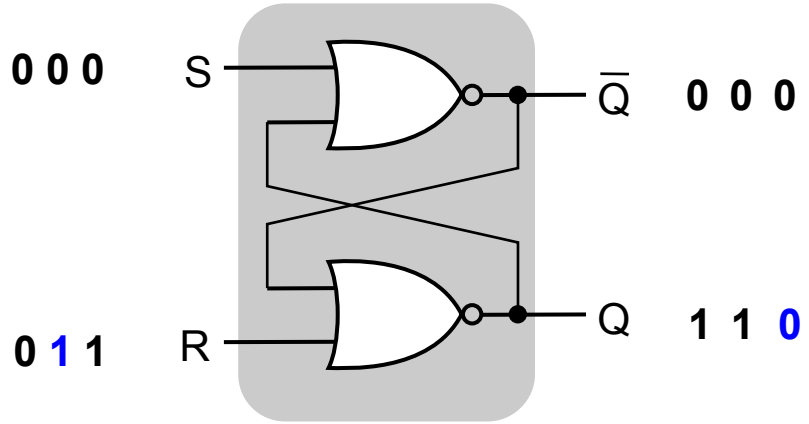
Generating Two-Phase Non-Overlapping Clock



Time = t_o

CMOS Sequential Circuits

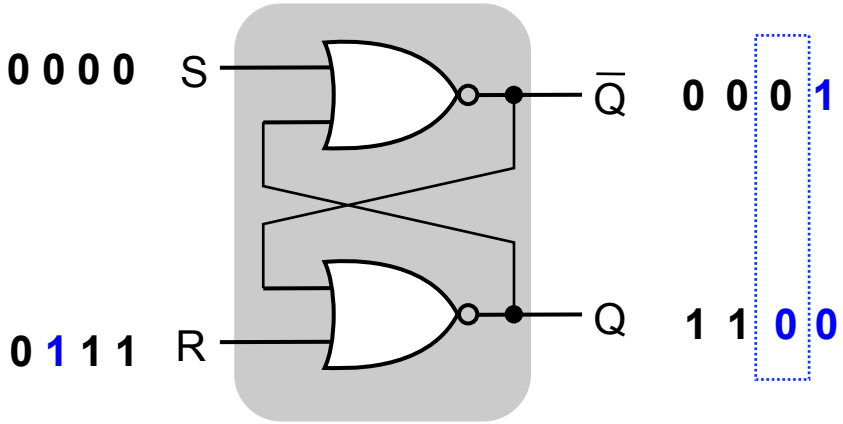
Generating Two-Phase Non-Overlapping Clock



Time = t_o + d

CMOS Sequential Circuits

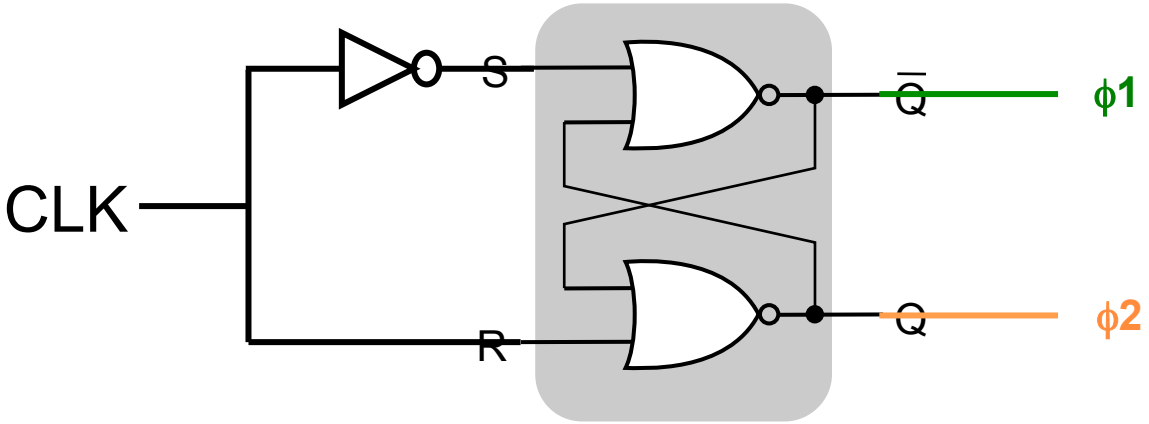
Generating Two-Phase Non-Overlapping Clock

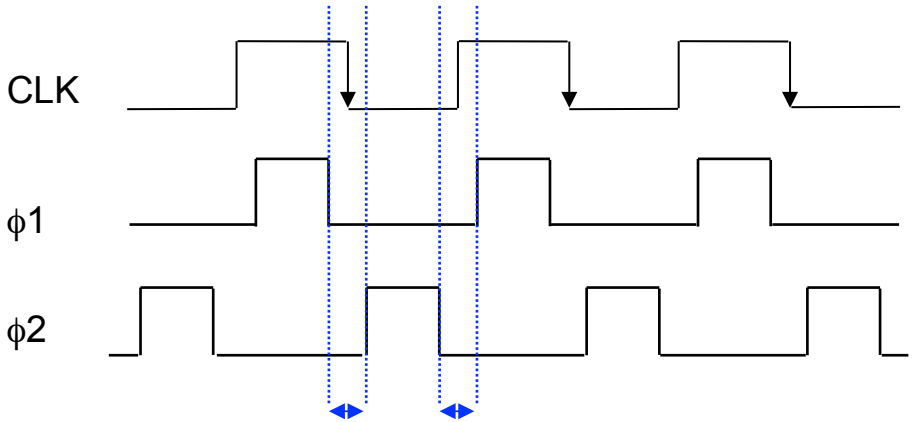


Time = t_o + 2d

CMOS Sequential Circuits

Generating Two-Phase Non-Overlapping Clock





References

1. RABAEY, J; CHANDRAKASAN, A.; NIKOLIC, B. **Digital Integrated Circuits**: a design perspective. 2nd Edition. Prentice Hall, 2003. ISBN: 0-13-090996-3.

2. WESTE, Neil; HARRIS, David. **CMOS VLSI Design:** a circuits and systems perspective. Addison-Wesley, 4th Edition, 2010. ISBN 978-0321547743.