PRACTICAL DESIGN TECHNIQUES FOR SENSOR SIGNAL CONDITIONING

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PRACTICAL DESIGN TECHNIQUES FOR SENSOR SIGNAL CONDITIONING

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Walt Kester
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PRACTICAL DESIGN TECHNIQUES FOR SENSOR SIGNAL CONDITIONING

SECTION 1
INTRODUCTION
Walt Kester

This book deals with sensors and associated signal conditioning circuits. The topic is broad, but the focus of this book is to concentrate on circuit and signal processing applications of sensors rather than the details of the actual sensors themselves.

Strictly speaking, a *sensor* is a device that receives a signal or stimulus and responds with an electrical signal, while a *transducer* is a converter of one type of energy into another. In practice, however, the terms are often used interchangeably.

Sensors and their associated circuits are used to measure various physical properties such as temperature, force, pressure, flow, position, light intensity, etc. These properties act as the stimulus to the sensor, and the sensor output is conditioned and processed to provide the corresponding measurement of the physical property. We will not cover all possible types of sensors, only the most popular ones, and specifically, those that lend themselves to process control and data acquisition systems.

Sensors do not operate by themselves. They are generally part of a larger system consisting of signal conditioners and various analog or digital signal processing circuits. The *system* could be a measurement system, data acquisition system, or process control system, for example.

Sensors may be classified in a number of ways. From a signal conditioning viewpoint it is useful to classify sensors as either *active* or *passive*. An *active* sensor requires an external source of excitation. Resistor-based sensors such as thermistors, RTDs (Resistance Temperature Detectors), and strain gages are examples of active sensors, because a current must be passed through them and the corresponding voltage measured in order to determine the resistance value. An alternative would be to place the devices in a bridge circuit, however in either case, an external current or voltage is required.

On the other hand, *passive* (or *self-generating*) sensors generate their own electrical output signal without requiring external voltages or currents. Examples of passive sensors are thermocouples and photodiodes which generate thermoelectric voltages and photocurrents, respectively, which are independent of external circuits.

It should be noted that these definitions (*active* vs. *passive*) refer to the need (or lack thereof) of external active circuitry to produce the electrical output signal from the sensor. It would seem equally logical to consider a thermocouple to be active in the sense that it produces an output voltage with no external circuitry, however the convention in the industry is to classify the sensor with respect to the external circuit requirement as defined above.

SENSOR OVERVIEW

- **Sensors:**
  Convert a Signal or Stimulus (Representing a Physical Property) into an Electrical Output

- **Transducers:**
  Convert One Type of Energy into Another

- **The Terms are often Interchanged**

- ***Active* Sensors Require an External Source of Excitation:**
  RTDs, Strain-Gages

- ***Passive* (Self-Generating) Sensors do not:**
  Thermocouples, Photodiodes

Figure 1.1

TYPICAL SENSORS AND THEIR OUTPUTS

PROPERTY	SENSOR	ACTIVE/ PASSIVE	OUTPUT
Temperature	Thermocouple	Passive	Voltage
	Silicon	Active	Voltage/Current
	RTD	Active	Resistance
	Thermistor	Active	Resistance
Force / Pressure	Strain Gage	Active	Resistance
	Piezoelectric	Passive	Voltage
Acceleration	Accelerometer	Active	Capacitance
Position	LVDT	Active	AC Voltage
Light Intensity	Photodiode	Passive	Current

Figure 1.2

A logical way to classify sensors is with respect to the physical property the sensor is designed to measure. Thus we have temperature sensors, force sensors, pressure sensors, motion sensors, etc. However, sensors which measure different properties may have the same type of electrical output. For instance, a Resistance Temperature Detector (RTD) is a variable resistance, as is a resistive strain gauge. Both RTDs and strain gages are often placed in bridge circuits, and the conditioning circuits are therefore quite similar. In fact, bridges and their conditioning circuits deserve a detailed discussion.

The full-scale outputs of most sensors (passive or active) are relatively small voltages, currents, or resistance changes, and therefore their outputs must be properly conditioned before further analog or digital processing can occur. Because of this, an entire class of circuits have evolved, generally referred to as *signal conditioning* circuits. Amplification, level translation, galvanic isolation, impedance transformation, linearization, and filtering are fundamental signal conditioning functions which may be required.

Whatever form the conditioning takes, however, the circuitry and performance will be governed by the electrical character of the sensor and its output. Accurate characterization of the sensor in terms of parameters appropriate to the application, e.g., sensitivity, voltage and current levels, linearity, impedances, gain, offset, drift, time constants, maximum electrical ratings, and stray impedances and other important considerations can spell the difference between substandard and successful application of the device, especially in cases where high resolution and precision, or low-level measurements are involved.

Higher levels of integration now allow ICs to play a significant role in both analog and digital signal conditioning. ADCs specifically designed for measurement applications often contain on-chip programmable-gain amplifiers (PGAs) and other useful circuits, such as current sources for driving RTDs, thereby minimizing the external conditioning circuit requirements.

Most sensor outputs are non-linear with respect to the stimulus, and their outputs must be linearized in order to yield correct measurements. Analog techniques may be used to perform this function, however the recent introduction of high performance ADCs now allows linearization to be done much more efficiently and accurately in software and eliminates the need for tedious manual calibration using multiple and sometimes interactive trimpots.

The application of sensors in a typical process control system is shown in Figure 1.3. Assume the physical property to be controlled is the temperature. The output of the temperature sensor is conditioned and then digitized by an ADC. The microcontroller or host computer determines if the temperature is above or below the desired value, and outputs a digital word to the digital-to-analog converter (DAC). The DAC output is conditioned and drives the *actuator*, in this case - a heater. Notice that the interface between the control center and the remote process is via the industry-standard 4-20mA loop.

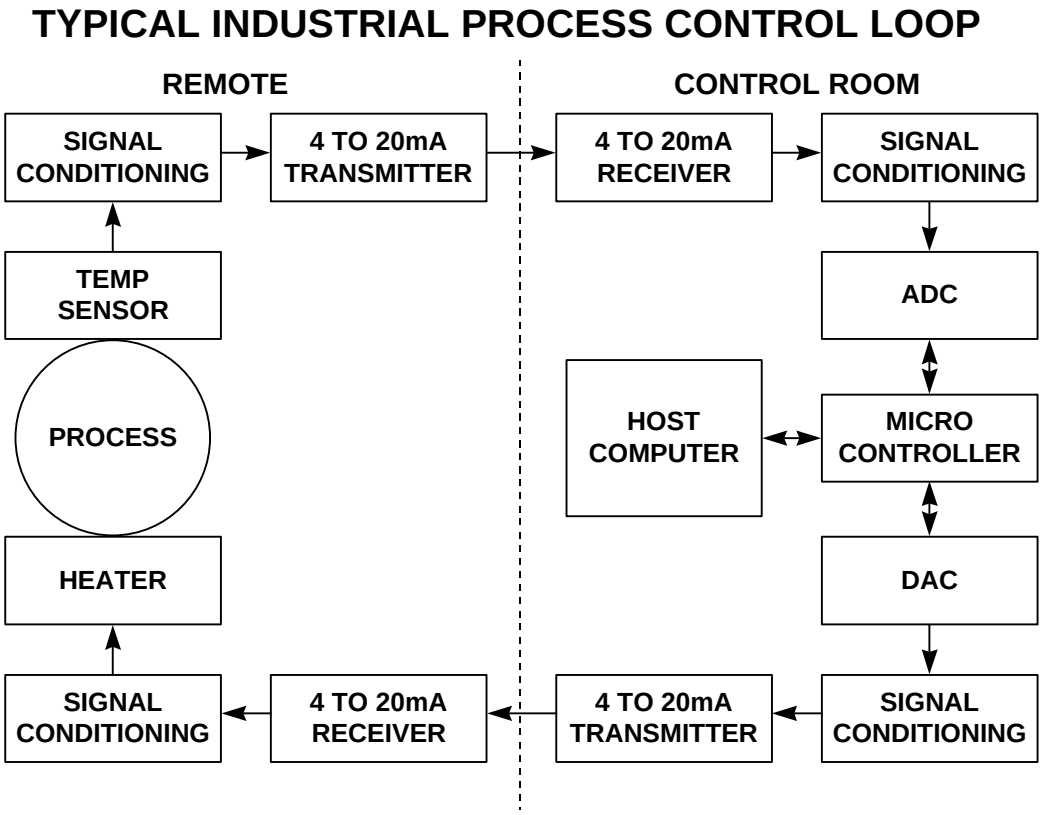


Figure 1.3

Digital techniques are becoming more and more popular in processing sensor outputs in data acquisition, process control, and measurement. 8-bit microcontrollers (8051-based, for example) generally have sufficient speed and processing capability for most applications. By including the A/D conversion and the microcontroller programmability on the sensor itself, a "smart sensor" can be implemented with self contained calibration and linearization features among others. A smart sensor can then interface directly to an industrial network as shown in Figure 1.4.

The basic building blocks of a "smart sensor" are shown in Figure 1.5, constructed with multiple ICs. The Analog Devices MicroConverter™ -series products includes on-chip high performance multiplexers, ADCs, and DACs, coupled with FLASH Memory and an industry-standard 8052 microcontroller core, as well as support circuitry and several standard serial port configurations. These are the first integrated circuits which are truly smart sensor data acquisition systems (high-performance data conversion circuits, microcontroller, FLASH memory) on a single chip (see Figure 1.6).

STANDARDIZATION AT THE DIGITAL INTERFACE USING SMART SENSORS

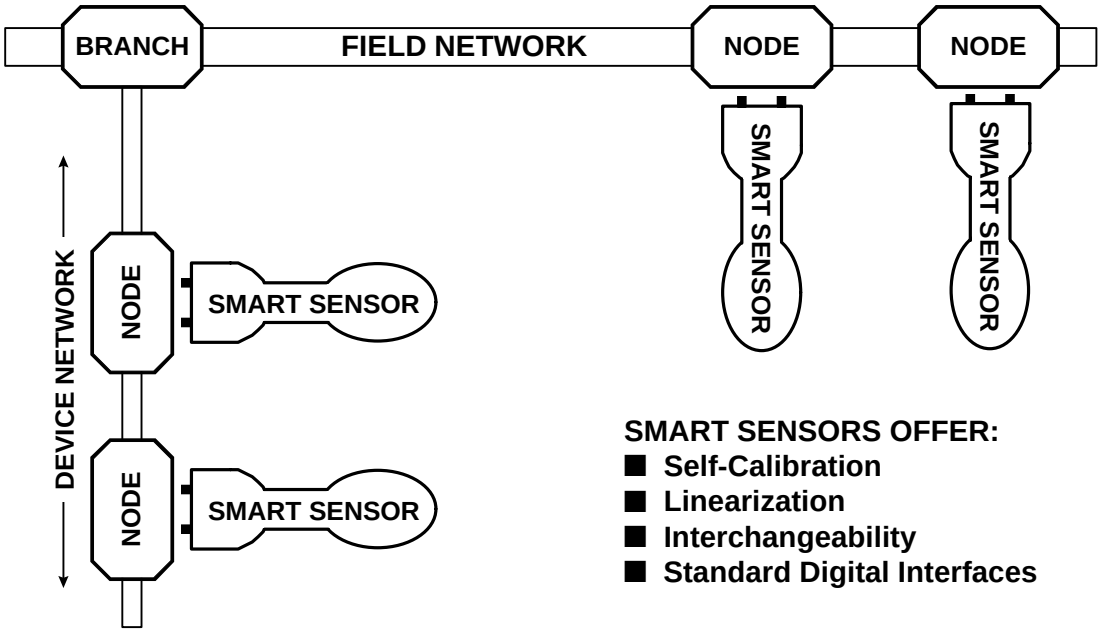


Figure 1.4

BASIC ELEMENTS IN A "SMART" SENSOR

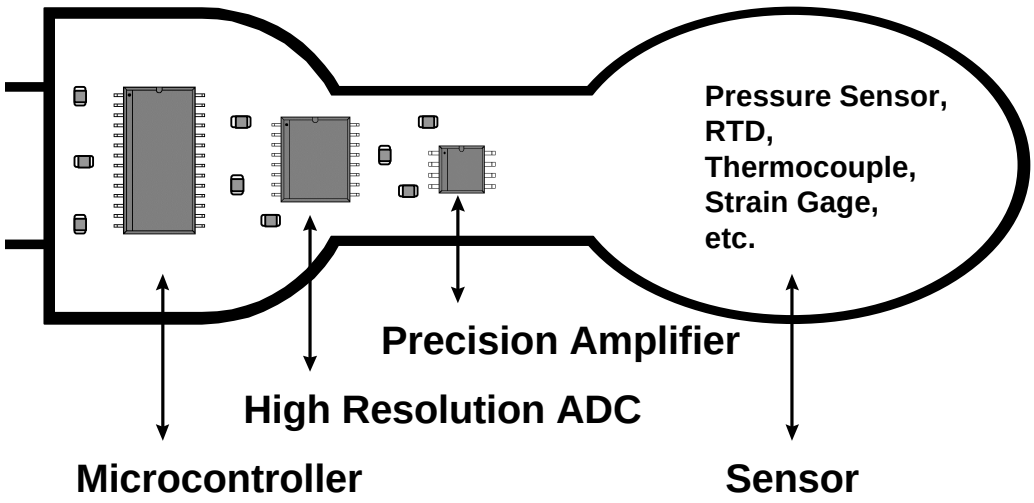


Figure 1.5

THE EVEN SMARTER SENSOR

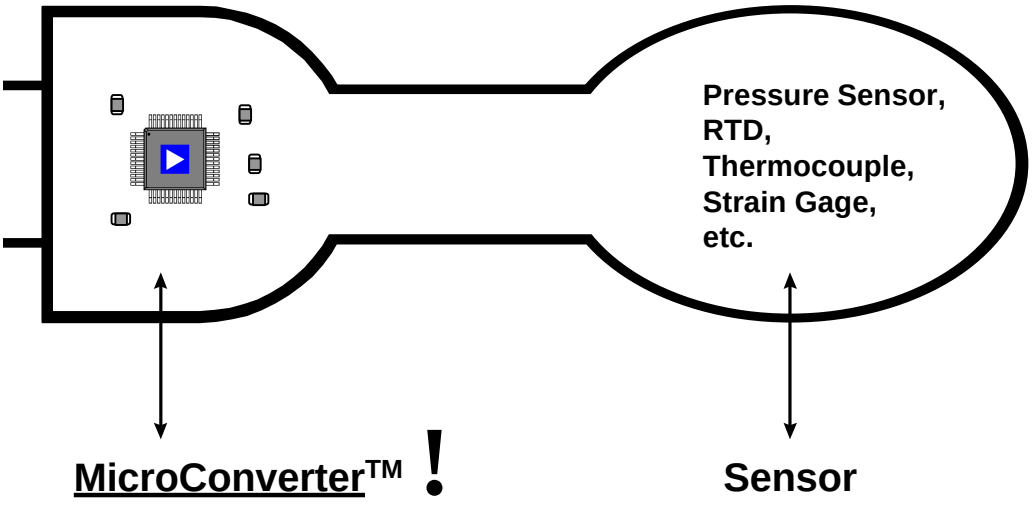


Figure 1.6

SECTION 2
BRIDGE CIRCUITS

Walt Kester

INTRODUCTION

This section discusses the fundamental concepts of bridge circuits, and is followed by a section on precision op amps (Section 3). Section 4 focuses on the detailed application circuits relating to strain gage-based sensors. Sections 2 and 4 can be read sequentially if the reader already understands the design issues relating to op amps which are covered in Section 3.

Resistive elements are some of the most common sensors. They are inexpensive to manufacture and relatively easy to interface with signal conditioning circuits. Resistive elements can be made sensitive to temperature, strain (by pressure or by flex), and light. Using these basic elements, many complex physical phenomena can be measured; such as fluid or mass flow (by sensing the temperature difference between two calibrated resistances) and dew-point humidity (by measuring two different temperature points), etc.

Sensor elements' resistances can range from less than 100Ω to several hundred kΩ, depending on the sensor design and the physical environment to be measured (See Figure 2.1). For example, RTDs (Resistance Temperature Devices) are typically 100Ω or 1000Ω. Thermistors are typically 3500Ω or higher.

RESISTANCE OF POPULAR SENSORS

■ **Strain Gages**	**120Ω, 350Ω, 3500Ω**
■ **Weigh-Scale Load Cells**	**350Ω - 3500Ω**
■ **Pressure Sensors**	**350Ω - 3500Ω**
■ **Relative Humidity**	**100kΩ - 10MΩ**
■ **Resistance Temperature Devices (RTDs)**	**100Ω , 1000Ω**
■ **Thermistors**	**100Ω - 10MΩ**

Figure 2.1

Resistive sensors such as RTDs and strain gages produce small percentage changes in resistance in response to a change in a physical variable such as temperature or force. Platinum RTDs have a temperature coefficient of about 0.385%/°C. Thus, in order to accurately resolve temperature to 1ºC, the measurement accuracy must be much better than 0.385Ω for a 100Ω RTD.

Strain gages present a significant measurement challenge because the typical change in resistance over the entire operating range of a strain gage may be less than 1% of the nominal resistance value. Accurately measuring small resistance changes is therefore critical when applying resistive sensors.

One technique for measuring resistance (shown in Figure 2.2) is to force a constant current through the resistive sensor and measure the voltage output. This requires both an accurate current source and an accurate means of measuring the voltage. Any change in the current will be interpreted as a resistance change. In addition, the power dissipation in the resistive sensor must be small, in accordance with the manufacturer's recommendations, so that self-heating does not produce errors, therefore the drive current must be small.

MEASURING RESISTANCE INDIRECTLY USING A CONSTANT CURRENT SOURCE

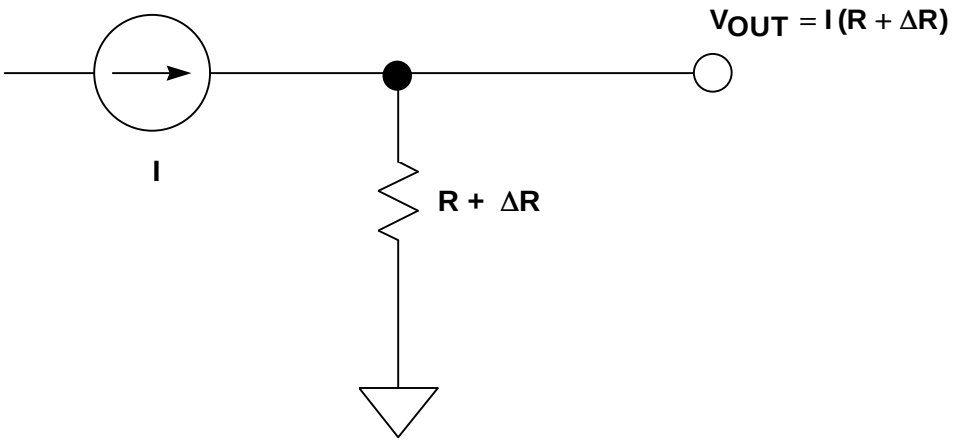
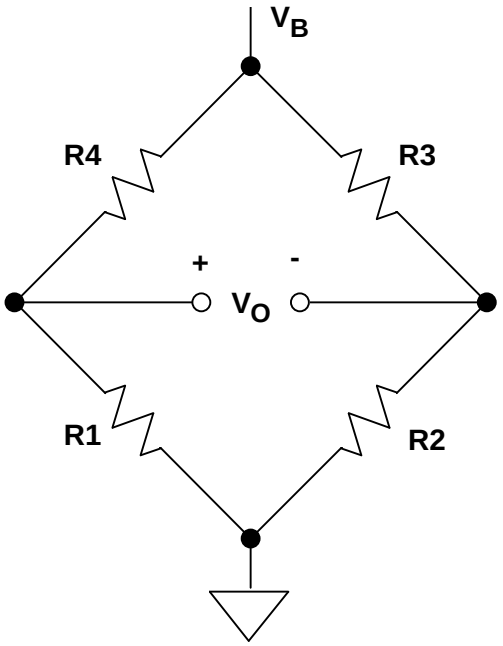


Figure 2.2

Bridges offer an attractive alternative for measuring small resistance changes accurately. The basic Wheatstone bridge (actually developed by S. H. Christie in 1833) is shown in Figure 2.3. It consists of four resistors connected to form a quadrilateral, a source of excitation (voltage or current) connected across one of the diagonals, and a voltage detector connected across the other diagonal. The detector measures the difference between the outputs of two voltage dividers connected across the excitation.

THE WHEATSTONE BRIDGE



$$V_O = \frac{R1}{R1+R4}V_B - \frac{R2}{R2+R3}V_B$$

$$= \frac{\frac{R1}{R4} - \frac{R2}{R3}}{\left(1+\frac{R1}{R4}\right)\left(1+\frac{R2}{R3}\right)}V_B$$

AT BALANCE,

$$V_O = 0 \quad \text{IF} \quad \frac{R1}{R4} = \frac{R2}{R3}$$

Figure 2.3

A bridge measures resistance indirectly by comparison with a similar resistance. The two principle ways of operating a bridge are as a null detector or as a device that reads a difference directly as voltage.

When R1/R4 = R2/R3, the resistance bridge is at a *null*, irrespective of the mode of excitation (current or voltage, AC or DC), the magnitude of excitation, the mode of readout (current or voltage), or the impedance of the detector. Therefore, if the ratio of R2/R3 is fixed at K, a null is achieved when R1 = K·R4. If R1 is unknown and R4 is an accurately determined variable resistance, the magnitude of R1 can be found by adjusting R4 until null is achieved. Conversely, in sensor-type measurements, R4 may be a fixed reference, and a null occurs when the magnitude of the external variable (strain, temperature, etc.) is such that R1 = K·R4.

Null measurements are principally used in feedback systems involving electromechanical and/or human elements. Such systems seek to force the active element (strain gage, RTD, thermistor, etc.) to balance the bridge by influencing the parameter being measured.

For the majority of sensor applications employing bridges, however, the deviation of one or more resistors in a bridge from an initial value is measured as an indication of the magnitude (or a change) in the measured variable. In this case, the output voltage change is an indication of the resistance change. Because very small resistance changes are common, the output voltage change may be as small as tens of millivolts, even with V_B = 10V (a typical excitation voltage for a load cell application).

In many bridge applications, there may be two, or even four elements which vary. Figure 2.4 shows the four commonly used bridges suitable for sensor applications and the corresponding equations which relate the bridge output voltage to the excitation voltage and the bridge resistance values. In this case, we assume a constant voltage drive, V_B. Note that since the bridge output is directly proportional to V_B, the measurement accuracy can be no better than that of the accuracy of the excitation voltage.

OUTPUT VOLTAGE AND LINEARITY ERROR FOR CONSTANT VOLTAGE DRIVE BRIDGE CONFIGURATIONS

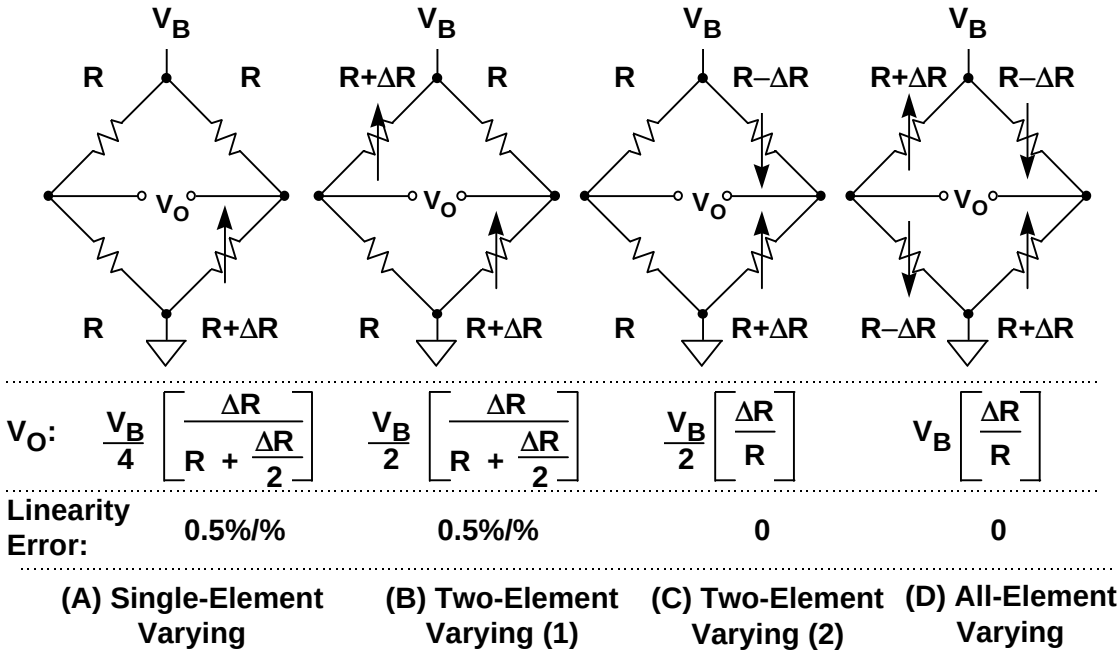


Figure 2.4

In each case, the value of the fixed bridge resistor, R, is chosen to be equal to the nominal value of the variable resistor(s). The deviation of the variable resistor(s) about the nominal value is proportional to the quantity being measured, such as strain (in the case of a strain gage) or temperature (in the case of an RTD).

The *sensitivity* of a bridge is the ratio of the maximum expected change in the output voltage to the excitation voltage. For instance, if V_B = 10V, and the fullscale bridge output is 10mV, then the sensitivity is 1mV/V.

The *single-element varying* bridge is most suited for temperature sensing using RTDs or thermistors. This configuration is also used with a single resistive strain gage. All the resistances are nominally equal, but one of them (the sensor) is variable by an amount ΔR. As the equation indicates, the relationship between the bridge output and ΔR is not linear. For example, if R = 100Ω and ΔR = 0.1Ω (0.1%

change in resistance), the output of the bridge is 2.49875mV for V_B = 10V. The error is 2.50000mV – 2.49875mV, or 0.00125mV. Converting this to a % of fullscale by dividing by 2.5mV yields an end-point linearity error in percent of approximately 0.05%. (Bridge end-point linearity error is calculated as the worst error in % FS from a straight line which connects the origin and the end point at FS, i.e. the FS gain error is not included). If $\Delta R = 1\Omega$, (1% change in resistance), the output of the bridge is 24.8756mV, representing an end-point linearity error of approximately 0.5%. The end-point linearity error of the single-element bridge can be expressed in equation form:

Single-Element Varying
Bridge End-Point Linearity Error $\approx$ % Change in Resistance $\div$ 2

It should be noted that the above nonlinearity refers to the nonlinearity of the bridge itself and not the sensor. In practice, most sensors exhibit a certain amount of their own nonlinearity which must be accounted for in the final measurement.

In some applications, the bridge nonlinearity may be acceptable, but there are various methods available to linearize bridges. Since there is a fixed relationship between the bridge resistance change and its output (shown in the equations), software can be used to remove the linearity error in digital systems. Circuit techniques can also be used to linearize the bridge output directly, and these will be discussed shortly.

There are two possibilities to consider in the case of the two-element varying bridge. In the first, Case (1), both elements change in the same direction, such as two identical strain gages mounted adjacent to each other with their axes in parallel.

The nonlinearity is the same as that of the single-element varying bridge, however the gain is twice that of the single-element varying bridge. The two-element varying bridge is commonly found in pressure sensors and flow meter systems.

A second configuration of the two-element varying bridge, Case (2), requires two identical elements that vary in *opposite* directions. This could correspond to two identical strain gages: one mounted on top of a flexing surface, and one on the bottom. Note that this configuration is linear, and like two-element Case (1), has twice the gain of the single-element configuration. Another way to view this configuration is to consider the terms $R+\Delta R$ and $R-\Delta R$ as comprising the two sections of a center-tapped potentiometer.

The *all-element varying* bridge produces the most signal for a given resistance change and is inherently linear. It is an industry-standard configuration for load cells which are constructed from four identical strain gages.

Bridges may also be driven from constant current sources as shown in Figure 2.5. Current drive, although not as popular as voltage drive, has an advantage when the bridge is located remotely from the source of excitation because the wiring resistance does not introduce errors in the measurement. Note also that with constant current excitation, all configurations are linear with the exception of the single-element varying case.

OUTPUT VOLTAGE AND LINEARITY ERROR FOR CONSTANT CURRENT DRIVE BRIDGE CONFIGURATIONS

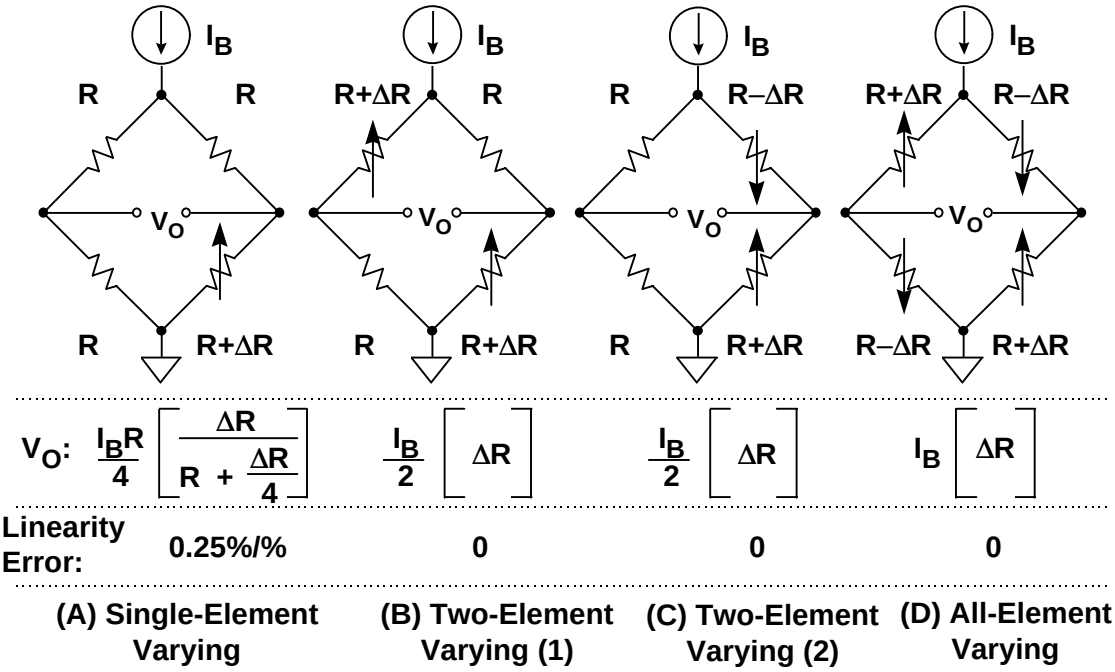


Figure 2.5

In summary, there are many design issues relating to bridge circuits. After selecting the basic configuration, the excitation method must be determined. The value of the excitation voltage or current must first be determined. Recall that the fullscale bridge output is directly proportional to the excitation voltage (or current). Typical bridge sensitivites are 1mV/V to 10mV/V. Although large excitation voltages yield proportionally larger fullscale output voltages, they also result in higher power dissipation and the possibility of sensor resistor self-heating errors. On the other hand, low values of excitation voltage require more gain in the conditioning circuits and increase the sensitivity to noise.

Regardless of its value, the stability of the excitation voltage or current directly affects the overall accuracy of the bridge output. Stable references and/or ratiometric techniques are required to maintain desired accuracy.

BRIDGE CONSIDERATIONS

- Selecting Configuration (1, 2, 4 - Element Varying)
- Selection of Voltage or Current Excitation
- Stability of Excitation Voltage or Current
- Bridge Sensitivity: FS Output / Excitation Voltage
  1mV / V to 10mV / V Typical
- Fullscale Bridge Outputs: 10mV - 100mV Typical
- Precision, Low Noise Amplification / Conditioning
  Techniques Required
- Linearization Techniques May Be Required
- Remote Sensors Present Challenges

Figure 2.6

AMPLIFYING AND LINEARIZING BRIDGE OUTPUTS

The output of a single-element varying bridge may be amplified by a single precision op-amp connected in the inverting mode as shown in Figure 2.7. This circuit, although simple, has poor gain accuracy and also unbalances the bridge due to loading from R_F and the op amp bias current. The R_F resistors must be carefully chosen and matched to maximize the common mode rejection (CMR). Also it is difficult to maximize the CMR while at the same time allowing different gain options. In addition, the output is nonlinear. The key redeeming feature of the circuit is that it is capable of single supply operation and requires a single op amp. Note that the R_F resistor connected to the non-inverting input is returned to $V_S/2$ (rather than ground) so that both positive and negative values of ΔR can be accommodated, and the op amp output is referenced to $V_S/2$.

A much better approach is to use an instrumentation amplifier (in-amp) as shown in Figure 2.8. This efficient circuit provides better gain accuracy (usually set with a single resistor, R_G) and does not unbalance the bridge. Excellent common mode rejection can be achieved with modern in-amps. Due to the bridge's intrinsic characteristics, the output is nonlinear, but this can be corrected in the software (assuming that the in-amp output is digitized using an analog-to-digital converter and followed by a microcontroller or microprocessor). Instrumentation amplifiers such as the AD620, AD623, and AD627 can be used in single supply applications provided the restrictions on the gain and input and output voltage swings are observed. (For a detailed discussion of these important considerations, see Section 3).

USING A SINGLE OP AMP AS A BRIDGE AMPLIFIER FOR A SINGLE-ELEMENT VARYING BRIDGE

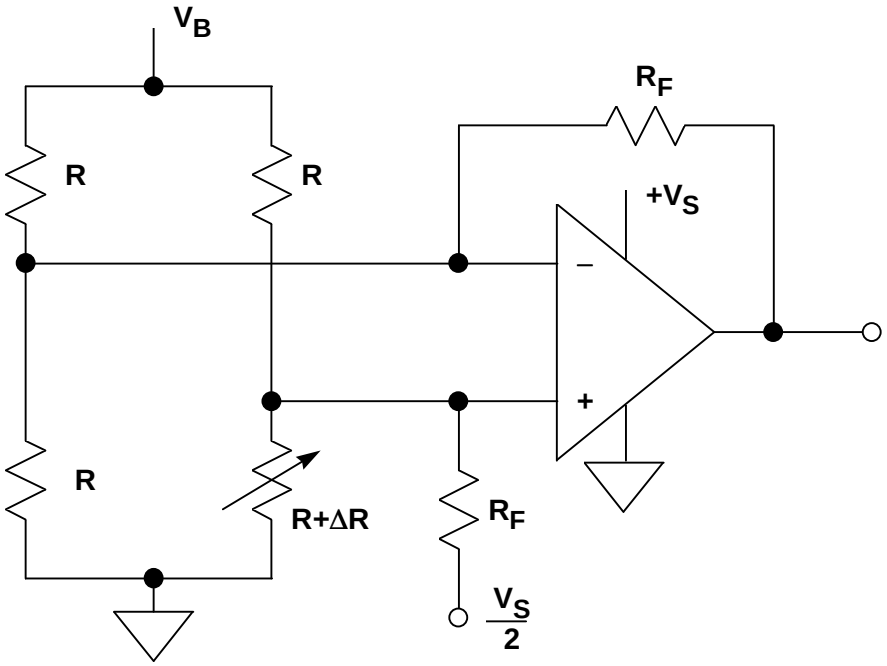


Figure 2.7

USING AN INSTRUMENTATION AMPLIFIER WITH A SINGLE-ELEMENT VARYING BRIDGE

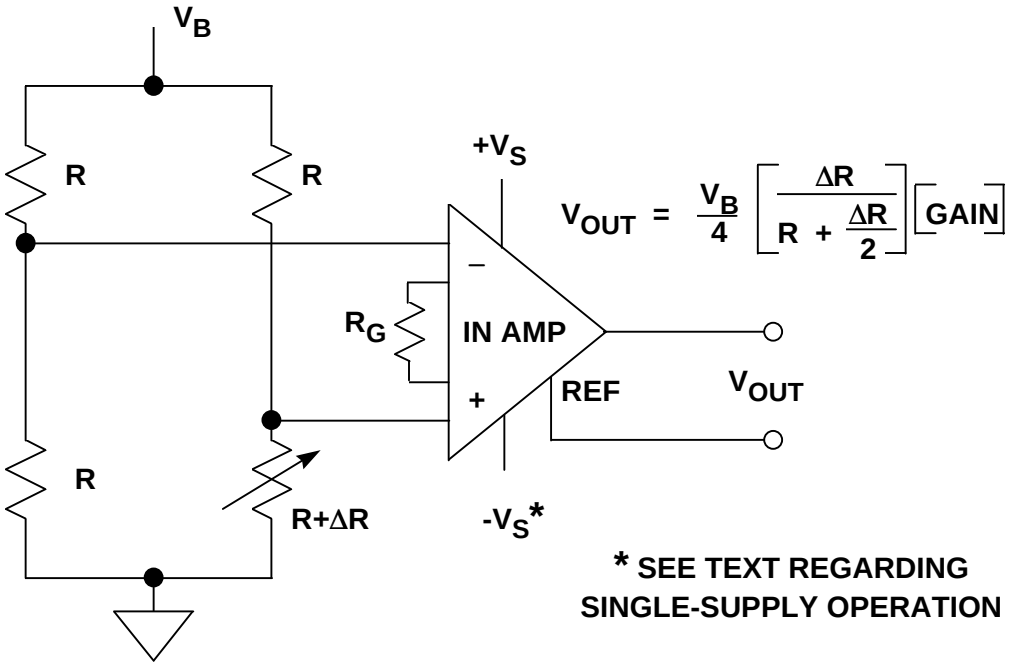


Figure 2.8

Various techniques are available to linearize bridges, but it is important to distinguish between the linearity of the bridge equation and the linearity of the sensor response to the phenomenon being sensed. For example, if the active element is an RTD, the bridge used to implement the measurement might have perfectly adequate linearity; yet the output could still be nonlinear due to the RTD's nonlinearity. Manufacturers of sensors employing bridges address the nonlinearity issue in a variety of ways, including keeping the resistive swings in the bridge small, shaping complimentary nonlinear response into the active elements of the bridge, using resistive trims for first-order corrections, and others.

Figure 2.9 shows a single-element varying active bridge in which an op amp produces a forced null, by adding a voltage in series with the variable arm. That voltage is equal in magnitude and opposite in polarity to the incremental voltage across the varying element and is linear with ΔR. Since it is an op amp output, it can be used as a low impedance output point for the bridge measurement. This active bridge has a gain of two over the standard single-element varying bridge, and the output is linear, even for large values of ΔR. Because of the small output signal, this bridge must usually be followed by an second amplifier. The amplifier used in this circuit requires dual supplies because its output must go negative.

LINEARIZING A SINGLE-ELEMENT VARYING BRIDGE METHOD 1

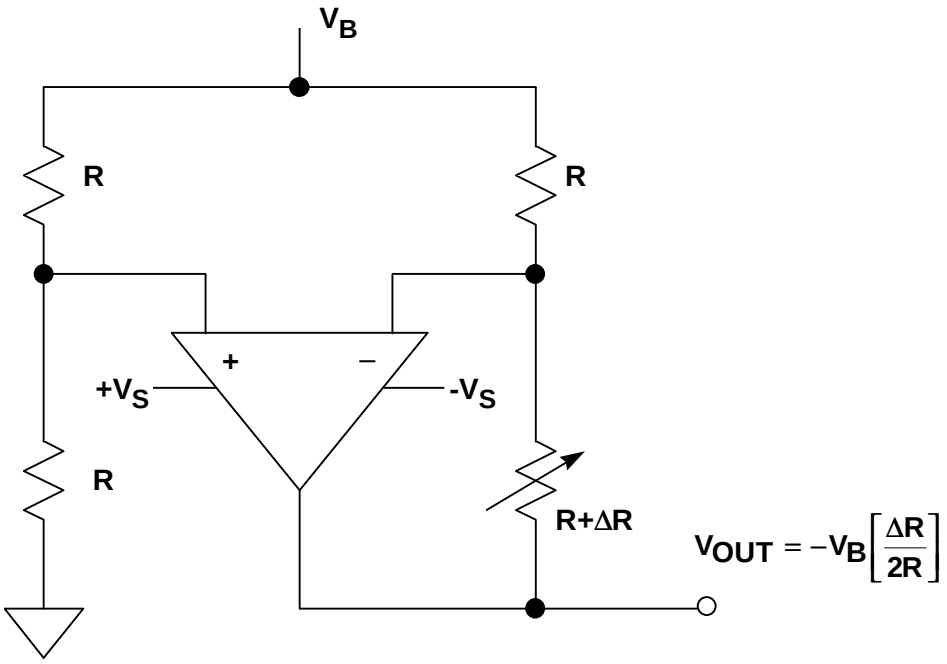


Figure 2.9

Another circuit for linearizing a single-element varying bridge is shown in Figure 2.10. The bottom of the bridge is driven by an op amp, which maintains a constant current in the varying resistance element. The output signal is taken from the right-hand leg of the bridge and amplified by a non-inverting op amp. The output is linear, but the circuit requires two op amps which must operate on dual supplies. In addition, R1 and R2 must be matched for accurate gain.

LINEARIZING A SINGLE-ELEMENT VARYING BRIDGE METHOD 2

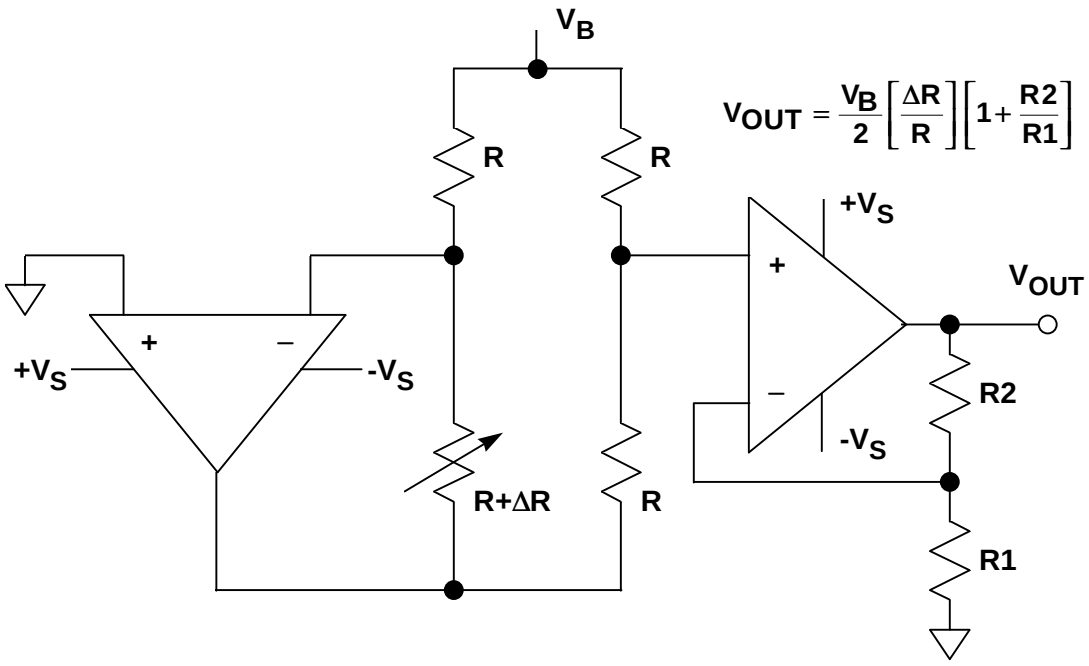


Figure 2.10

A circuit for linearizing a voltage-driven two-element varying bridge is shown in Figure 2.11. This circuit is similar to Figure 2.9 and has twice the sensitivity. A dual supply op amp is required. Additional gain may be necessary.

LINEARIZING A TWO-ELEMENT VARYING BRIDGE METHOD 1 (CONSTANT VOLTAGE DRIVE)

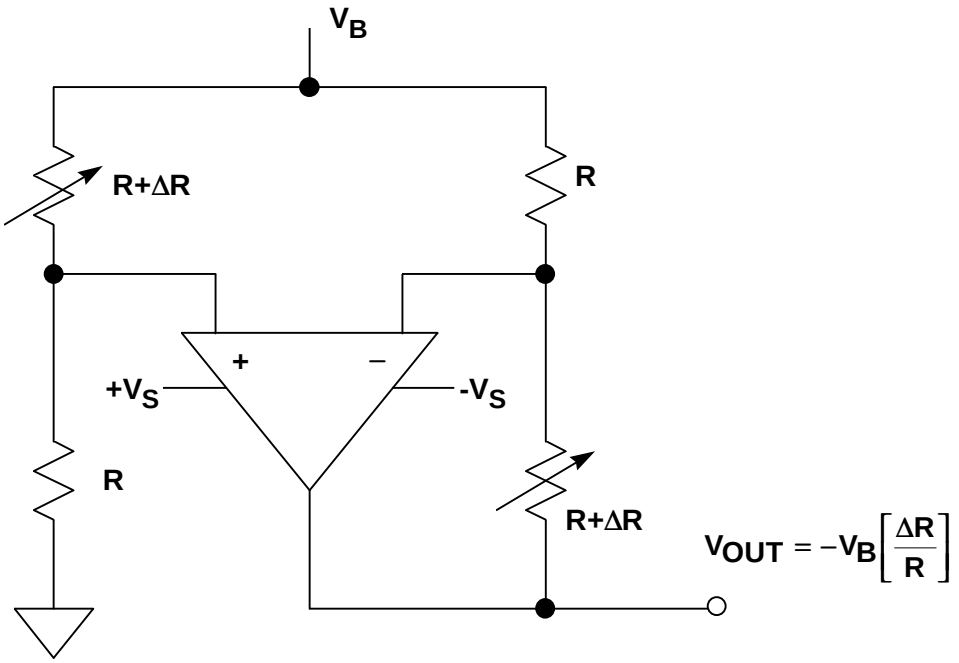


Figure 2.11

The two-element varying bridge circuit in Figure 2.12 uses an op amp, a sense resistor, and a voltage reference to maintain a constant current through the bridge ($I_B = V_{REF}/R_{SENSE}$). The current through each leg of the bridge remains constant ($I_B/2$) as the resistances change, therefore the output is a linear function of ΔR. An instrumentation amplifier provides the additional gain. This circuit can be operated on a single supply with the proper choice of amplifiers and signal levels.

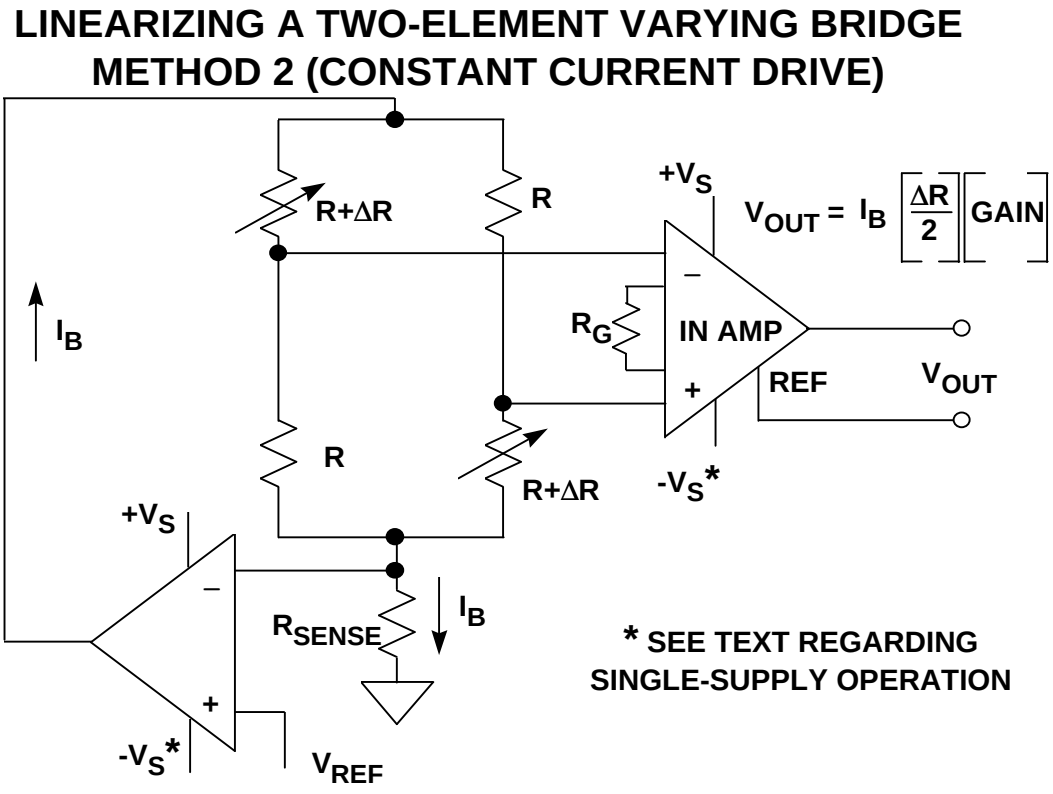


Figure 2.12

DRIVING BRIDGES

Wiring resistance and noise pickup are the biggest problems associated with remotely located bridges. Figure 2.13 shows a 350Ω strain gage which is connected to the rest of the bridge circuit by 100 feet of 30 gage twisted pair copper wire. The resistance of the wire at 25ºC is 0.105Ω/ft, or 10.5Ω for 100ft. The total lead resistance in series with the 350Ω strain gage is therefore 21Ω. The temperature coefficient of the copper wire is 0.385%/ºC. Now we will calculate the gain and offset error in the bridge output due to a +10ºC temperature rise in the cable. These calculations are easy to make, because the bridge output voltage is simply the difference between the output of two voltage dividers, each driven from a +10V source.

ERRORS PRODUCED BY WIRING RESISTANCE FOR REMOTE RESISTIVE BRIDGE SENSOR

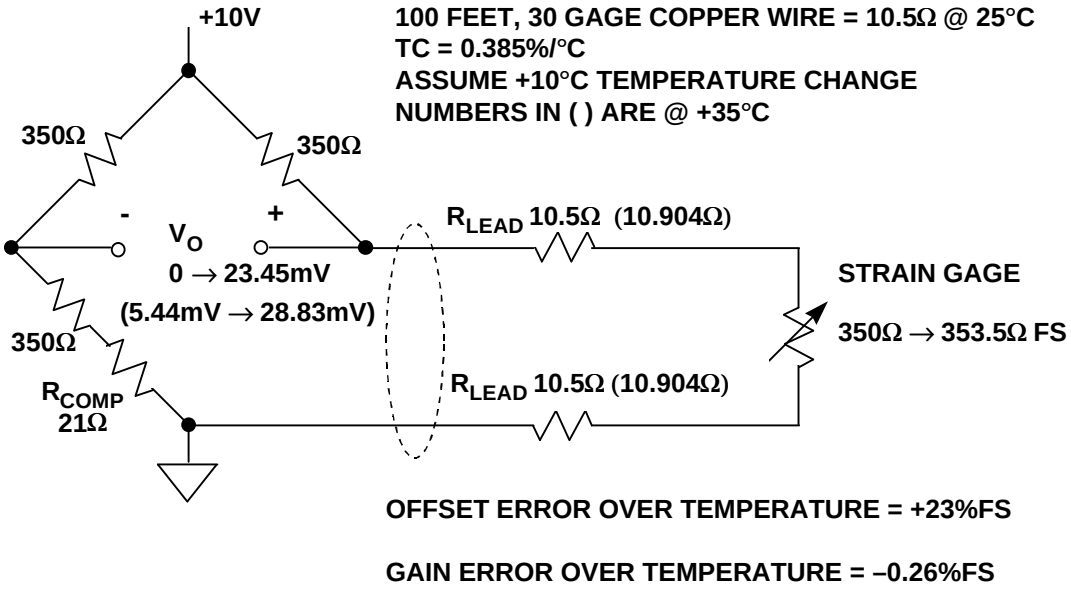


Figure 2.13

The fullscale variation of the strain gage resistance (with flex) above its nominal 350Ω value is +1% (+3.5Ω), corresponding to a fullscale strain gage resistance of 353.5Ω which causes a bridge output voltage of +23.45mV. Notice that the addition of the 21Ω R_{COMP} resistor compensates for the wiring resistance and balances the bridge when the strain gage resistance is 350Ω. Without R_{COMP}, the bridge would have an output offset voltage of 145.63mV for a nominal strain gage resistance of 350Ω. This offset could be compensated for in software just as easily, but for this example, we chose to do it with R_{COMP}.

Assume that the cable temperature increases +10ºC above nominal room temperature. This results in a total lead resistance increase of +0.404Ω (10.5Ω×0.00385/ºC×10ºC) in each lead. *Note: The values in parentheses in the diagram indicate the values at +35ºC.* The total additional lead resistance (of the two leads) is +0.808Ω. With no strain, this additional lead resistance produces an offset of +5.44mV in the bridge output. Fullscale strain produces a bridge output of +28.83mV (a change of +23.39mV from no strain). Thus the increase in temperature produces an offset voltage error of +5.44mV (+23% fullscale) and a gain error of –0.06mV (23.39mV – 23.45mV), or –0.26% fullscale. Note that these errors are produced solely by the 30 gage wire, and do not include any temperature coefficient errors in the strain gage itself.

The effects of wiring resistance on the bridge output can be minimized by the 3-wire connection shown in Figure 2.14. We assume that the bridge output voltage is measured by a high impedance device, therefore there is no current in the sense lead. Note that the sense lead measures the voltage output of a divider: the top half is the bridge resistor plus the lead resistance, and the bottom half is strain gage resistance plus the lead resistance. The nominal sense voltage is therefore

independent of the lead resistance. When the strain gage resistance increases to fullscale (353.5Ω), the bridge output increases to +24.15mV.

Increasing the temperature to +35ºC increases the lead resistance by +0.404Ω in each half of the divider. The fullscale bridge output voltage decreases to +24.13mV because of the small loss in sensitivity, but there is no offset error. The gain error due to the temperature increase of +10ºC is therefore only –0.02mV, or –0.08% of fullscale. Compare this to the +23% fullscale offset error and the –0.26% gain error for the two-wire connection shown in Figure 2.13.

3-WIRE CONNECTION TO REMOTE BRIDGE ELEMENT (SINGLE-ELEMENT VARYING)

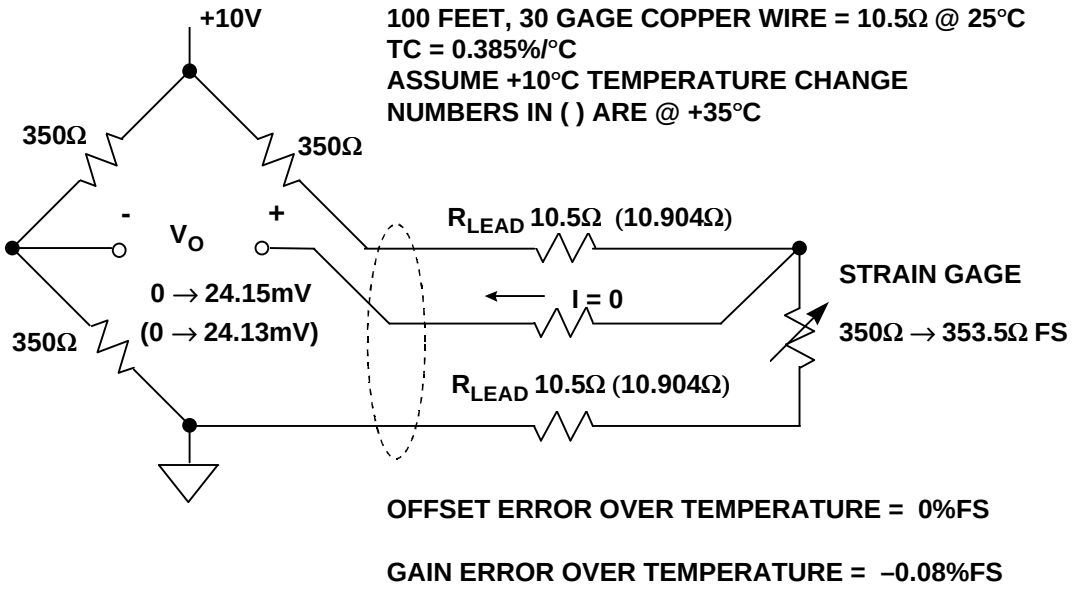


Figure 2.14

The three-wire method works well for remotely located resistive elements which make up one leg of a single-element varying bridge. However, all-element varying bridges generally are housed in a complete assembly, as in the case of a load cell. When these bridges are remotely located from the conditioning electronics, special techniques must be used to maintain accuracy.

Of particular concern is maintaining the accuracy and stability of the bridge excitation voltage. The bridge output is directly proportional to the excitation voltage, and any drift in the excitation voltage produces a corresponding drift in the output voltage.

For this reason, most all-element varying bridges (such as load cells) are six-lead assemblies: two leads for the bridge output, two leads for the bridge excitation, and two *sense* leads. This method (called Kelvin or 4-wire sensing) is shown in Figure 2.15. The sense lines go to high impedance op amp inputs, thus there is minimal error due to the bias current induced voltage drop across their lead resistance. The op amps maintain the required excitation voltage to make the voltage measured between the sense leads always equal to V_B. Although Kelvin sensing eliminates

errors due to voltage drops in the wiring resistance, the drive voltages must still be highly stable since they directly affect the bridge output voltage. In addition, the op amps must have low offset, low drift, and low noise.

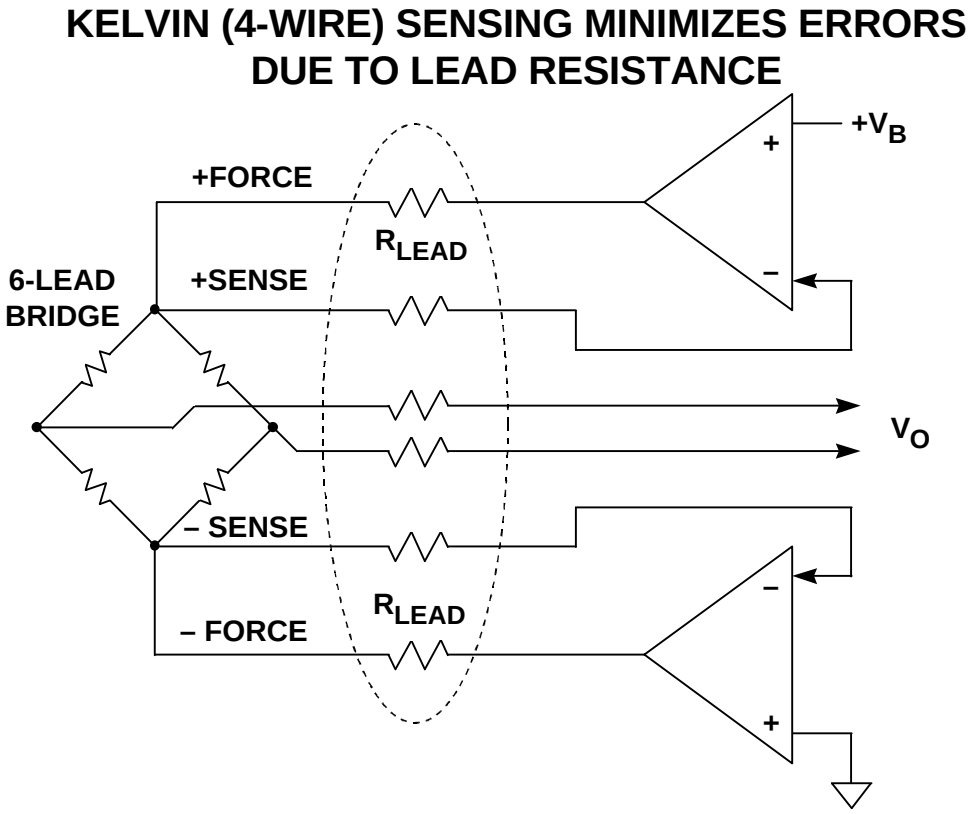


Figure 2.15

The constant current excitation method shown in Figure 2.16 is another method for minimizing the effects of wiring resistance on the measurement accuracy. However, the accuracy of the reference, the sense resistor, and the op amp all influence the overall accuracy.

A very powerful *ratiometric* technique which includes Kelvin sensing to minimize errors due to wiring resistance and also eliminates the need for an accurate excitation voltage is shown in Figure 2.17. The AD7730 measurement ADC can be driven from a single supply voltage which is also used to excite the remote bridge. Both the analog input and the reference input to the ADC are high impedance and fully differential. By using the + and – SENSE outputs from the bridge as the differential reference to the ADC, there is no loss in measurement accuracy if the actual bridge excitation voltage varies. The AD7730 is one of a family of sigma-delta ADCs with high resolution (24 bits) and internal programmable gain amplifiers (PGAs) and is ideally suited for bridge applications. These ADCs have self- and system calibration features which allow offset and gain errors due to the ADC to be minimized. For instance, the AD7730 has an offset drift of 5nV/ºC and a gain drift of 2ppm/ºC. Offset and gain errors can be reduced to a few microvolts using the system calibration feature. (A more detailed discussion of these ADCs can be found in Section 8).

CONSTANT CURRENT EXCITATION MINIMIZES WIRING RESISTANCE ERRORS

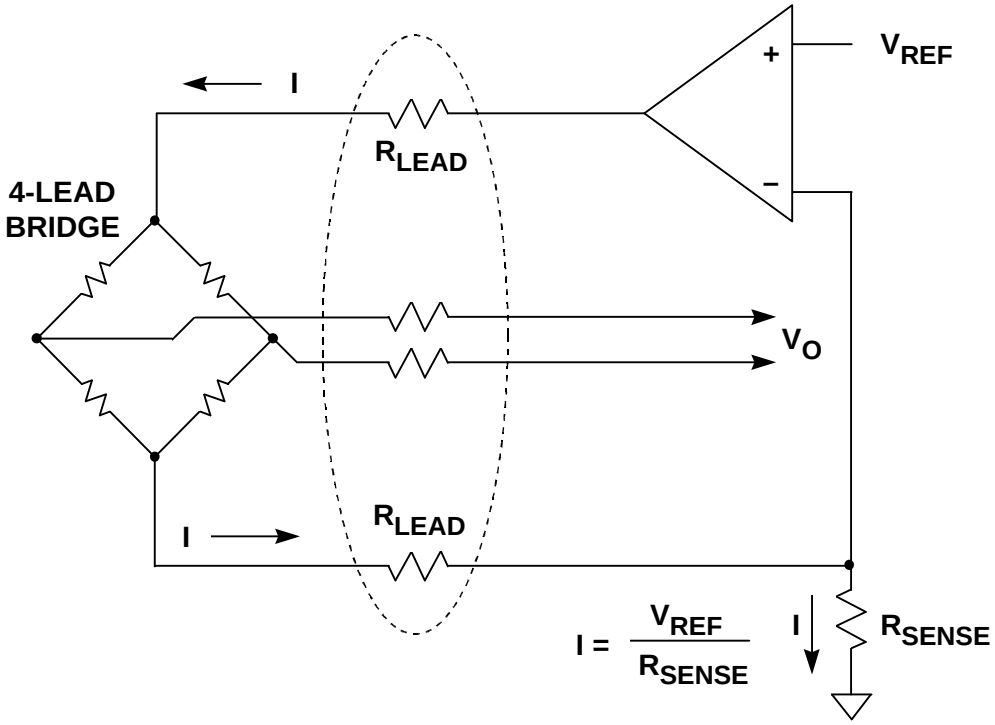


Figure 2.16

DRIVING REMOTE BRIDGE USING KELVIN (4-WIRE) SENSING AND RATIOMETRIC CONNECTION TO ADC

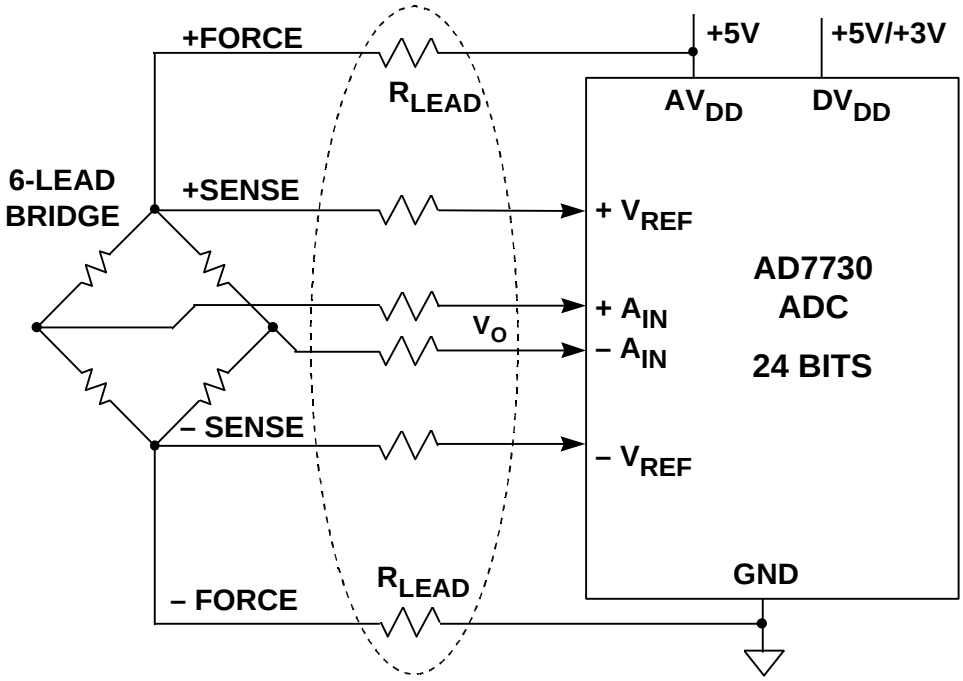


Figure 2.17

Maintaining an accuracy of 0.1% or better with a fullscale bridge output voltage of 20mV requires that the sum of all offset errors be less than 20µV. Figure 2.18 shows some typical sources of offset error that are inevitable in a system. Parasitic thermocouples whose junctions are at different temperatures can generate voltages between a few and tens of microvolts for a 1ºC temperature differential. The diagram shows a typical parasitic junction formed between the copper printed circuit board traces and the kovar pins of the IC amplifier. This thermocouple voltage is about 35µV/ºC temperature differential. The thermocouple voltage is significantly less when using a plastic package with a copper lead frame.

The amplifier offset voltage and bias current are other sources of offset error. The amplifier bias current must flow through the source impedance. Any unbalance in either the source resistances or the bias currents produce offset errors. In addition, the offset voltage and bias currents are a function of temperature. High performance low offset, low offset drift, low bias current, and low noise precision amplifiers such as the OP177 or AD707 are required. In some cases, chopper-stabilized amplifiers such as the AD8551/AD8552/AD8554 may be the only solution.

TYPICAL SOURCES OF OFFSET VOLTAGE

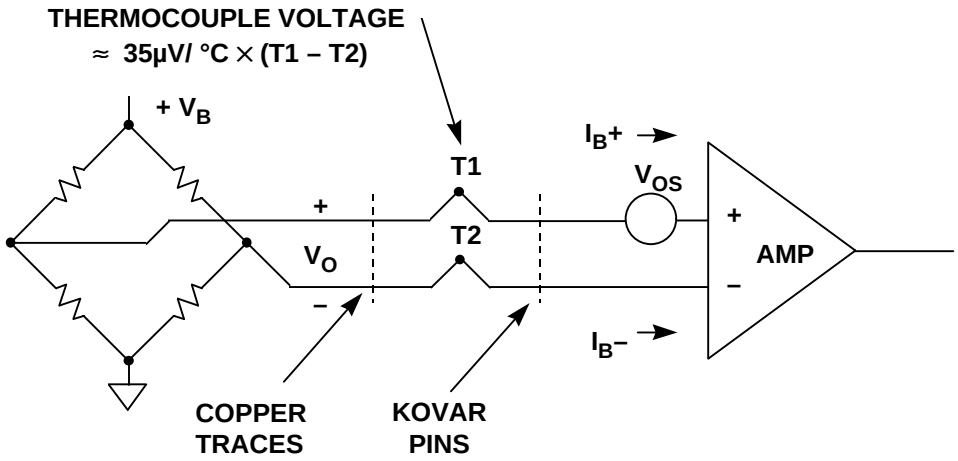


Figure 2.18

AC bridge excitation as shown in Figure 2.19 can effectively remove offset voltages in series with the bridge output. The concept is simple. The net bridge output voltage is measured under two conditions as shown. The first measurement yields a measurement V_A, where V_A is the sum of the desired bridge output voltage V_O and the net offset error voltage E_{OS}. The polarity of the bridge excitation is reversed, and a second measurement V_B is made. Subtracting V_B from V_A yields $2V_O$, and the offset error term E_{OS} cancels as shown.

Obviously, this technique requires a highly accurate measurement ADC (such as the AD7730) as well as a microcontroller to perform the subtraction. If a ratiometric reference is desired, the ADC must also accommodate the changing polarity of the reference voltage. Again, the AD7730 includes this capability.

AC EXCITATION MINIMIZES OFFSET ERRORS

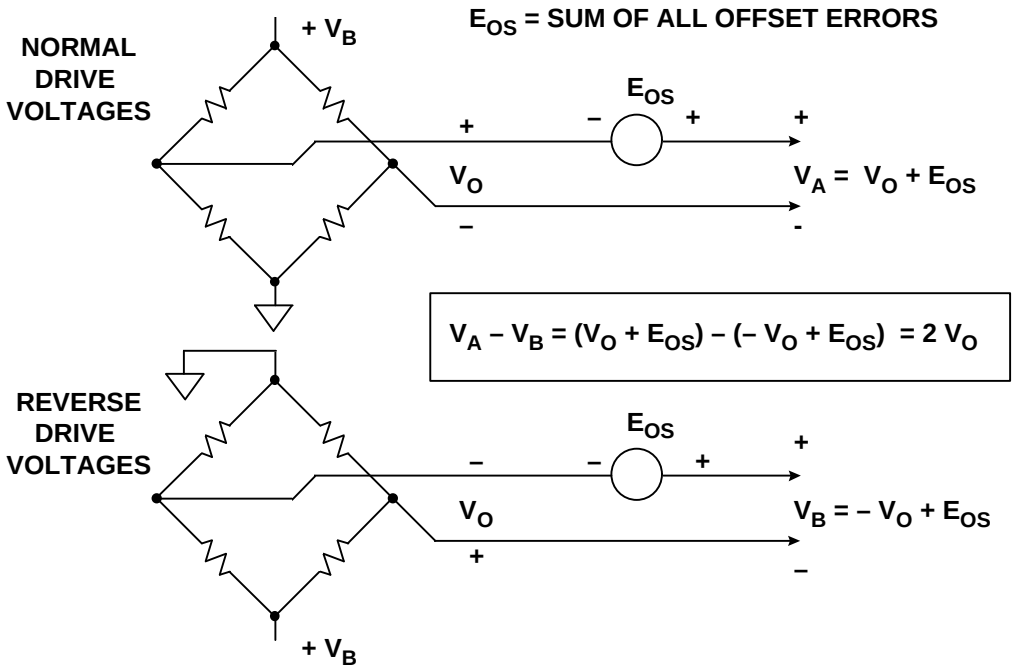


Figure 2.19

P-Channel and N-Channel MOSFETs can be configured as an AC bridge driver as shown in Figure 2.20. Dedicated bridge driver chips are also available, such as the Micrel MIC4427. Note that because of the on-resistance of the MOSFETs, Kelvin sensing must be used in these applications. It is also important that the drive signals be non-overlapping to prevent excessive MOSFET switching currents. The AD7730 ADC has on chip circuitry to generate the required non-overlapping drive signals for AC excitation.

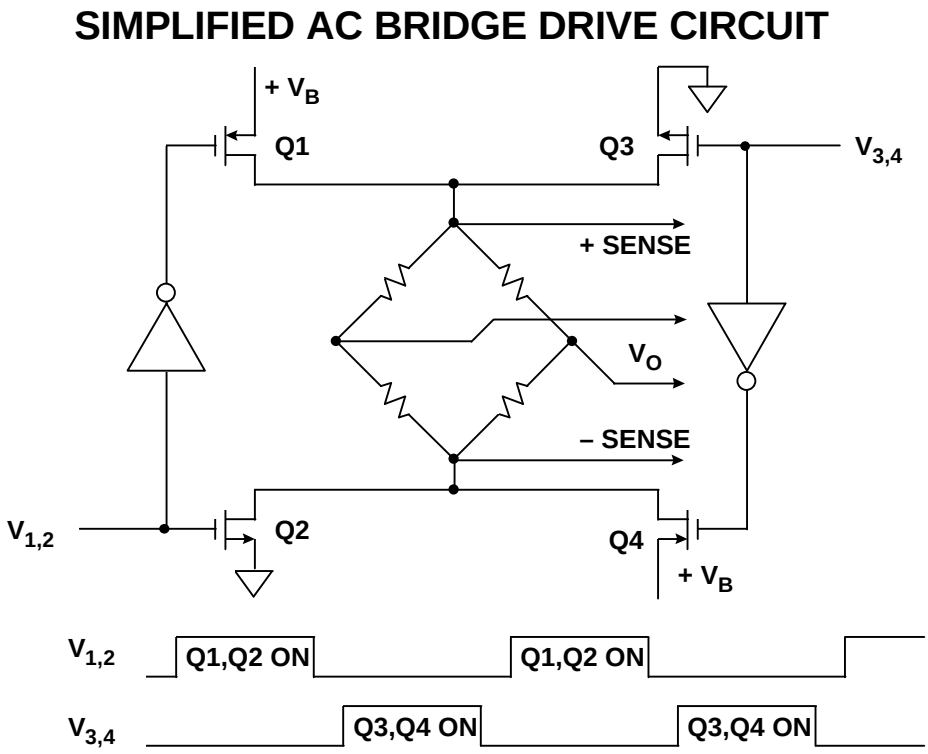

SIMPLIFIED AC BRIDGE DRIVE CIRCUIT
+ V_B
Q1
Q3
$V_{3,4}$
+ SENSE
V_O
– SENSE
$V_{1,2}$
Q2
Q4
+ V_B
$V_{1,2}$
Q1,Q2 ON
Q1,Q2 ON
$V_{3,4}$
Q3,Q4 ON
Q3,Q4 ON

Figure 2.20

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1. Ramon Pallas-Areny and John G. Webster, **Sensors and Signal Conditionin**g, John Wiley, New York, 1991.

2. Dan Sheingold, Editor, **Transducer Interfacing Handbook**, Analog Devices, Inc., 1980.

3. Walt Kester, Editor, **1992 Amplifier Applications Guide**, Section 2, 3, Analog Devices, Inc., 1992.

4. Walt Kester, Editor, **System Applications Guide**, Section 1, 6, Analog Devices, Inc., 1993.

5. AD7730 Data Sheet, Analog Devices, available at http://www.analog.com.

SECTION 3
AMPLIFIERS FOR SIGNAL CONDITIONING

Walt Kester, James Bryant, Walt Jung

INTRODUCTION

This section examines the critical parameters of amplifiers for use in precision signal conditioning applications. Offset voltages for precision IC op amps can be as low as 10µV with corresponding temperature drifts of 0.1µV/ºC. Chopper stabilized op amps provide offsets and offset voltage drifts which cannot be distinguished from noise. Open loop gains greater than 1 million are common, along with common mode and power supply rejection ratios of the same magnitude. Applying these precision amplifiers while maintaining the amplifier performance can present significant challenges to a design engineer, i.e., external passive component selection and PC board layout.

It is important to understand that DC open-loop gain, offset voltage, power supply rejection (PSR), and common mode rejection (CMR) alone should not be the only considerations in selecting precision amplifiers. The AC performance of the amplifier is also important, even at "low" frequencies. Open-loop gain, PSR, and CMR all have relatively low corner frequencies, and therefore what may be considered "low" frequency may actually fall above these corner frequencies, increasing errors above the value predicted solely by the DC parameters. For example, an amplifier having a DC open-loop gain of 10 million and a unity-gain crossover frequency of 1MHz has a corresponding corner frequency of 0.1Hz! One must therefore consider the open loop gain at the actual *signal* frequency. The relationship between the single-pole unity-gain crossover frequency, f_u, the signal frequency, f_{sig}, and the open-loop gain $A_{VOL(fsig)}$ (measured at the signal frequency is given by:

$$A_{VOL(f_{sig})} = \frac{f_u}{f_{sig}}.$$

It the example above, the open loop gain is 10 at 100kHz, and 100,000 at 10Hz.

Loss of open loop gain at the frequency of interest can introduce distortion, especially at audio frequencies. Loss of CMR or PSR at the line frequency or harmonics thereof can also introduce errors.

The challenge of selecting the right amplifier for a particular signal conditioning application has been complicated by the sheer proliferation of various types of amplifiers in various processes (Bipolar, Complementary Bipolar, BiFET, CMOS, BiCMOS, etc.) and architectures (traditional op amps, instrumentation amplifiers, chopper amplifiers, isolation amplifiers, etc.) In addition, a wide selection of precision amplifiers are now available which operate on single supply voltages which complicates the design process even further because of the reduced signal swings and voltage input and output restrictions. Offset voltage and noise are now a more significant portion of the input signal. Selection guides and parametric search engines which can simplify this process somewhat are available on the world-wide-web (http://www.analog.com) as well as on CDROM.

In this section, we will first look at some key performance specifications for precision op amps. Other amplifiers will then be examined such as instrumentation amplifiers, chopper amplifiers, and isolation amplifiers. The implications of single supply operation will be discussed in detail because of their significance in today's designs, which often operate from batteries or other low power sources.

AMPLIFIERS FOR SIGNAL CONDITIONING

- **Input Offset Voltage** **<100µV**
- **Input Offset Voltage Drift** **<1µV/°C**
- **Input Bias Current** **<2nA**
- **Input Offset Current** **<2nA**
- **DC Open Loop Gain** **>1,000,000**
- **Unity Gain Bandwidth Product, f_u** **500kHz - 5MHz**
- **Always Check Open Loop Gain at Signal Frequency!**
- **1/f (0.1Hz to 10Hz) Noise** **<1µV p-p**
- **Wideband Noise** **<10nV/√Hz**
- **CMR, PSR** **>100dB**
    - **Single Supply Operation**
    - **Power Dissipation**

Figure 3.1

PRECISION OP AMP CHARACTERISTICS

Input Offset Voltage

Input offset voltage error is usually one of the largest error sources for precision amplifier circuit designs. However, it is a systemic error and can usually be dealt with by using a manual offset null trim or by system calibration techniques using a microcontroller or microprocessor. Both solutions carry a cost penalty, and today's precision op amps offer initial offset voltages as low as 10µV for bipolar devices, and far less for chopper stabilized amplifiers. With low offset amplifiers, it is possible to eliminate the need for manual trims or system calibration routines.

Measuring input offset voltages of a few microvolts requires that the test circuit does not introduce more error than the offset voltage itself. Figure 3.2 shows a circuit for measuring offset voltage. The circuit amplifies the input offset voltage by the noise gain (1001). The measurement is made at the amplifier output using an accurate digital voltmeter. The offset referred to the input (RTI) is calculated by dividing the output voltage by the noise gain. The small source resistance seen at R1||R2 results in negligible bias current contribution to the measured offset voltage. For example, 2nA bias current flowing through the 10Ω resistor produces a 0.02μV error referred to the input.

MEASURING INPUT OFFSET VOLTAGE

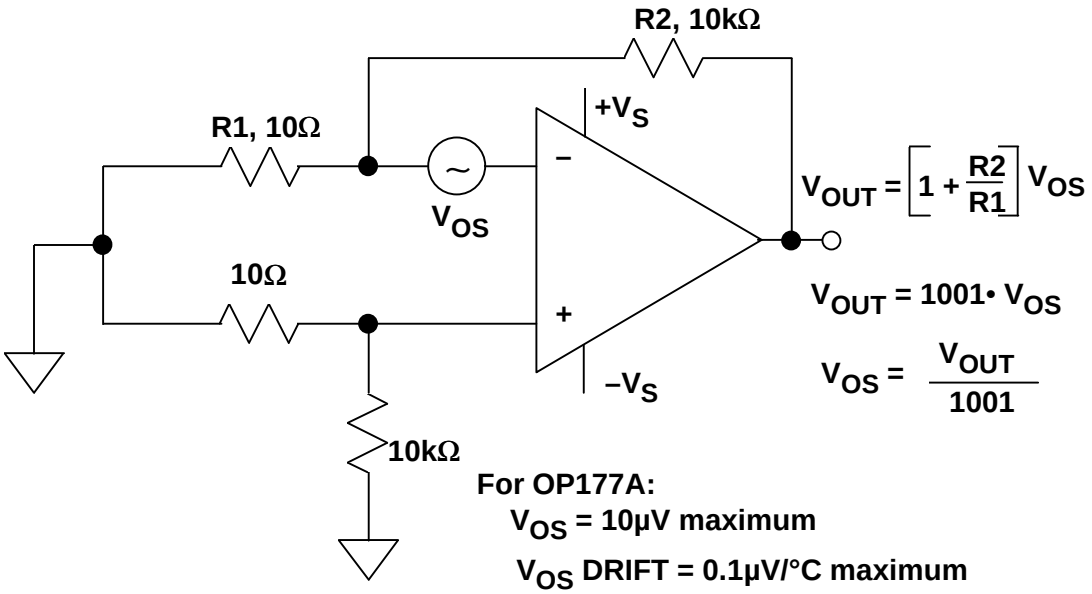


Figure 3.2

As simple as it looks, this circuit may give inaccurate results. The largest potential source of error comes from parasitic thermocouple junctions formed where two different metals are joined. The thermocouple voltage formed by temperature difference between two junctions can range from 2μV/ºC to more than 40μV/ºC. Note that in the circuit additional resistors have been added to the non-inverting input in order to exactly match the thermocouple junctions in the inverting input path.

The accuracy of the measurement depends on the mechanical layout of the components and how they are placed on the PC board. Keep in mind that the two connections of a component such as a resistor create two equal, but opposite polarity thermoelectric voltages (assuming they are connected to the same metal, such as the copper trace on a PC board) which cancel each other *assuming both are at exactly the*

same temperature. Clean connections and short lead lengths help to minimize temperature gradients and increase the accuracy of the measurement.

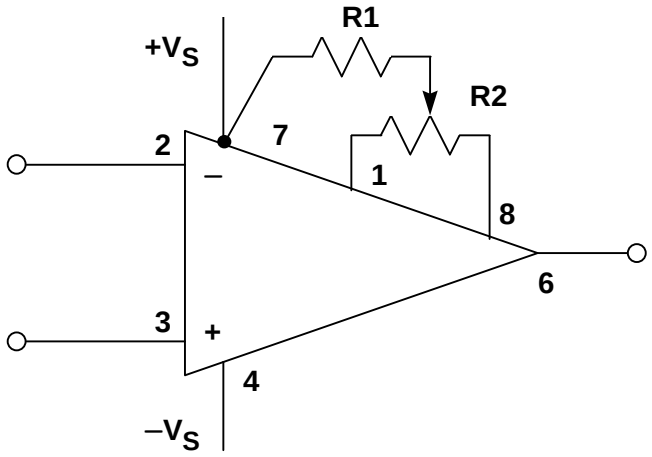
Airflow should be minimal so that all the thermocouple junctions stabilize at the same temperature. In some cases, the circuit should be placed in a small closed container to eliminate the effects of external air currents. The circuit should be placed flat on a surface so that convection currents flow up and off the top of the board, not across the components as would be the case if the board was mounted vertically.

Measuring the offset voltage shift over temperature is an even more demanding challenge. Placing the printed circuit board containing the amplifier being tested in a small box or plastic bag with foam insulation prevents the temperature chamber air current from causing thermal gradients across the parasitic thermocouples. If cold testing is required, a dry nitrogen purge is recommended. Localized temperature cycling of the amplifier itself using a Thermostream-type heater/cooler may be an alternative, however these units tend to generate quite a bit of airflow which can be troublesome.

In addition to temperature related drift, the offset voltage of an amplifier changes as time passes. This aging effect is generally specified as *long-term stability* in µV/month, or µV/1000 hours, but this is misleading. Since aging is a "drunkard's walk" phenomenon, it is proportional to the *square root* of the elapsed time. An aging rate of 1µV/1000 hours becomes about 3µV/year, not 9µV/year. Long-term stability of the OP177 and the AD707 is approximately 0.3µV/month. This refers to a time period *after* the first 30 days of operation. Excluding the initial hour of operation, changes in the offset voltage of these devices during the first 30 days of operation are typically less than 2µV.

As a general rule of thumb, it is prudent to control amplifier offset voltage by device selection whenever possible, bus sometimes trim may be desired. Many precision op amps have pins available for optional offset null. Generally, two pins are joined by a potentiometer, and the wiper goes to one of the supplies through a resistor as shown in Figure 3.3. If the wiper is connected to the wrong supply, the op amp will probably be destroyed, so the data sheet instructions must be carefully observed! The range of offset adjustment in a precision op amp should be no more than two or three times the maximum offset voltage of the lowest grade device, in order to minimize the sensitivity of these pins. The voltage gain of an op amp between its offset adjustment pins and its output may actually be greater than the gain at its signal inputs! It is therefore very important to keep these pins free of noise. It is inadvisable to have long leads from an op amp to a remote potentiometer. To minimize any offset error due to supply current, connect R1 directly to the pertinent device supply pin, such as pin 7 shown in the diagram.

OP177/AD707 OFFSET ADJUSTMENT PINS



- R1 = 10kΩ, R2 = 2kΩ , OFFSET ADJUST RANGE = 200µV
- R1 = 0, R1 = 20kΩ , OFFSET ADJUST RANGE = 3mV

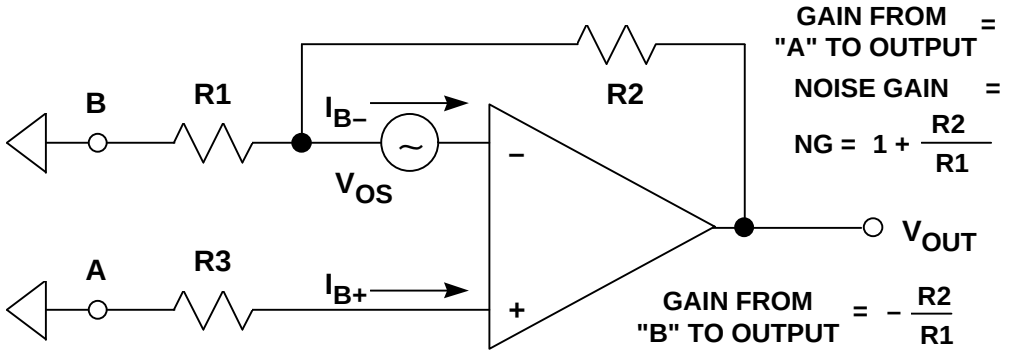
Figure 3.3

It is important to note that the offset drift of an op amp with temperature will vary with the setting of its offset adjustment. In most cases a bipolar op amp will have minimum drift at minimum offset. The offset adjustment pins should therefore be used only to adjust the op amp's own offset, not to correct any system offset errors, since this would be at the expense of increased temperature drift. The drift penalty for a JFET input op amp is much worse than for a bipolar input and is in the order of 4µV/ºC for each millivolt of nulled offset voltage. It is generally better to control the offset voltage by proper selection of devices and device grades. Dual, triple, quad, and single op amps in small packages do not generally have null capability because of pin count limitations, and offset adjustments must be done elsewhere in the system when using these devices. This can be accomplished with minimal impact on drift by a universal trim, which sums a small voltage into the input.

Input Offset Voltage and Input Bias Current Models

Thus far, we have considered only the op amp input offset voltage. However, the input bias currents also contribute to offset error as shown in the generalized model of Figure 3.4. It is useful to refer all offsets to the op amp input (RTI) so that they can be easily compared with the input signal. The equations in the diagram are given for the total offset voltage referred to input (RTI) and referred to output (RTO).

OP AMP TOTAL OFFSET VOLTAGE MODEL



■ OFFSET (RTO) = $V_{OS}\left[1 + \frac{R2}{R1}\right] + I_{B+} \cdot R3\left[1 + \frac{R2}{R1}\right] - I_{B-} \cdot R2$

■ OFFSET (RTI) = $V_{OS} + I_{B+} \cdot R3 - I_{B-}\left[\frac{R1 \cdot R2}{R1 + R2}\right]$

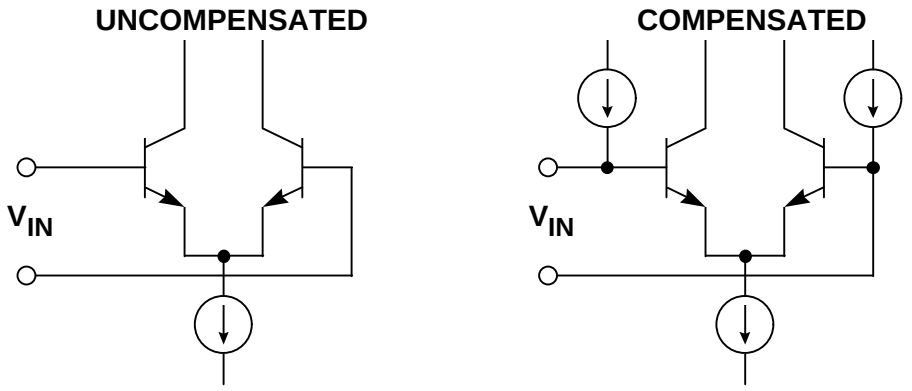
FOR BIAS CURRENT CANCELLATION:

OFFSET (RTI) = V_{OS} IF $I_{B+} = I_{B-}$ AND $R3 = \frac{R1 \cdot R2}{R1 + R2}$

Figure 3.4

For a precision op amp having a standard bipolar input stage using either PNPs or NPNs, the input bias currents are typically 50nA to 400nA and are well matched. By making R3 equal to the parallel combination of R1 and R2, their effect on the net RTI and RTO offset voltage is approximately canceled, thus leaving the offset current, i.e., the difference between the input currents as an error. This current is usually an order of magnitude lower than the bias current specification. This scheme, however, does not work for bias-current compensated bipolar op amps (such as the OP177 and the AD707) as shown in Figure 3.5. Bias-current compensated input stages have most of the good features of the simple bipolar input stage: low offset and drift, and low voltage noise. Their bias current is low and fairly stable over temperature. The additional current sources reduce the net bias currents typically to between 0.5nA and 10nA. However, the signs of the + and – input bias currents may or may not be the same, and they are not well matched, but are very low. Typically, the specification for the *offset current* (the difference between the + and – input bias currents) in bias-current compensated op amps is generally about the same as the individual bias currents. In the case of the standard bipolar differential pair with no bias-current compensation, the offset current specification is typically five to ten times lower than the bias current specification.

INPUT BIAS CURRENT COMPENSATED OP AMPS



- MATCHED BIAS CURRENTS
- SAME SIGN
- 50nA - 10µA
- 50pA - 5nA (Super Beta)
- $I_{OFFSET} << I_{BIAS}$

- LOW, UNMATCHED BIAS CURRENTS
- CAN HAVE DIFFERENT SIGNS
- 0.5nA - 10nA
- HIGHER CURRENT NOISE
- $I_{OFFSET} \approx I_{BIAS}$

Figure 3.5

DC Open Loop Gain Nonlinearity

It is well understood that in order to maintain accuracy, a precision amplifier's DC open loop gain, A_{VOL}, should be high. This can be seen by examining the equation for the closed loop gain:

$$\text{Closed Loop Gain} = A_{VCL} = \frac{NG}{1 + \frac{NG}{A_{VOL}}}.$$

Noise gain (NG) is simply the gain seen by a small voltage source in series with the op amp input and is also the amplifier signal gain in the noninverting mode. If A_{VOL} in the above equation is infinite, the closed loop gain is exactly equal to the noise gain. However, for finite values of A_{VOL}, there is a closed loop gain error given by the equation:

$$\%\text{Gain Error} = \frac{NG}{NG + A_{VOL}} \times 100\% \approx \frac{NG}{A_{VOL}} \times 100\%, \text{ for } NG << A_{VOL}.$$

Notice from the equation that the percent gain error is directly proportional to the noise gain, therefore the effects of finite A_{VOL} are less for low gain. The first example in Figure 3.6 where the noise gain is 1000 shows that for an open loop gain of 2 million, there is a gain error of about 0.05%. If the open loop gain stays constant over temperature and for various output loads and voltages, the gain error can be calibrated out of the measurement, and there is then no overall system gain error. If, however, the open loop gain *changes*, the closed loop gain will also change, thereby introducing a *gain uncertainty*. In the second example in the figure, an A_{VOL} decrease to 300,000 produces a gain error of 0.33%, introducing a *gain*

uncertainty of 0.28% in the closed loop gain. In most applications, using the proper amplifier, the resistors around the circuit will be the largest source of gain error.

CHANGES IN DC OPEN LOOP GAIN CAUSE CLOSED LOOP GAIN UNCERTAINTY

- **"IDEAL" CLOSED LOOP GAIN = NOISE GAIN = NG**
- **ACTUAL CLOSED LOOP GAIN =** $\dfrac{NG}{1+\dfrac{NG}{A_{VOL}}}$
- **% CLOSED LOOP GAIN ERROR =** $\dfrac{NG}{NG + A_{VOL}} \times 100\% \approx \dfrac{NG}{A_{VOL}} \times 100\%$
  - **Assume A_{VOL} = 2,000,000, NG = 1,000**
    %GAIN ERROR ≈ 0.05%
  - **Assume A_{VOL} Drops to 300,000**
    %GAIN ERROR ≈ 0.33%
  - **CLOSED LOOP GAIN UNCERTAINTY**
    = 0.33% – 0.05% = 0.28%

Figure 3.6

Changes in the output voltage level and the output loading are the most common causes of changes in the open loop gain of op amps. A change in open loop gain with signal level produces *nonlinearity* in the closed loop gain transfer function which cannot be removed during system calibration. Most op amps have fixed loads, so A_{VOL} changes with load are not generally important. However, the sensitivity of A_{VOL} to output signal level may increase for higher load currents.

The severity of the nonlinearity varies widely from device type to device type, and is generally not specified on the data sheet. The minimum A_{VOL} is always specified, and choosing an op amp with a high A_{VOL} will minimize the probability of gain nonlinearity errors. Gain nonlinearity can come from many sources, depending on the design of the op amp. One common source is thermal feedback. If temperature shift is the sole cause of the nonlinearity error, it can be assumed that minimizing the output loading will help. To verify this, the nonlinearity is measured with no load and then compared to the loaded condition.

An oscilloscope X-Y display test circuit for measuring DC open loop gain nonlinearity is shown in Figure 3.7. The same precautions previously discussed relating to the offset voltage test circuit must be observed in this circuit. The amplifier is configured for a signal gain of –1. The open loop gain is defined as the change in output voltage divided by the change in the input offset voltage. However, for large values of A_{VOL}, the offset may change only a few microvolts over the entire output voltage swing. Therefore the divider consisting of the 10Ω resistor and R_G (1M Ω) forces the voltage V_Y to be :

$$V_Y = \left[1 + \frac{R_G}{10\Omega}\right] V_{OS} = 100{,}001 \bullet V_{OS}.$$

The value of R_G is chosen to give measurable voltages at V_Y depending on the expected values of V_{OS}.

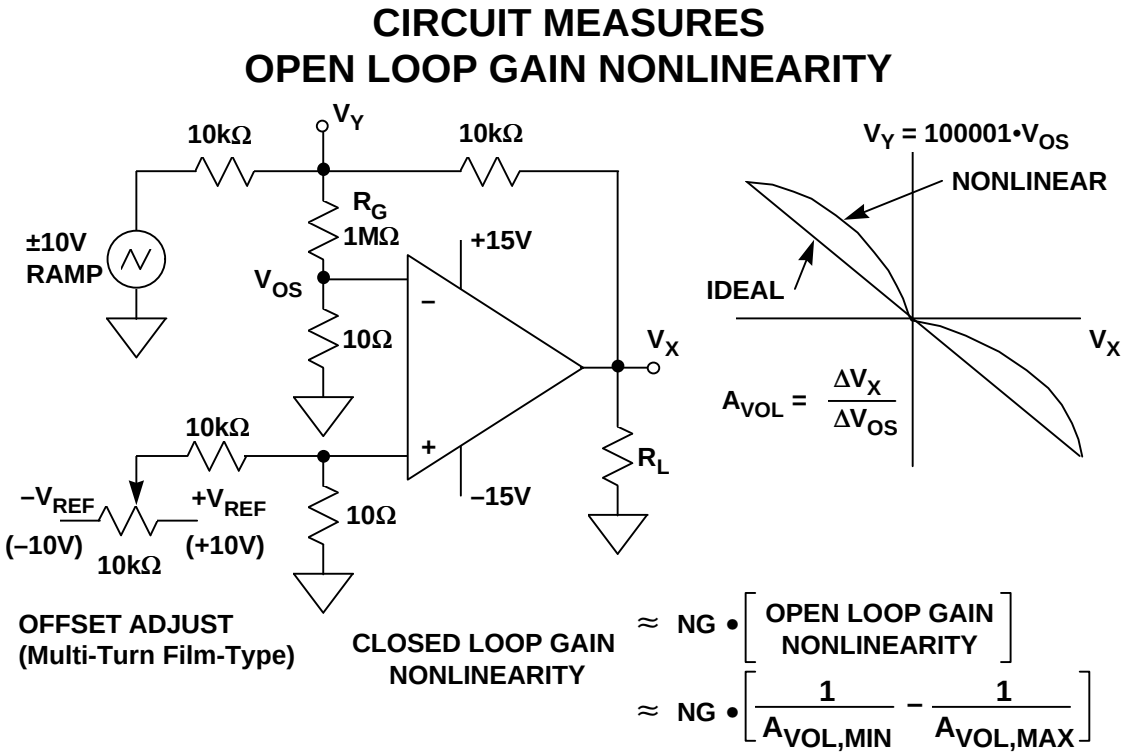


Figure 3.7

The ±10V ramp generator output is multiplied by the signal gain, –1, and forces the op amp output voltage V_X to swing from +10V to –10V. Because of the gain factor applied to the offset voltage, the offset adjust potentiometer is added to allow the initial output offset to be set to zero. The resistor values chosen will null an input offset voltage of up to ±10mV. Stable 10V voltage references (AD688) should be used at each end of the potentiometer to prevent output drift. *Also, the frequency of the ramp generator must be quite low, probably no more than a fraction of 1Hz because of the low corner frequency of the open loop gain (0.1Hz for the OP177).*

The plot on the right-hand side of Figure 3.7 shows V_Y plotted against V_X. If there is no gain nonlinearity the graph will have a constant slope, and A_{VOL} is calculated as follows:

$$A_{VOL} = \frac{\Delta V_X}{\Delta V_{OS}} = \left[1 + \frac{R_G}{10\Omega}\right]\left[\frac{\Delta V_X}{\Delta V_Y}\right] = 100{,}001 \bullet \left[\frac{\Delta V_X}{\Delta V_Y}\right].$$

If there is nonlinearity, A_{VOL} will vary as the output signal changes. The approximate open loop gain nonlinearity is calculated based on the maximum and minimum values of A_{VOL} over the output voltage range:

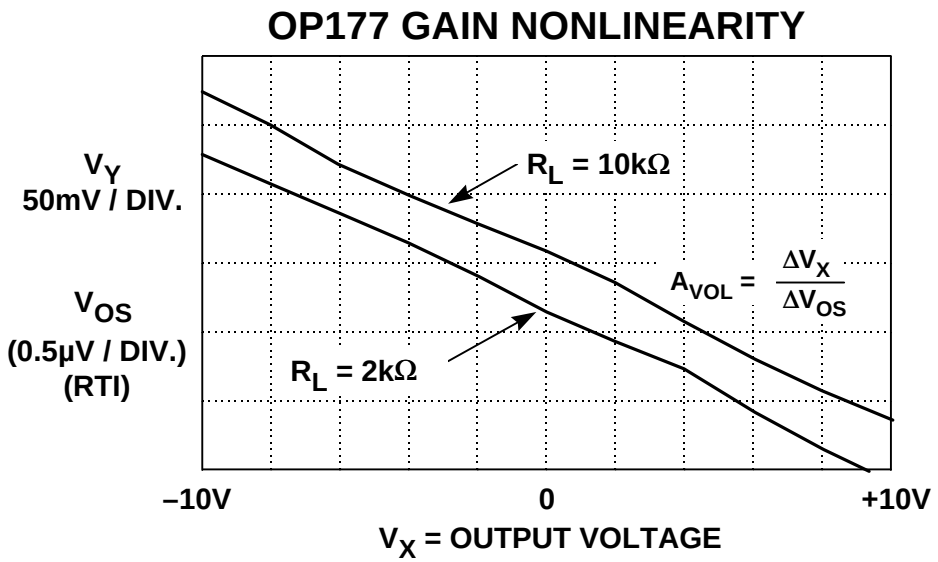
$$\text{Open Loop Gain Nonlinearity} = \frac{1}{A_{VOL,MIN}} - \frac{1}{A_{VOL,MAX}}.$$

The closed loop gain nonlinearity is obtained by multiplying the open loop gain nonlinearity by the noise gain, NG:

$$\text{Closed Loop Gain Nonlinearity} \approx NG \bullet \left[\frac{1}{A_{VOL,MIN}} - \frac{1}{A_{VOL,MAX}}\right].$$

In the ideal case, the plot of V_{OS} versus V_X would have a constant slope, and the reciprocal of the slope is the open loop gain, A_{VOL}. A horizontal line with zero slope would indicate infinite open loop gain. In an actual op amp, the slope may change across the output range because of nonlinearity, thermal feedback, etc. In fact, the slope can even change sign.

Figure 3.8 shows the V_Y (and V_{OS}) versus V_X plot for the OP177 precision op amp. The plot is shown for two different loads, 2kΩ and 10kΩ. The reciprocal of the slope is calculated based on the end points, and the average A_{VOL} is about 8 million. The maximum and minimum values of A_{VOL} across the output voltage range are measured to be approximately 9.1 million, and 5.7 million, respectively. This corresponds to an open loop gain nonlinearity of about 0.07ppm. Thus, for a noise gain of 100, the corresponding closed loop gain nonlinearity is about 7ppm.



A_{VOL} (AVERAGE) ≈ 8 million

$A_{VOL,MAX}$ ≈ 9.1 million, $A_{VOL,MIN}$ ≈ 5.7million

OPEN LOOP GAIN NONLINEARITY ≈ 0.07ppm

CLOSED LOOP GAIN NONLINEARITY ≈ NG×0.07ppm

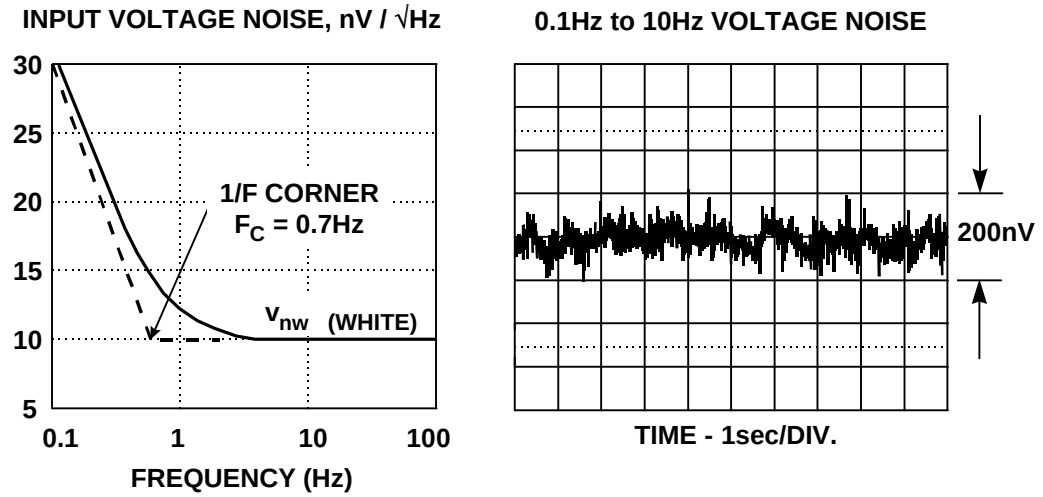
Figure 3.8

Op Amp Noise

The three noise sources in an op amp circuit are the voltage noise of the op amp, the current noise of the op amp (there are two uncorrelated sources, one in each input),

and the Johnson noise of the resistances in the circuit. Op amp noise has two components - "white" noise at medium frequencies and low frequency "1/f" noise, whose spectral density is inversely proportional to the square root of the frequency. It should be noted that, though both the voltage and the current noise may have the same characteristic behavior, in a particular amplifier the 1/f corner frequency is not necessarily the same for voltage and current noise (it is usually specified for the voltage noise as shown in Figure 3.9.

INPUT VOLTAGE NOISE FOR OP177/AD707



- $V_{n,rms}(F_H, F_L) = v_{nw}\sqrt{F_C \ln\left[\frac{F_H}{F_L}\right] + (F_H - F_L)}$
- For F_L = 0.1Hz, F_H = 10Hz, v_{nw} = 10nV/ √Hz, F_C = 0.7Hz:
  - $V_{n,rms}$ = 36nV
  - $V_{n,pp}$ = 6.6 × 36nV = 238nV

Figure 3.9

The low frequency noise is generally known as 1/f noise (the noise power obeys a 1/f law - the noise voltage or noise current is proportional to 1/√f). The frequency at which the 1/f noise spectral density equals the white noise is known as the *1/f corner frequency*, F_C, and is a figure of merit for an op amp, with low corner frequencies indicating better performance. Values of 1/f corner frequency vary from less than 1Hz high accuracy bipolar op amps like the OP177/AD707, several hundred Hz for the AD743/745 FET-input op amps, to several thousands of Hz for some high speed op amps where process compromises favor high speed rather than low frequency noise.

For the OP177/AD707 shown in Figure 3.9, the 1/f corner frequency is 0.7Hz, and the white noise is 10nV/√Hz. The low frequency 1/f noise is often expressed as the peak-to-peak noise in the bandwidth 0.1Hz to 10Hz as shown in the scope photo in Figure 3.9. Note that this noise ultimately limits the resolution of a precision measurement system because the bandwidth up to 10Hz is usually the bandwidth of most interest. The equation for the total rms noise, $V_{n,rms}$, in the bandwidth F_L to F_H is given by the equation:

$$V_{n,rms}(F_H, F_L) = v_{nw}\sqrt{F_C \ln\left[\frac{F_H}{F_L}\right] + (F_H - F_L)},$$

where v_{nw} is the noise spectral density in the "white noise" region (usually specified at a frequency of 1kHz), F_C is the 1/f corner frequency, and F_L and F_H is the measurement bandwidth of interest. In the example shown, the 0.1Hz to 10Hz noise is calculated to be 36nV rms, or approximately 238nV peak-to-peak, which closely agrees with the scope photo on the right (a factor of 6.6 is generally used to convert rms values to peak-to-peak values).

It should be noted that at higher frequencies, the term in the equation containing the natural logarithm becomes insignificant, and the expression for the rms noise becomes:

$$V_{n,rms}(F_H, F_L) \approx v_{nw}\sqrt{F_H - F_L}.$$

And, if $F_H >> F_L$,

$$V_{n,rms}(F_H) \approx v_{nw}\sqrt{F_H}.$$

However, some op amps (such as the OP07 and OP27) have voltage noise characteristics that increase slightly at high frequencies. The voltage noise versus frequency curve for op amps should therefore be examined carefully for flatness when calculating high frequency noise using this approximation.

At very low frequencies when operating exclusively in the 1/f region, $F_C >> (F_H - F_L)$, and the expression for the rms noise reduces to:

$$V_{n,rms}(F_H, F_L) \approx v_{nw}\sqrt{F_C \ln\left[\frac{F_H}{F_L}\right]}.$$

Note that there is no way of reducing this 1/f noise by filtering if operation extends to DC. Making F_H=0.1Hz and F_L= 0.001 still yields an rms 1/f noise of about 18nV rms, or 119nV peak-to-peak.

The point is that averaging the results of a large number of measurements taken over a long period of time has practically no effect on the error produced by 1/f noise. The only method of reducing it further is to use a chopper stabilized op amp which does not pass the low frequency noise components.

A generalized noise model for an op amp is shown in Figure 3.10. All uncorrelated noise sources add as a root-sum-of-squares manner, i.e., noise voltages V1, V2, and V3 give a result of:

$$\sqrt{V1^2 + V2^2 + V3^2}.$$

Thus, any noise voltage which is more than 4 or 5 times any of the others is dominant, and the others may generally be ignored. This simplifies noise analysis.

In this diagram, the total noise of all sources is shown referred to the input (RTI). The RTI noise is useful because it can be compared directly to the input signal level. The total noise referred to the output (RTO) is obtained by simply multiplying the RTI noise by the noise gain.

The diagram assumes that the feedback network is purely resistive. If it contains reactive elements (usually capacitors), the noise gain is not constant over the bandwidth of interest, and more complex techniques must be used to calculate the total noise (see in particular, Reference 12). However, for precision applications where the feedback network is most likely to be resistive, the equations are valid.

Notice that the Johnson noise voltage associated with the three resistors has been included. All resistors have a Johnson noise of $\sqrt{4kTBR}$, where k is Boltzmann's Constant (1.38×10^{-23} J/K), T is the absolute temperature, B is the bandwidth in Hz, and R is the resistance in Ω. A simple relationship which is easy to remember is that *a 1000Ω resistor generates a Johnson noise of 4nV/√Hz at 25°C*.

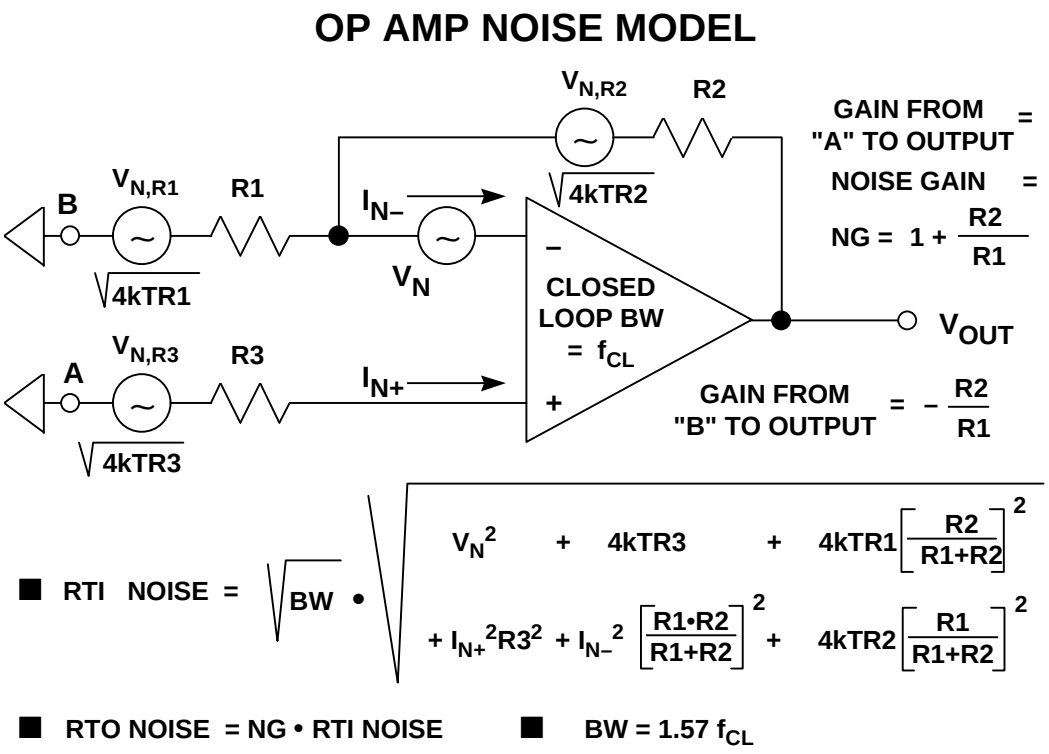


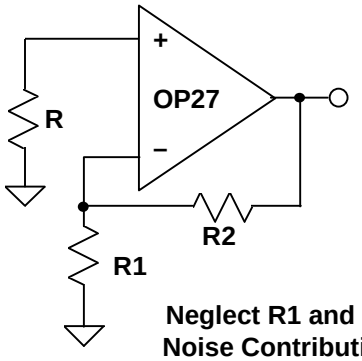
Figure 3.10

The voltage noise of various op amps may vary from under 1nV/√Hz to 20nV/√Hz, or even more. Bipolar input op amps tend to have lower voltage noise than JFET input ones, although it is possible to make JFET input op amps with low voltage noise (such as the AD743/AD745), at the cost of large input devices and hence large (~20pF) input capacitance. Current noise can vary much more widely, from around 0.1fA/√Hz (in JFET input electrometer op amps) to several pA/√Hz (in high speed bipolar op amps). For bipolar or JFET input devices where all the bias current flows into the input junction, the current noise is simply the Schottky (or shot) noise of the bias current. The shot noise spectral density is simply $\sqrt{2I_Bq}$ amps/√Hz, where I_B is the bias current (in amps) and q is the charge on an electron (1.6×10^{-19} C). It cannot be calculated for bias-compensated or current feedback op amps where the external bias current is the difference between two internal current sources.

Current noise is only important when it flows through an impedance and in turn generates a noise voltage. The equation shown in Figure 3.10 shows how the current noise flowing in the resistors contribute to the total noise. The choice of a low noise op amp therefore depends on the impedances around it. Consider an OP27, a bias compensated op amp with low voltage noise (3nV/√Hz), but quite high current noise (1pA/√Hz) as shown in the schematic of Figure 3.11. With zero source impedance, the voltage noise dominates. With a source resistance of 3kΩ, the current noise (1pA/√Hz) flowing in 3kΩ will equal the voltage noise, but the Johnson noise of the 3kΩ resistor is 7nV/√Hz and so is dominant. With a source resistance of 300kΩ, the effect of the current noise increases a hundredfold to 300nV/√Hz, while the voltage noise is unchanged, and the Johnson noise (which is proportional to the *square root* of the resistance) increases tenfold. Here, the current noise dominates.

DIFFERENT NOISE SOURCES DOMINATE AT DIFFERENT SOURCE IMPEDANCES

EXAMPLE: OP27
Voltage Noise = 3nV / √ Hz
Current Noise = 1pA / √ Hz
T = 25°C



Neglect R1 and R2 Noise Contribution

CONTRIBUTION FROM	VALUES OF R		
	0	3kΩ	300kΩ
AMPLIFIER VOLTAGE NOISE	**3**	3	3
AMPLIFIER CURRENT NOISE FLOWING IN R	0	3	**300**
JOHNSON NOISE OF R	0	**7**	70

RTI NOISE (nV / √ Hz)
Dominant Noise Source is Highlighted

Figure 3.11

The above example shows that the choice of a low noise op amp depends on the source impedance of the input signal, and at high impedances, current noise always dominates. This is shown in Figure 3.12 for several bipolar (OP07, OP27, 741) and JFET (AD645, AD743, AD744) op amps.

For low impedance circuitry (generally < 1kΩ), amplifiers with low voltage noise, such as the OP27 will be the obvious choice, and their comparatively large current noise will not affect the application. At medium resistances, the Johnson noise of resistors is dominant, while at very high resistances, we must choose an op amp with the smallest possible current noise, such as the AD549 or AD645.

Until recently, BiFET amplifiers (with JFET inputs) tended to have comparatively high voltage noise (though very low current noise), and thus were more suitable for low noise applications in high rather than low impedance circuitry. The AD645, AD743, and AD745 have very low values of both voltage and current noise. The AD645 specifications at 10kHz are 10nV/√Hz and 0.6fA/√Hz, and the AD743/AD745 specifications at 10kHz are 2.0nV/√Hz and 6.9fA/√Hz. These make possible the design of low noise amplifier circuits which have low noise over a wide range of source impedances.

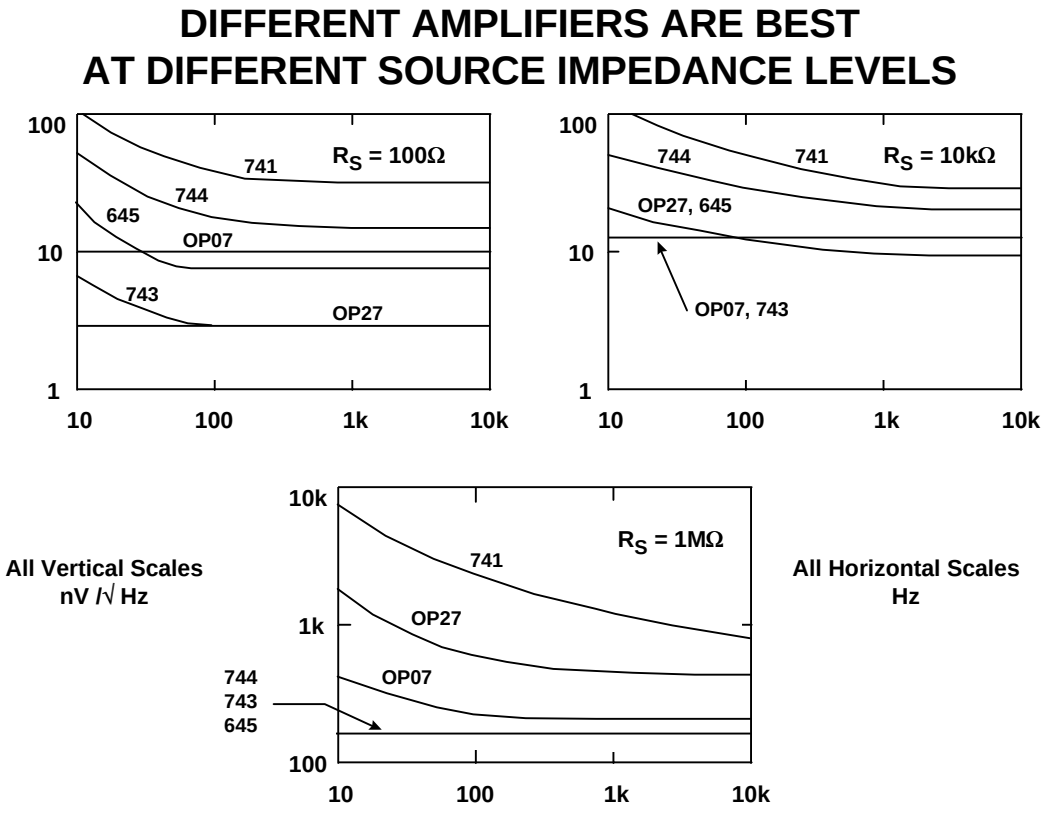


Figure 3.12

Common Mode Rejection and Power Supply Rejection

If a signal is applied equally to both inputs of an op amp so that the differential input voltage is unaffected, the output should not be affected. In practice, changes in common mode voltage will produce changes in the output. The *common mode rejection ratio* or CMRR is the ratio of the common mode gain to the differential-mode gain of an op amp. For example, if a differential input change of Y volts will produce a change of 1V at the output, and a common mode change of X volts produces a similar change of 1V, then the CMRR is X/Y. It is normally expressed in dB, and typical LF values are between 70 and 120dB. When expressed in dB, it is generally referred to as *common mode rejection* (CMR). At higher frequencies, CMR deteriorates - many op amp data sheets show a plot of CMR versus frequency as shown in Figure 3.13 for the OP177/AD707 precision op amps.

CMRR produces a corresponding output offset voltage error in op amps configured in the non-inverting mode as shown in Figure 3.14. Op amps configured in the inverting mode have no CMRR output error because both inputs are at ground or virtual ground, so there is no common mode voltage, only the offset voltage of the amplifier if un-nulled.

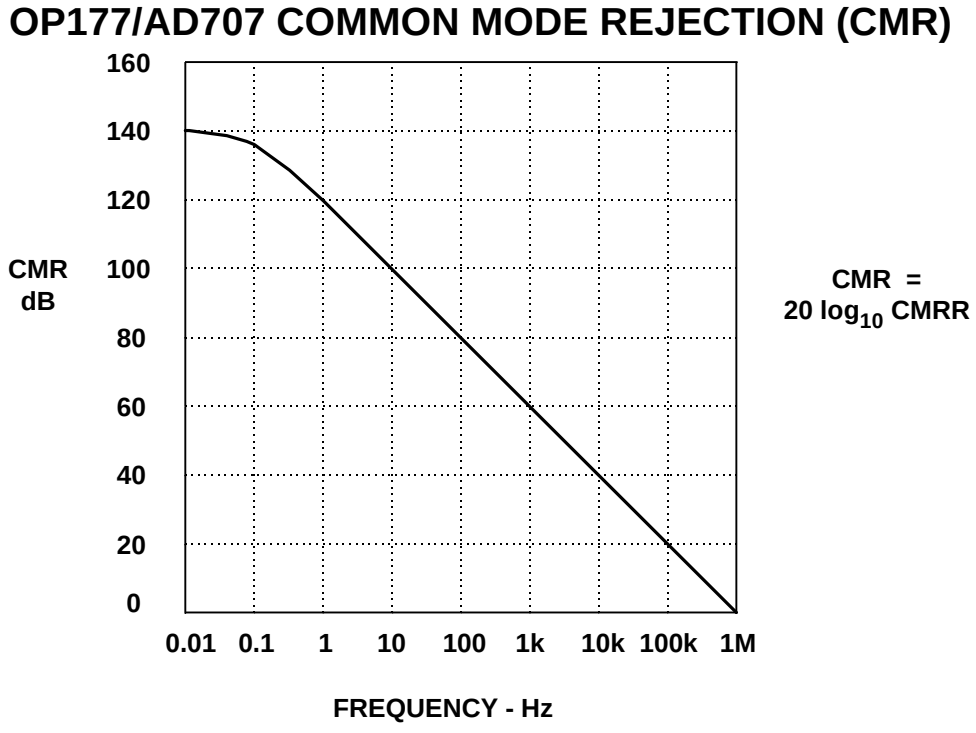


Figure 3.13

CALCULATING OFFSET ERROR DUE TO COMMON MODE REJECTION RATIO (CMRR)

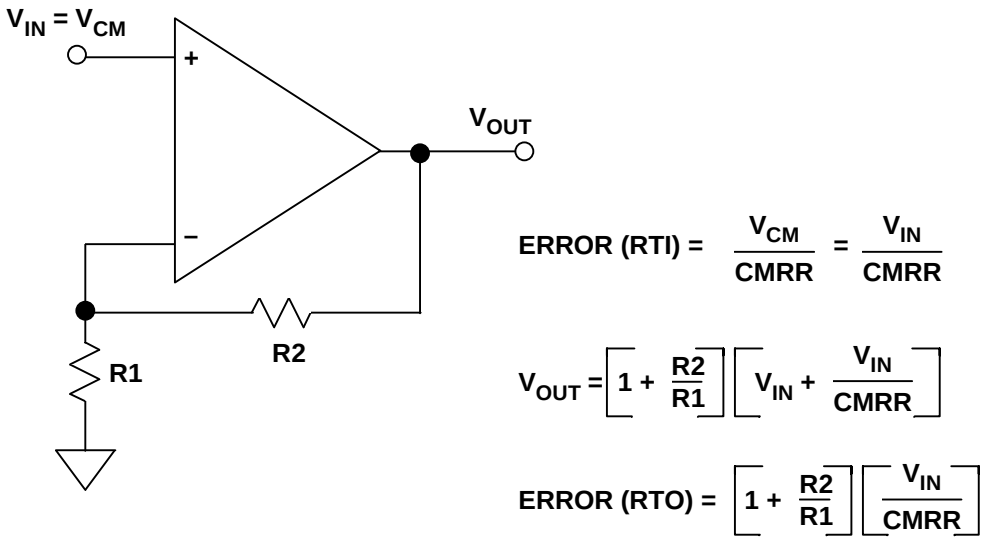


Figure 3.14

If the supply of an op amp changes, its output should not, but it will. The specification of *power supply rejection ratio* or PSRR is defined similarly to the definition of CMRR. If a change of X volts in the supply produces the same output change as a differential input change of Y volts, then the PSRR on that supply is X/Y. When the ratio is expressed in dB, it is generally referred to as *power supply rejection*, or PSR. The definition of PSRR assumes that both supplies are altered equally in opposite directions - otherwise the change will introduce a common mode change as well as a supply change, and the analysis becomes considerably more complex. It is this effect which causes apparent differences in PSRR between the positive and negative supplies. In the case of single supply op amps, PSR is generally defined with respect to the change in the positive supply. Many single supply op amps have separate PSR specifications for the positive and negative supplies. The PSR of the OP177/AD707 is shown in Figure 3.15.

The PSRR of op amps is frequency dependent, therefore power supplies must be well decoupled as shown in Figure 3.16. At low frequencies, several devices may share a 10 - 50µF capacitor on each supply, provided it is no more than 10cm (PC track distance) from any of them. At high frequencies, each IC must have every supply decoupled by a low inductance capacitor (0.1µF or so) with short leads and PC tracks. These capacitors must also provide a return path for HF currents in the op amp load. Decoupling capacitors should be connected to a low impedance large area ground plane with minimum lead lengths. Surface mount capacitors minimize lead inductance and are a good choice.

OP177/AD707 POWER SUPPLY REJECTION (PSR)

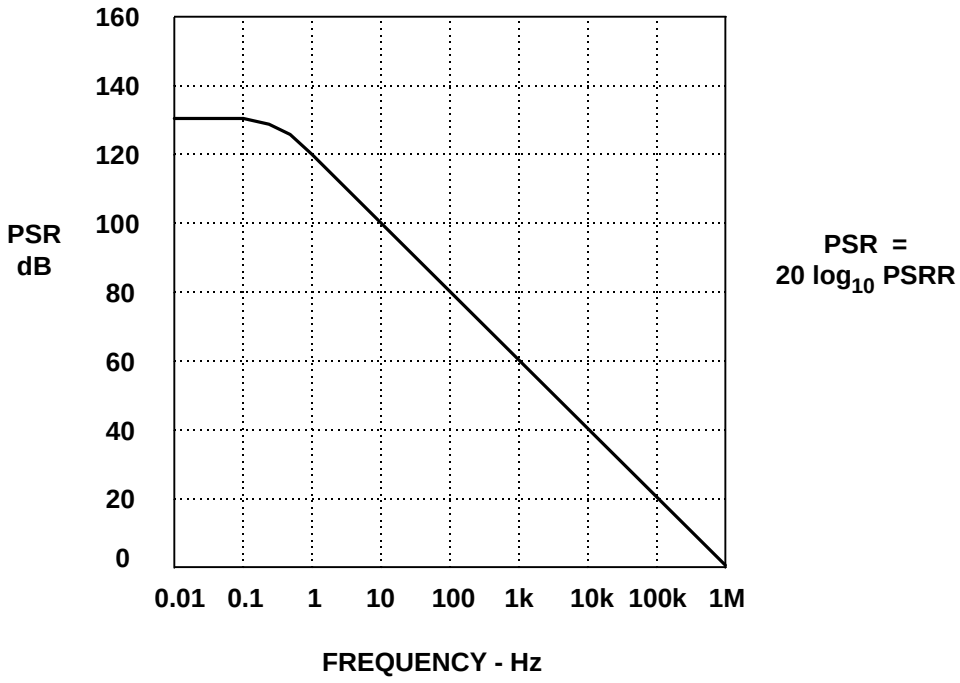


Figure 3.15

PROPER LOW AND HIGH-FREQUENCY DECOUPLING TECHNIQUES FOR OP AMPS

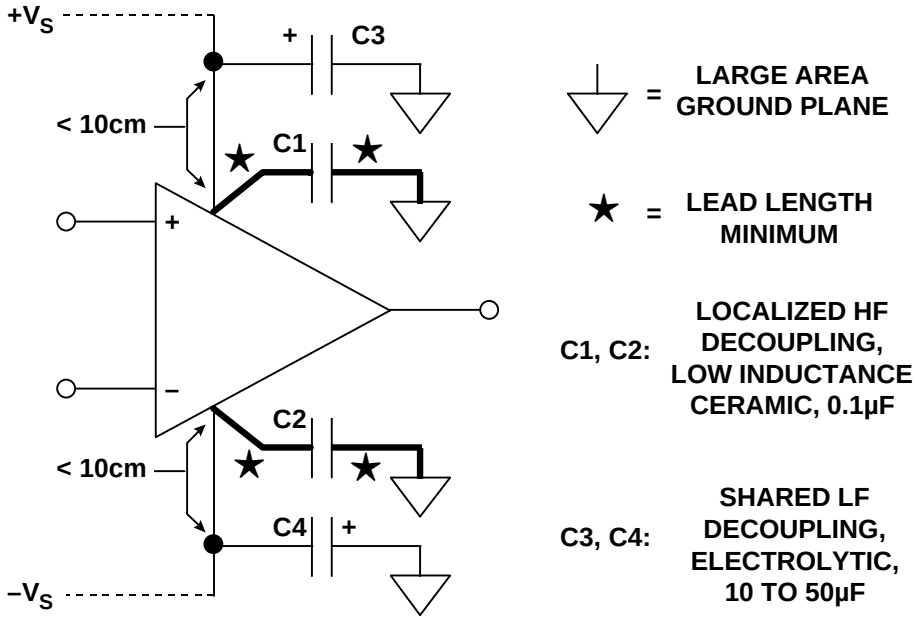


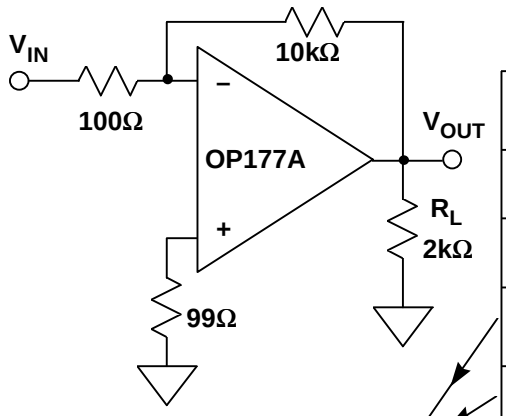
Figure 3.16

AMPLIFIER DC ERROR BUDGET ANALYSIS

A room temperature error budget analysis for the OP177A op amp is shown in Figure 3.17. The amplifier is connected in the inverting mode with a signal gain of 100. The key data sheet specifications are also shown in the diagram. We assume an input signal of 100mV fullscale which corresponds to an output signal of 10V. The various error sources are normalized to fullscale and expressed in parts per million (ppm). Note: parts per million (ppm) error = fractional error × 10^6 = % error × 10^4.

Note that the offset errors due to V_{OS} and I_{OS} and the gain error due to finite A_{VOL} can be removed with a system calibration. However, the error due to open loop gain nonlinearity cannot be removed with calibration and produces a relative accuracy error, often called *resolution error*. The second contributor to resolution error is the 1/f noise. This noise is always present and adds to the uncertainty of the measurement. The overall relative accuracy of the circuit at room temperature is 9ppm which is equivalent to approximately 17 bits of resolution.

PRECISION OP AMP (OP177A) DC ERROR BUDGET



SPECS @ +25°C:

V_{OS} = 10µV max
I_{OS} = 1nA max
A_{VOL} = 5×10^6 min
A_{VOL} Nonlinearity = 0.07ppm
0.1Hz to 10Hz Noise = 200nV

MAXIMUM ERROR CONTRIBUTION, + 25°C
FULLSCALE: V_{IN}=100mV, V_{OUT} = 10V

V_{OS}	10µV ÷ 100mV	100ppm
I_{OS}	100Ω × 1nA ÷ 100mV	1ppm
A_{VOL}	(100/ 5×10^6) × 100mV	20ppm
A_{VOL} Nonlinearity	100 × 0.07ppm	7ppm
0.1Hz to 10Hz 1/f Noise	200nV ÷ 100mV	2ppm
Total Unadjusted Error	≈ 13 Bits Accurate	130ppm
Resolution Error	≈ 17 Bits Accurate	9ppm

Figure 3.17

SINGLE SUPPLY OP AMPS

Over the last several years, single-supply operation has become an increasingly important requirement because of market requirements. Automotive, set-top box, camera/cam-corder, PC, and laptop computer applications are demanding IC vendors to supply an array of linear devices that operate on a single supply rail, with the same performance of dual supply parts. Power consumption is now a key parameter for line or battery operated systems, and in some instances, more important than cost. This makes low-voltage/low supply current operation critical; at the same time, however, accuracy and precision requirements have forced IC manufacturers to meet the challenge of “doing more with less” in their amplifier designs.

SINGLE SUPPLY AMPLIFIERS

- **Single Supply Offers:**
  - **Lower Power**
  - **Battery Operated Portable Equipment**
  - **Requires Only One Voltage**

- **Design Tradeoffs:**
  - **Reduced Signal Swing Increases Sensitivity to Errors Caused by Offset Voltage, Bias Current, Finite Open-Loop Gain, Noise, etc.**
  - **Must Usually Share Noisy Digital Supply**
  - **Rail-to-Rail Input and Output Needed to Increase Signal Swing**
  - **Precision Less than the best Dual Supply Op Amps but not Required for All Applications**
  - **Many Op Amps Specified for Single Supply, but do not have Rail-to-Rail Inputs or Outputs**

Figure 3.18

In a single-supply application, the most immediate effect on the performance of an amplifier is the reduced input and output signal range. As a result of these lower input and output signal excursions, amplifier circuits become more sensitive to internal and external error sources. Precision amplifier offset voltages on the order of 0.1mV are less than a 0.04 LSB error source in a 12-bit, 10V full-scale system. In a single-supply system, however, a "rail-to-rail" precision amplifier with an offset voltage of 1mV represents a 0.8LSB error in a 5V fullscale system, and 1.6LSB error in a 2.5V fullscale system.

To keep battery current drain low, larger resistors are usually used around the op amp. Since the bias current flows through these larger resistors, they can generate offset errors equal to or greater than the amplifier's own offset voltage.

Gain accuracy in some low voltage single-supply devices is also reduced, so device selection needs careful consideration. Many amplifiers having open-loop gains in the millions typically operate on dual supplies: for example, the OP07 family types. However, many single-supply/rail-to-rail amplifiers for precision applications typically have open-loop gains between 25,000 and 30,000 under light loading (>10kΩ). Selected devices, like the OP113/213/413 family, do have high open-loop gains (i.e., > 1M).

Many trade-offs are possible in the design of a single-supply amplifier circuit: speed versus power, noise versus power, precision versus speed and power, etc. Even if the noise floor remains constant (highly unlikely), the signal-to-noise ratio will drop as the signal amplitude decreases.

Besides these limitations, many other design considerations that are otherwise minor issues in dual-supply amplifiers now become important. For example, signal-to-noise (SNR) performance degrades as a result of reduced signal swing. "Ground reference" is no longer a simple choice, as one reference voltage may work for some devices, but not others. Amplifier voltage noise increases as operating supply current drops, and bandwidth decreases. Achieving adequate bandwidth and required precision with a somewhat limited selection of amplifiers presents significant system design challenges in single-supply, low-power applications.

Most circuit designers take "ground" reference for granted. Many analog circuits scale their input and output ranges about a ground reference. In dual-supply applications, a reference that splits the supplies (0V) is very convenient, as there is equal supply headroom in each direction, and 0V is generally the voltage on the low impedance ground plane.

In single-supply/rail-to-rail circuits, however, the ground reference can be chosen anywhere within the supply range of the circuit, since there is no standard to follow. The choice of ground reference depends on the type of signals processed and the amplifier characteristics. For example, choosing the negative rail as the ground reference may optimize the dynamic range of an op amp whose output is designed to swing to 0V. On the other hand, the signal may require level shifting in order to be compatible with the input of other devices (such as ADCs) that are not designed to operate at 0V input.

Early single-supply “zero-in, zero-out” amplifiers were designed on bipolar processes which optimized the performance of the NPN transistors. The PNP transistors were either lateral or substrate PNPs with much less bandwidth than the NPNs. Fully complementary processes are now required for the new-breed of single-supply/rail-to-rail operational amplifiers. These new amplifier designs do not use lateral or substrate PNP transistors within the signal path, but incorporate parallel NPN and PNP input stages to accommodate input signal swings from ground to the positive supply rail. Furthermore, rail-to-rail output stages are designed with bipolar NPN and PNP common-emitter, or N-channel/P-channel common-source amplifiers whose

collector-emitter saturation voltage or drain-source channel on-resistance determine output signal swing as a function of the load current.

The characteristics of a single-supply amplifier input stage (common mode rejection, input offset voltage and its temperature coefficient, and noise) are critical in precision, low-voltage applications. Rail-to-rail input operational amplifiers must resolve small signals, whether their inputs are at ground, or in some cases near the amplifier's positive supply. Amplifiers having a minimum of 60dB common mode rejection over the entire input common mode voltage range from 0V to the positive supply are good candidates. It is not necessary that amplifiers maintain common mode rejection for signals beyond the supply voltages: *what is required is that they do not self-destruct for momentary overvoltage conditions*. Furthermore, amplifiers that have offset voltages less than 1mV and offset voltage drifts less than 2µV/°C are also very good candidates for precision applications. Since *input* signal dynamic range and SNR are equally if not more important than *output* dynamic range and SNR, precision single-supply/rail-to-rail operational amplifiers should have noise levels referred-to-input (RTI) less than 5µVp-p in the 0.1Hz to 10Hz band.

The need for rail-to-rail amplifier output stages is driven by the need to maintain wide dynamic range in low-supply voltage applications. A single-supply/rail-to-rail amplifier should have output voltage swings which are within at least 100mV of either supply rail (under a nominal load). The output voltage swing is very dependent on output stage topology and load current. The voltage swing of a good output stage should maintain its rated swing for loads down to 10kΩ. The smaller the V_{OL} and the larger the V_{OH}, the better. System parameters, such as "zero-scale" or "full-scale" output voltage, should be determined by an amplifier's V_{OL} (for zero-scale) and V_{OH} (for full-scale).

Since the majority of single-supply data acquisition systems require at least 12- to 14-bit performance, amplifiers which exhibit an open-loop gain greater than 30,000 for all loading conditions are good choices in precision applications.

Single Supply Op Amp Input Stages

There is some demand for op amps whose input common mode voltage includes *both* supply rails. Such a feature is undoubtedly useful in some applications, but engineers should recognize that there are relatively few applications where it is absolutely essential. These should be carefully distinguished from the many applications where common mode range *close* to the supplies or one that includes *one* of the supplies is necessary, but input rail-to-rail operation is not.

In many single-supply applications, it is required that the input go to only one of the supply rails (usually ground). High-side or low-side sensing applications are good examples of this. Amplifiers which will handle zero-volt inputs are relatively easily designed using PNP differential pairs (or N-channel JFET pairs) as shown in Figure 3.19. The input common mode range of such an op amp extends from about 200mV below the negative supply to within about 1V of the positive supply.

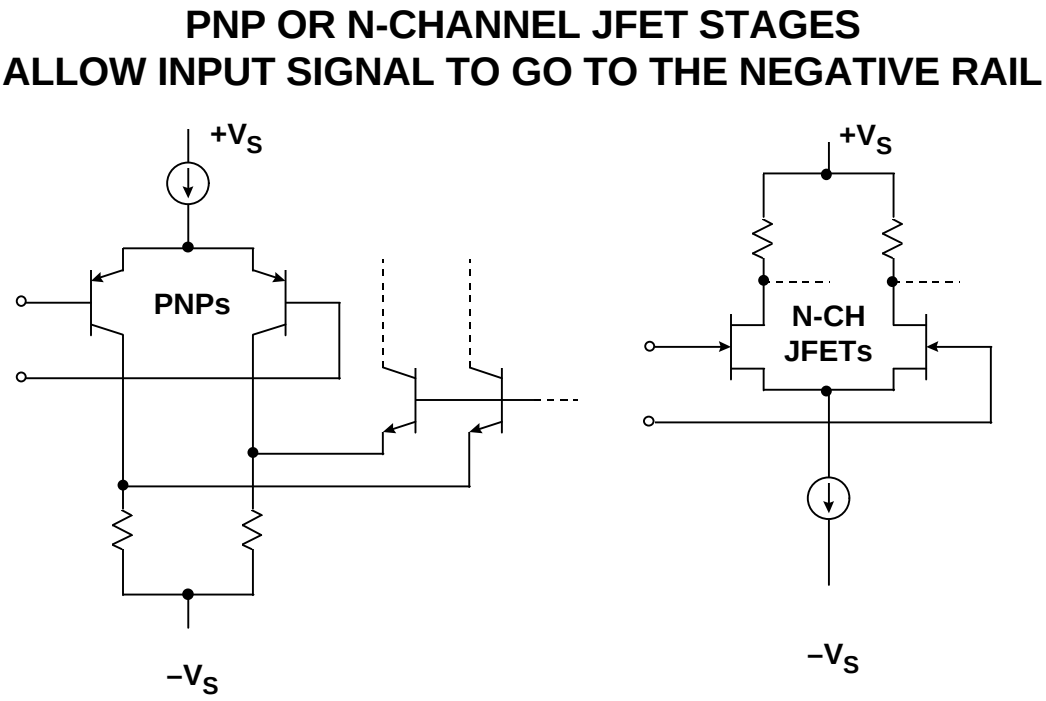


Figure 3.19

The input stage could also be designed with NPN transistors (or P-channel JFETs), in which case the input common mode range would include the positive rail and to within about 1V of the negative rail. This requirement typically occurs in applications such as high-side current sensing, a low-frequency measurement application. The OP282/OP482 input stage uses the P-channel JFET input pair whose input common mode range includes the positive rail. Other circuit topologies for high-side sensing (such as the AD626) use the precision resistors to attenuate the common mode voltage.

True rail-to-rail input stages require two long-tailed pairs (see Figure 3.20), one of NPN bipolar transistors (or N-channel JFETs), the other of PNP transistors (or P-channel JFETs). These two pairs exhibit *different* offsets and bias currents, so when the applied input common mode voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources remain active throughout the entire input common mode range, amplifier input offset voltage is the *average* offset voltage of the NPN pair and the PNP pair. In those designs where the current sources are alternatively switched off at some point along the input common mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply. It should be noted that true rail-to-rail input stages can also be constructed from CMOS transistors as in the case of the OP250/450 and the AD8531/8532/8534.

TRUE RAIL-TO-RAIL INPUT STAGE

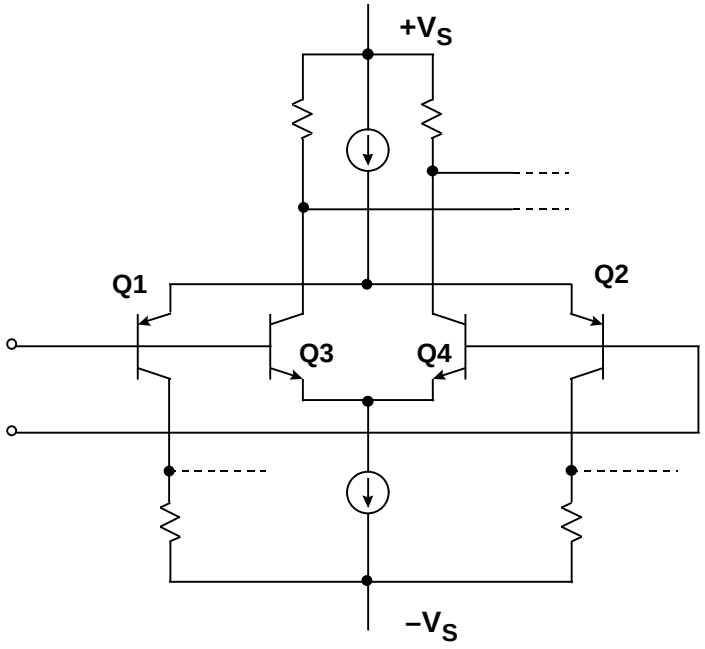


Figure 3.20

Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common mode voltage. The result is relatively poor common mode rejection (CMR), and a changing common mode input impedance over the common mode input voltage range, compared to familiar dual-supply devices. These specifications should be considered carefully when choosing a rail-rail input op amp, especially for a non-inverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over *part* of the common mode range, but much worse in the region where operation shifts between the NPN and PNP devices and vice versa.

True rail-to-rail amplifier input stage designs must transition from one differential pair to the other differential pair somewhere along the input common mode voltage range. Some devices like the OP191/291/491 family and the OP279 have a common mode crossover threshold at approximately 1V below the positive supply. The PNP differential input stage is active from about 200mV below the negative supply to within about 1V of the positive supply. Over this common mode range, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are primarily determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly. Also, amplifier bias currents, dominated by the PNP differential pair over most of the input common mode range, change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active.

Op amps like the OP184/284/484, utilize a rail-to-rail input stage design where both NPN and PNP transistor pairs are active throughout the entire input common mode voltage range, and there is no common mode crossover threshold. Amplifier input offset voltage is the average offset voltage of the NPN and the PNP stages. Amplifier

input offset voltage exhibits a smooth transition throughout the entire input common mode range because of careful laser trimming of the resistors in the input stage. In the same manner, through careful input stage current balancing and input transistor design, amplifier input bias currents also exhibit a smooth transition throughout the entire common mode input voltage range. The exception occurs at the extremes of the input common mode range, where amplifier offset voltages and bias currents increase sharply due to the slight forward-biasing of parasitic p-n junctions. This occurs for input voltages within approximately 1V of either supply rail.

When *both* differential pairs are active throughout the entire input common mode range, amplifier transient response is faster through the middle of the common mode range by as much as a factor of 2 for bipolar input stages and by a factor of $\sqrt{2}$ for JFET input stages. Input stage transconductance determines the slew rate and the unity-gain crossover frequency of the amplifier, hence response time degrades slightly at the extremes of the input common mode range when either the PNP stage (signals approaching the positive supply rail) or the NPN stage (signals approaching the negative supply rail) are forced into cutoff. The thresholds at which the transconductance changes occur are approximately within 1V of either supply rail, and the behavior is similar to that of the input bias currents.

Applications which require true rail-rail inputs should therefore be carefully evaluated, and the amplifier chosen to ensure that its input offset voltage, input bias current, common mode rejection, and noise (voltage and current) are suitable.

Single Supply Op Amp Output Stages

The earliest IC op amp output stages were NPN emitter followers with NPN current sources or resistive pull-downs, as shown in the left-hand diagram of Figure 3.21. Naturally, the slew rates were greater for positive-going than for negative-going signals. While all modern op amps have push-pull output stages of some sort, many are still asymmetrical, and have a greater slew rate in one direction than the other. Asymmetry tends to introduce distortion on AC signals and generally results from the use of IC processes with faster NPN than PNP transistors. It may also result in the ability of the output to approach one supply more closely than the other.

In many applications, the output is required to swing only to one rail, usually the negative rail (i.e., ground in single-supply systems). A pulldown resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high enough, or is also grounded to that rail), but only slowly. Using an FET current source instead of a resistor can speed things up, but this adds complexity.

With new complementary bipolar processes (CB), well matched high speed PNP and NPN transistors are available. The complementary emitter follower output stage shown in the right-hand diagram of Figure 3.21 has many advantages including low output impedance. However, the output can only swing within about one V_{BE} drop of either supply rail. An output swing of +1V to +4V is typical of such stages when operated on a single +5V supply.

TRADITIONAL OUTPUT STAGES

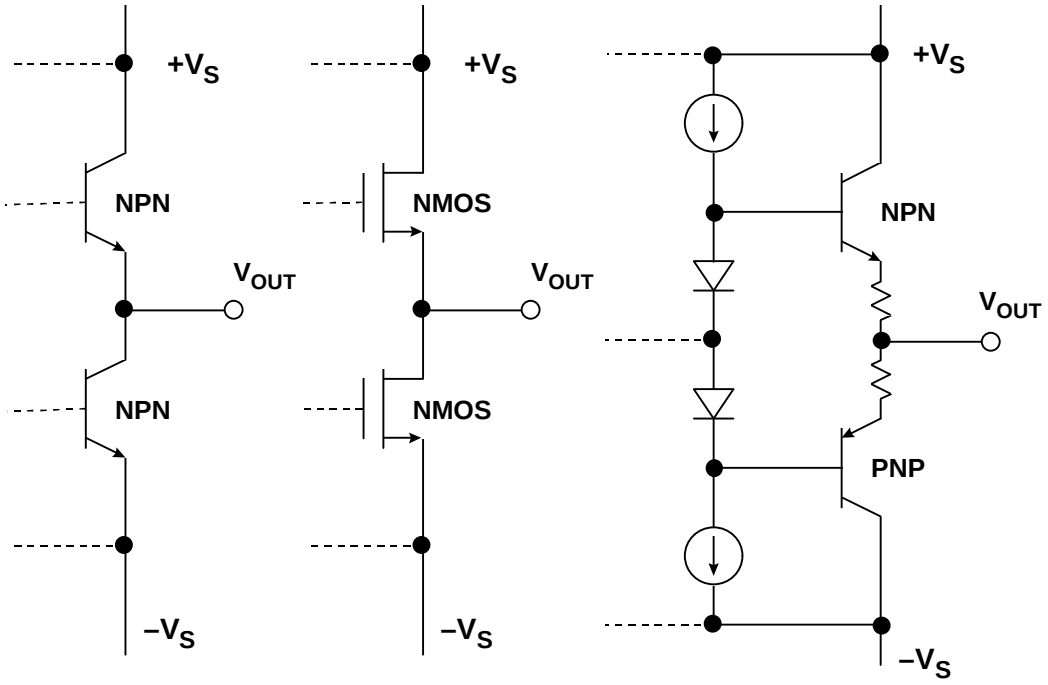


Figure 3.21

The complementary common-emitter/common-source output stages shown in Figure 3.22 allow the output voltage to swing much closer to the output rails, but these stages have higher open loop output impedance than the emitter follower- based stages. In practice, however, the amplifier's open loop gain and local feedback produce an apparent low output impedance, particularly at frequencies below 10Hz.

The complementary common emitter output stage using BJTs (left-hand diagram in Figure 3.22) cannot swing completely to the rails, but only to within the transistor saturation voltage (V_{CESAT}) of the rails. For small amounts of load current (less than 100µA), the saturation voltage may be as low as 5 to 10mV, but for higher load currents, the saturation voltage can increase to several hundred mV (for example, 500mV at 50mA).

On the other hand, an output stage constructed of CMOS FETs can provide nearly true rail-to-rail performance, but only under no-load conditions. If the output must source or sink current, the output swing is reduced by the voltage dropped across the FETs internal "on" resistance (typically, 100Ω for precision amplifiers, but can be less than 10Ω for high current drive CMOS amplifiers).

For these reasons, it is apparent that there is no such thing as a true rail-to-rail output stage, hence the title of Figure 3.22 ("Almost" Rail-to-Rail Output Stages).

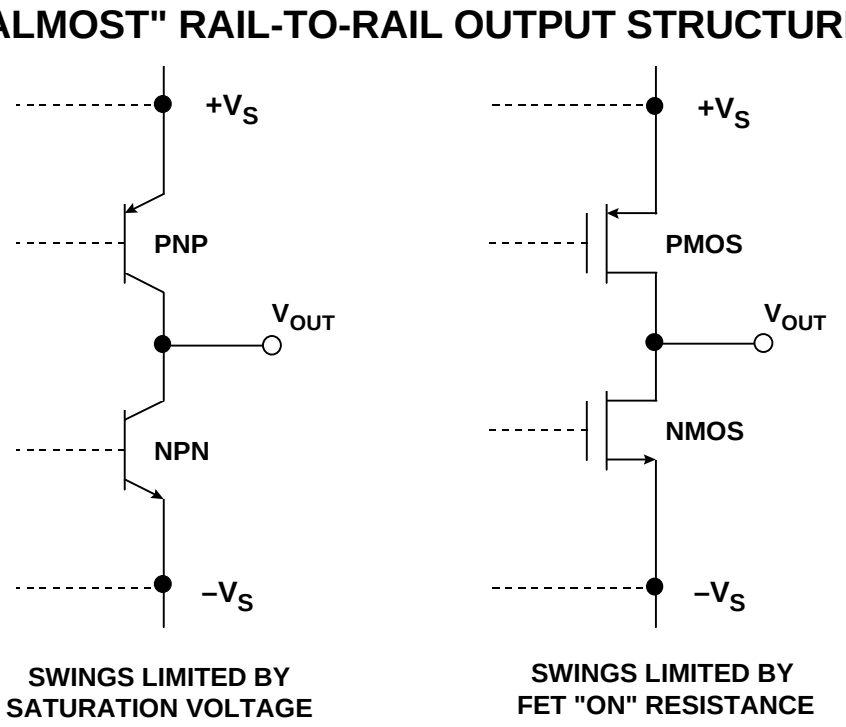


Figure 3.22

Figure 3.23 summarizes the performance characteristics of a number of single-supply op amps suitable for some precision applications. The devices are listed in order of increasing supply current. Single, dual, and quad versions of each op amp are available, so the supply current is the normalized I_{SY}/amplifier for comparison. The input and output voltage ranges (V_S = +5V) are also supplied in the table. The "0, 4V" inputs are PNP pairs, with the exception of the AD820/822/824 which use N-Channel JFETs. Output stages having voltage ranges designated "5mV, 4V" are NPN emitter-followers with current source pull-downs (OP193/293/493, OP113/213/413). Output stages designated "R/R" use CMOS common source stages (OP181/281/481) or CB common emitter stages (OP196/296/496, OP191/291/491, AD820/822/824, OP184/284/484).

In summary, the following points should be considered when selecting amplifiers for single-supply/rail-to-rail applications:

First, input offset voltage and input bias currents are a function of the applied input common mode voltage (for true rail-to-rail input op amps). Circuits using this class of amplifiers should be designed to minimize resulting errors. An inverting amplifier configuration with a false ground reference at the non-inverting input prevents these errors by holding the input common mode voltage constant. If the inverting amplifier configuration cannot be used, then amplifiers like the OP184/284/OP484 which do not exhibit any common mode crossover thresholds should be used.

PRECISION SINGLE-SUPPLY OP AMP PERFORMANCE CHARACTERISTICS

****LISTED IN ORDER OF INCREASING SUPPLY CURRENT**

**PART NO.	V_{OS} max	V_{OS} TC	A_{VOL} min	NOISE (1kHz)	INPUT	OUTPUT	I_{SY}/AMP
OP181/281/481	1500µV	10µV/°C	5M	70nV/√Hz	0, 4V	"R/R"	4µA
OP193/293/493	75µV	0.2µV/°C	200k	65nV/√Hz	0, 4V	5mV, 4V	15µA
OP196/296/496	300µV	1.5µV/°C	150k	26nV/√Hz	R/R	"R/R"	50µA
OP191/291/491	700µV	1.1µV/°C	25k	35nV/√Hz	R/R	"R/R"	400µA
*AD820/822/824	400µV	2µV/°C	500k	16nV/√Hz	0, 4V	"R/R"	800µA
OP184/284/484	65µV	0.2µV/°C	50k	3.9nV/√Hz	R/R	"R/R"	1250µA
OP113/213/413	125µV	0.2µV/°C	2M	4.7nV/√Hz	0, 4V	5mV, 4V	1750µA

***JFET INPUT**

NOTE: Unless Otherwise Stated Specifications are Typical @ +25°C V_S = +5V

Figure 3.23

Second, since input bias currents are not always small and can exhibit different polarities, source impedance levels should be carefully matched to minimize additional input bias current-induced offset voltages and increased distortion. Again, consider using amplifiers that exhibit a smooth input bias current transition throughout the applied input common mode voltage.

Third, rail-to-rail amplifier output stages exhibit load-dependent gain which affects amplifier open-loop gain, and hence closed-loop gain accuracy. Amplifiers with open-loop gains greater than 30,000 for resistive loads less than 10kΩ are good choices in precision applications. For applications not requiring full rail-rail swings, device families like the OP113/213/413 and OP193/293/493 offer DC gains of 200,000 or more.

Lastly, no matter what claims are made, rail-to-rail output voltage swings are functions of the amplifier's output stage devices and load current. The saturation voltage (V_{CESAT}), saturation resistance (R_{SAT}) for bipolar output stages, and FET on-resistance for CMOS output stages, as well as load current all affect the amplifier output voltage swing.

Op Amp Process Technologies

The wide variety of processes used to make op amps are shown in Figure 3.24. The earliest op amps were made using standard NPN-based bipolar processes. The PNP transistors available on these processes were extremely slow and were used primarily for current sources and level shifting.

The ability to produce matching high speed PNP transistors on a bipolar process added great flexibility to op amp circuit designs. These complementary bipolar (CB) processes are widely used in today's precision op amps, as well as those requiring wide bandwidths. The high-speed PNP transistors have f_ts which are greater than one-half the f_ts of the NPNs.

The addition of JFETs to the complementary bipolar process (CBFET) allow high input impedance op amps to be designed suitable for such applications as photodiode or electrometer preamplifiers.

CMOS op amps, with a few exceptions, generally have relatively poor offset voltage, drift, and voltage noise. However, the input bias current is very low. They offer low power and cost, however, and improved performance can be achieved with BiFET or CBFET processes.

The addition of bipolar or complementary devices to a CMOS process (BiMOS or CBCMOS) adds great flexibility, better linearity, and low power. The bipolar devices are typically used for the input stage to provide good gain and linearity, and CMOS devices for the rail-to-rail output stage.

In summary, there is no single IC process which is optimum for all op amps. Process selection and the resulting op amp design depends on the targeted applications and ultimately should be transparent to the customer.

OP AMP PROCESS TECHNOLOGY SUMMARY

- **BIPOLAR (NPN-BASED): This is Where it All Started!!**
- **COMPLEMENTARY BIPOLAR (CB): Rail-to-Rail, Precision, High Speed**
- **BIPOLAR + JFET (BiFET): High Input Impedance, High Speed**
- **COMPLEMENTARY BIPOLAR + JFET (CBFET): High Input Impedance, Rail-to-Rail Output, High Speed**
- **COMPLEMENTARY MOSFET (CMOS): Low Cost, Non-Critical Op Amps**
- **BIPOLAR + CMOS (BiCMOS): Bipolar Input Stage adds Linearity, Low Power, Rail-to-Rail Output**
- **COMPLEMENTARY BIPOLAR + CMOS (CBCMOS): Rail-to-Rail Inputs, Rail-to-Rail Outputs, Good Linearity, Low Power**

Figure 3.24

INSTRUMENTATION AMPLIFIERS (IN-AMPS)

An instrumentation amplifier is a closed-loop gain block which has a differential input and an output which is single-ended with respect to a reference terminal (see Figure 3.25). The input impedances are balanced and have high values, typically $10^9\Omega$ or higher. Unlike an op amp, which has its closed-loop gain determined by external resistors connected between its inverting input and its output, an in-amp employs an internal feedback resistor network which is isolated from its signal input terminals. With the input signal applied across the two differential inputs, gain is either preset internally or is user-set by an internal (via pins) or external gain resistor, which is also isolated from the signal inputs. Typical in-amp gain settings range from 1 to 10,000.

INSTRUMENTATION AMPLIFIER

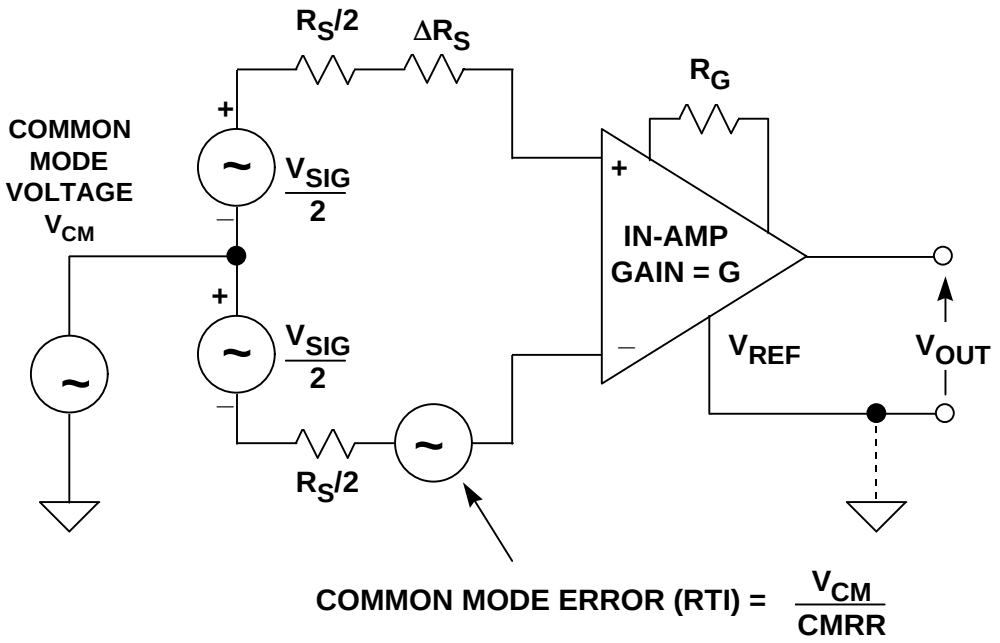


Figure 3.25

In order to be effective, an in-amp needs to be able to amplify microvolt-level signals, while simultaneously rejecting volts of common mode signal at its inputs. This requires that in-amps have very high common mode rejection (CMR): typical values of CMR are 70dB to over 100dB, with CMR usually improving at higher gains.

It is important to note that a CMR specification for DC inputs alone is not sufficient in most practical applications. In industrial applications, the most common cause of external interference is pickup from the 50/60Hz AC power mains. Harmonics of the power mains frequency can also be troublesome. In differential measurements, this type of interference tends to be induced equally onto both in-amp inputs. The interfering signal therefore appears as a common mode signal to the in-amp. Specifying CMR over frequency is more important than specifying its DC value. Imbalance in the source impedance can degrade the CMR of some in-amps. Analog Devices fully specifies in-amp CMR at 50/60Hz with a source impedance imbalance of 1kΩ.

Low-frequency CMR of op amps, connected as subtractors as shown in Figure 3.26, generally is a function of the resistors around the circuit, not the op amp. A mismatch of only 0.1% in the resistor ratios will reduce the DC CMR to approximately 66dB. Another problem with the simple op amp subtractor is that the input impedances are relatively low and are unbalanced between the two sides. The input impedance seen by V_1 is R_1, but the input impedance seen by V_2 is R1' + R2'. This configuration can be quite problematic in terms of CMR, since even a small source impedance imbalance (~ 10 Ω) will degrade the workable CMR.

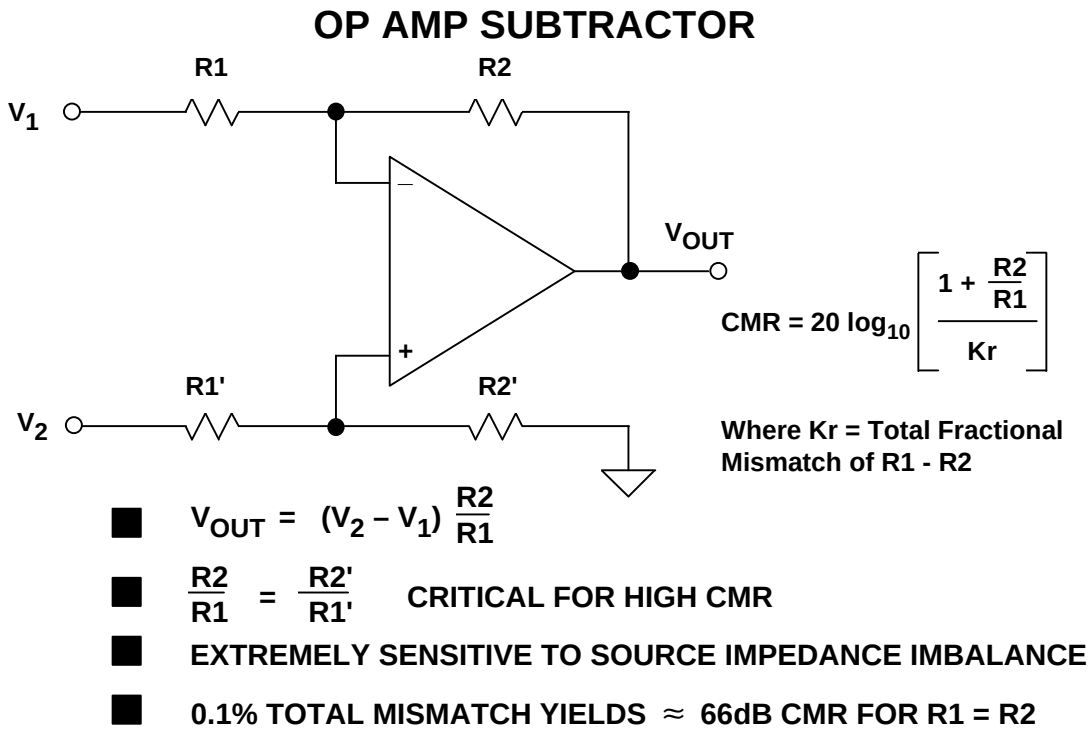


Figure 3.26

Instrumentation Amplifier Configurations

Instrumentation amplifier configurations are based on op amps, but the simple subtractor circuit described above lacks the performance required for precision applications. An in-amp architecture which overcomes some of the weaknesses of the subtractor circuit uses two op amps as shown in Figure 3.27. This circuit is typically referred to as the *two op amp in-amp*. Dual IC op amps are used in most cases for good matching. The circuit gain may be trimmed with an external resistor, R_G. The input impedance is high, permitting the impedance of the signal sources to be high and unbalanced. The DC common mode rejection is limited by the matching of R1/R2 to R1'/R2'. If there is a mismatch in any of the four resistors, the DC common mode rejection is limited to:

$$\text{CMR} \le 20 \log\left[\frac{\text{GAIN} \times 100}{\%\text{MISMATCH}}\right].$$

TWO OP AMP INSTRUMENTATION AMPLIFIER

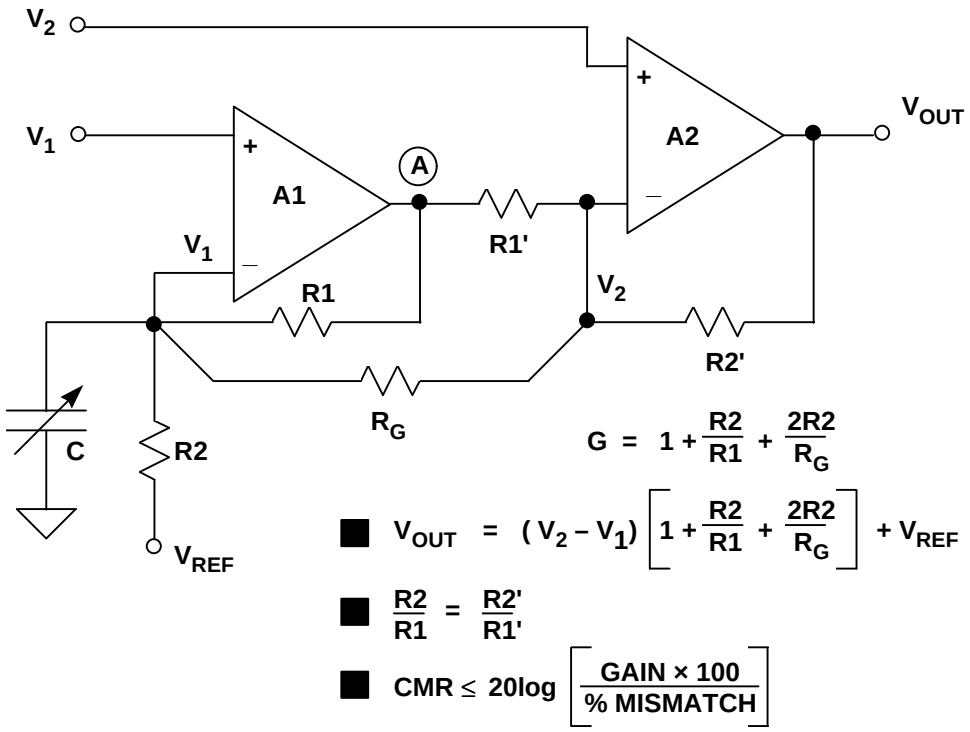


Figure 3.27

There is an implicit advantage to this configuration due to the gain executed on the signal. This raises the CMR in proportion.

Integrated instrumentation amplifiers are particularly well suited to meeting the combined needs of ratio matching and temperature tracking of the gain-setting resistors. While thin film resistors fabricated on silicon have an initial tolerance of up to ±20%, laser trimming during production allows the ratio error between the resistors to be reduced to 0.01% (100ppm). Furthermore, the tracking between the temperature coefficients of the thin film resistors is inherently low and is typically less than 3ppm/ºC (0.0003%/ºC).

When dual supplies are used, V_{REF} is normally connected directly to ground. In single supply applications, V_{REF} is usually connected to a low impedance voltage source equal to one-half the supply voltage. The gain from V_{REF} to node "A" is R1/R2, and the gain from node "A" to the output is R2'/R1'. This makes the gain from V_{REF} to the output equal to unity, assuming perfect ratio matching. Note that it is critical that the source impedance seen by V_{REF} be low, otherwise CMR will be degraded.

One major disadvantage of this design is that common mode voltage input range must be traded off against gain. The amplifier A1 must amplify the signal at V_1 by

$$1+\frac{R1}{R2}.$$

If R1 >> R2 (low gain in Figure 3.27), A1 will saturate if the common mode signal is too high, leaving no headroom to amplify the wanted differential signal. For high gains (R1<< R2), there is correspondingly more headroom at node "A" allowing larger common mode input voltages.

The AC common mode rejection of this configuration is generally poor because the signal from V_1 to V_{OUT} has the additional phase shift of A1. In addition, the two amplifiers are operating at different closed-loop gains (and thus at different bandwidths). The use of a small trim capacitor "C" as shown in the diagram can improve the AC CMR somewhat.

A low gain (G = 2) single supply two op amp in-amp configuration results when R_G is not used, and is shown in Figure 3.28. The input common mode and differential signals must be limited to values which prevent saturation of either A1 or A2. In the example, the op amps remain linear to within 0.1V of the supply rails, and their upper and lower output limits are designated V_{OH} and V_{OL}, respectively. Using the equations shown in the diagram, the voltage at V_1 must fall between 1.3V and 2.4V to prevent A1 from saturating. Notice that V_{REF} is connected to the average of V_{OH} and V_{OL} (2.5V). This allows for bipolar differential input signals with V_{OUT} referenced to +2.5V.

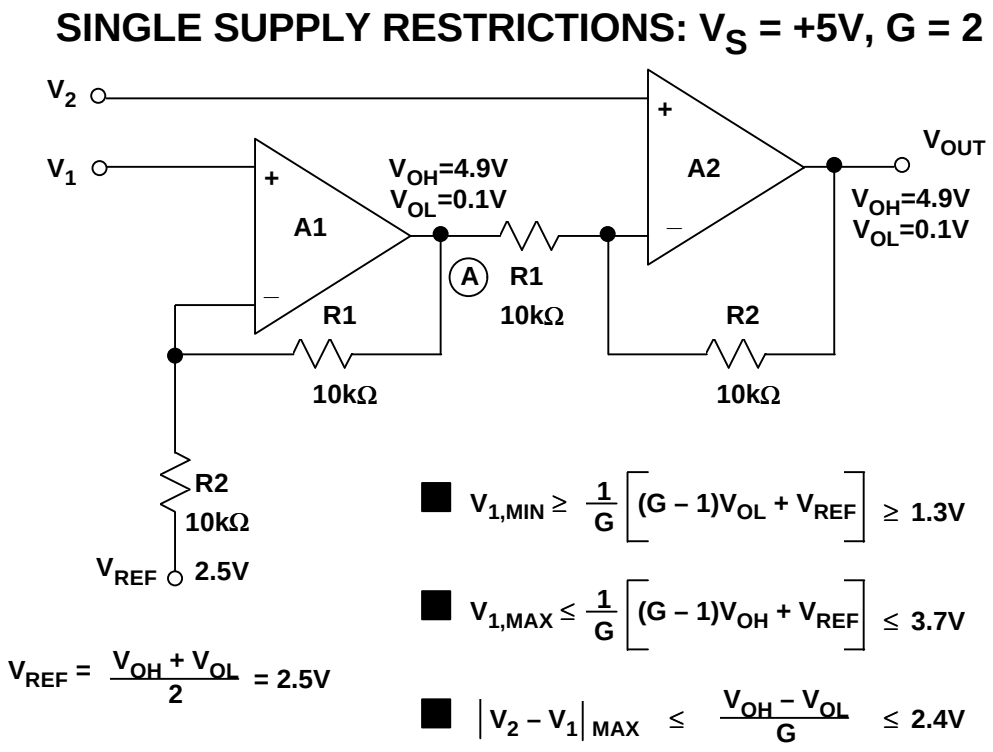


Figure 3.28

A high gain (G = 100) single supply two op amp in-amp configuration is shown in Figure 3.29. Using the same equations, note that the voltage at V_1 can now swing between 0.124V and 4.876V. Again, V_{REF} is connected to 2.5V to allow for bipolar differential input and output signals.

SINGLE SUPPLY RESTRICTIONS: V_S = +5V, G = 100

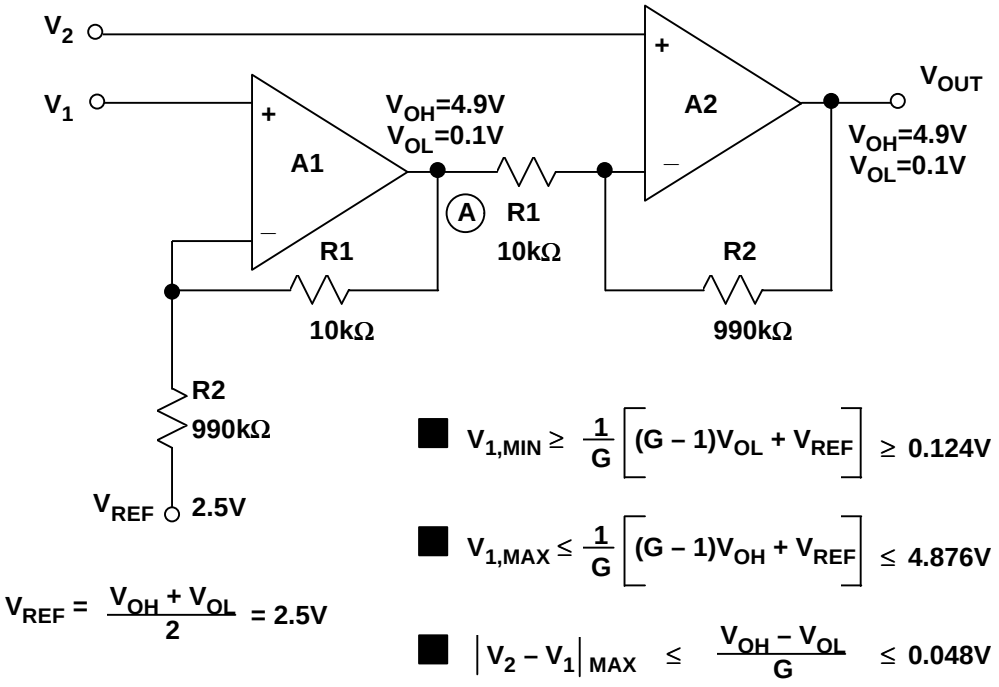


Figure 3.29

The above discussion shows that regardless of gain, the basic two op amp in-amp does not allow for zero-volt common mode input voltages when operated on a single supply. This limitation can be overcome using the circuit shown in Figure 3.30 which is implemented in the AD627 in-amp. Each op amp is composed of a PNP common emitter input stage and a gain stage, designated Q1/A1 and Q2/A2, respectively. The PNP transistors not only provide gain but also level shift the input signal positive by about 0.5V, thereby allowing the common mode input voltage to go to 0.1V below the negative supply rail. The maximum positive input voltage allowed is 1V less than the positive supply rail.

The AD627 in-amp delivers rail-to-rail output swing and operates over a wide supply voltage range (+2.7V to ±18V). Without R_G, the external gain setting resistor, the in-amp gain is 5. Gains up to 1000 can be set with a single external resistor. Common mode rejection of the AD627B at 60Hz with a 1kΩ source imbalance is 85dB when operating on a single +3V supply and G = 5. Even though the AD627 is a two op amp in-amp, a patented circuit keeps the CMR flat out to a much higher frequency than would be achievable with a conventional discrete two op amp in-amp. The AD627 data sheet (available at http://www.analog.com) has a detailed discussion of allowable input/output voltage ranges as a function of gain and power supply voltages. Key specifications for the AD627 are summarized in Figure 3.31.

AD627 IN-AMP ARCHITECTURE

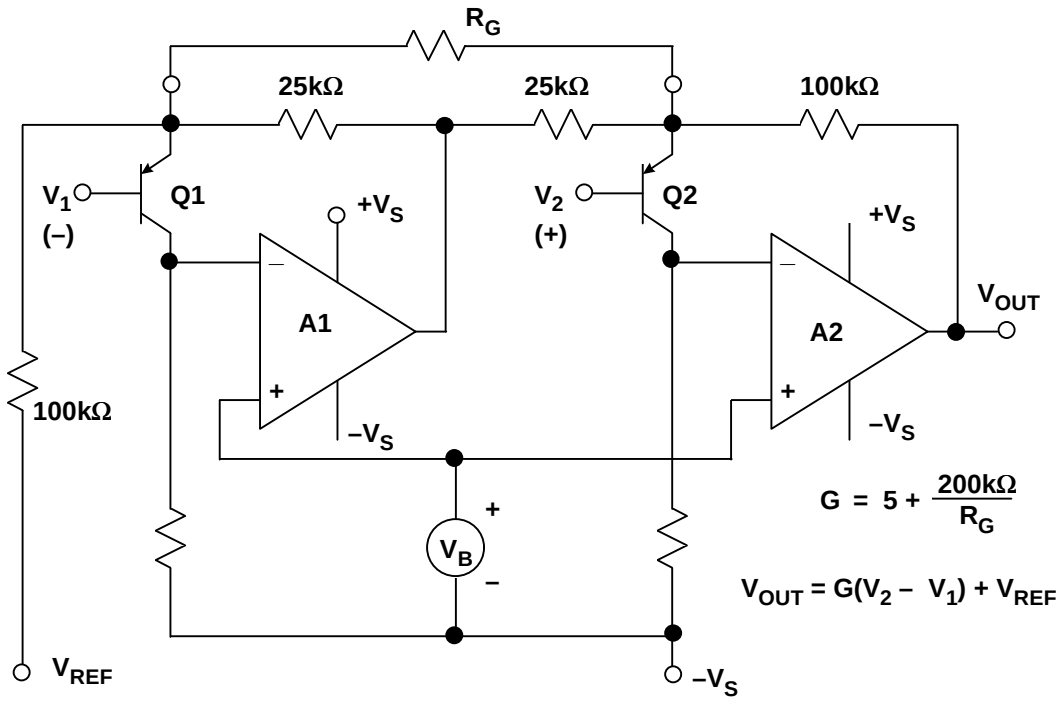


Figure 3.30

AD627 IN-AMP KEY SPECIFICATIONS

- **Wide Supply Range : +2.7V to ±18V**
- **Input Voltage Range: $–V_S$ – 0.1V to $+V_S$ – 1V**
- **85µA Supply Current**
- **Gain Range: 5 to 1000**
- **75µV Maximum Input Offset Volage (AD627B)**
- **10ppm/°C Maximum Offset Voltage TC (AD627B)**
- **10ppm Gain Nonlinearity**
- **85dB CMR @ 60Hz, 1kΩ Source Imbalance (G = 5)**
- **3µV p-p 0.1Hz to 10Hz Input Voltage Noise (G = 5)**

Figure 3.31

For true balanced high impedance inputs, three op amps may be connected to form the in-amp shown in Figure 3.32. This circuit is typically referred to as the *three op amp in-amp*. The gain of the amplifier is set by the resistor, R_G, which may be internal, external, or (software or pin-strap) programmable. In this configuration, CMR depends upon the ratio matching of R3/R2 to R3'/R2'. Furthermore, common mode signals are only amplified by a factor of 1 regardless of gain (no common mode voltage will appear across R_G, hence, no common mode current will flow in it

because the input terminals of an op amp will have no significant potential difference between them). Thus, CMR will theoretically increase in direct proportion to gain. Large common mode signals (within the A1-A2 op amp headroom limits) may be handled at all gains. Finally, because of the symmetry of this configuration, common mode errors in the input amplifiers, if they track, tend to be canceled out by the subtractor output stage. These features explain the popularity of the three op amp in-amp configuration.

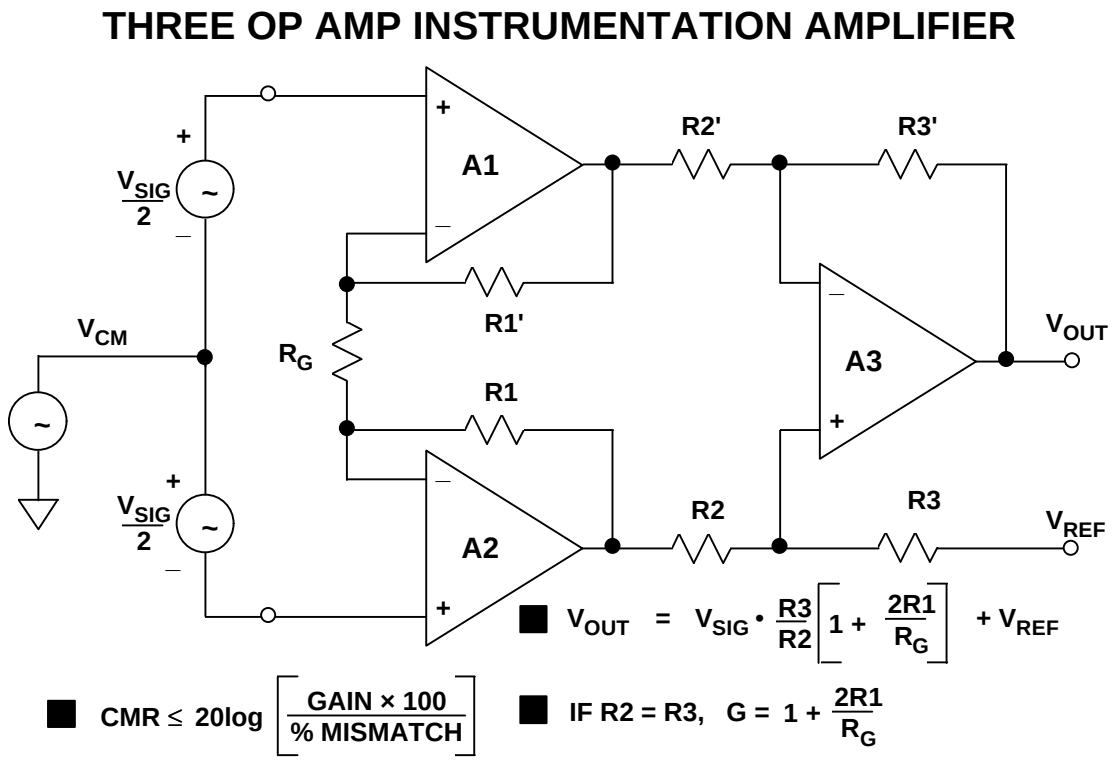


Figure 3.32

The classic three op amp configuration has been used in a number of monolithic IC instrumentation amplifiers. Besides offering excellent matching between the three internal op amps, thin film laser trimmed resistors provide excellent ratio matching and gain accuracy at much lower cost than using discrete op amps and resistor networks. The AD620 is an excellent example of monolithic in-amp technology, and a simplified schematic is shown in Figure 3.33.

The AD620 is a highly popular in-amp and is specified for power supply voltages from ±2.3V to ±18V. Input voltage noise is only 9nV/√Hz @ 1kHz. Maximum input bias current is only 1nA maximum because of the Superbeta input stage.

Overvoltage protection is provided by the internal 400Ω thin-film current-limit resistors in conjunction with the diodes which are connected from the emitter-to-base of Q1 and Q2. The gain is set with a single external R_G resistor. The appropriate internal resistors are trimmed so that standard 1% or 0.1% resistors can be used to set the AD620 gain to popular gain values.

AD620 IN-AMP SIMPLIFIED SCHEMATIC

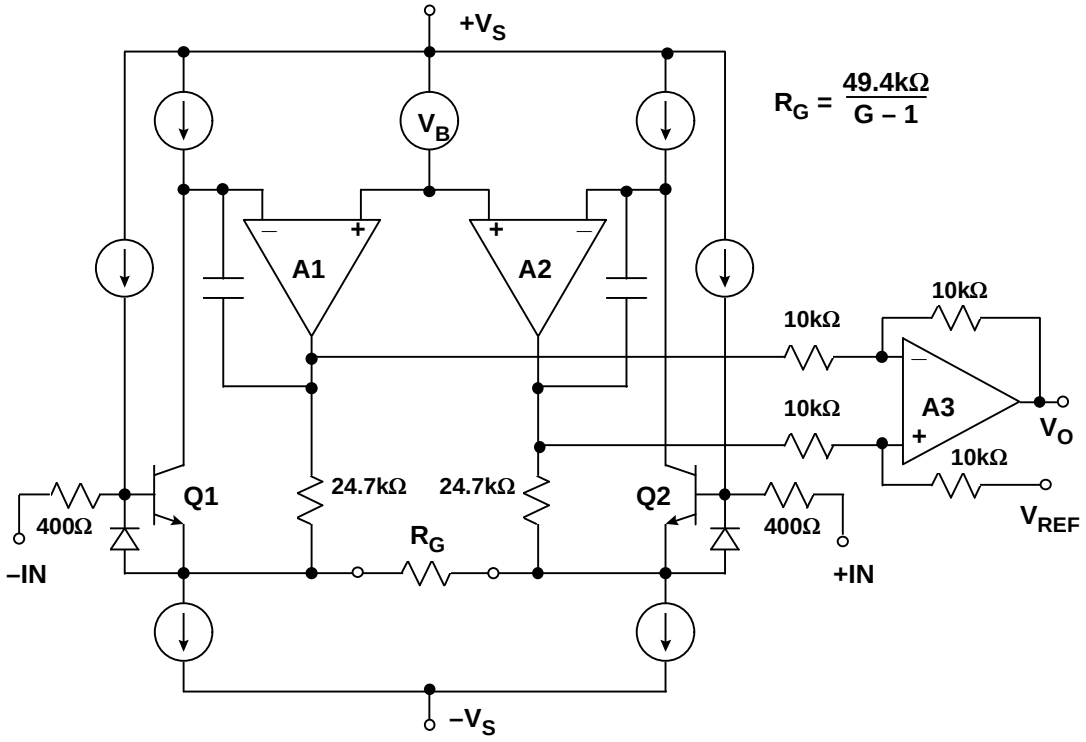


Figure 3.33

As in the case of the two op amp in-amp configuration, single supply operation of the three op amp in-amp requires an understanding of the internal node voltages. Figure 3.34 shows a generalized diagram of the in-amp operating on a single +5V supply. The maximum and minimum allowable output voltages of the individual op amps are designated V_{OH} (maximum high output) and V_{OL} (minimum low output) respectively. Note that the gain from the common mode voltage to the outputs of A1 and A2 is unity, and that *the sum of the common mode voltage and the signal voltage at these outputs must fall within the amplifier output voltage range.* It is obvious that this configuration cannot handle input common mode voltages of either zero volts or +5V because of saturation of A1 and A2. As in the case of the two op amp in-amp, the output reference is positioned halfway between V_{OH} and V_{OL} in order to allow for bipolar differential input signals.

This chapter has emphasized the operation of high performance linear circuits from a single, low-voltage supply (5V or less) is a common requirement. While there are many precision single supply operational amplifiers, such as the OP213, the OP291, and the OP284, and some good single-supply instrumentation amplifiers, the highest performance instrumentation amplifiers are still specified for dual-supply operation.

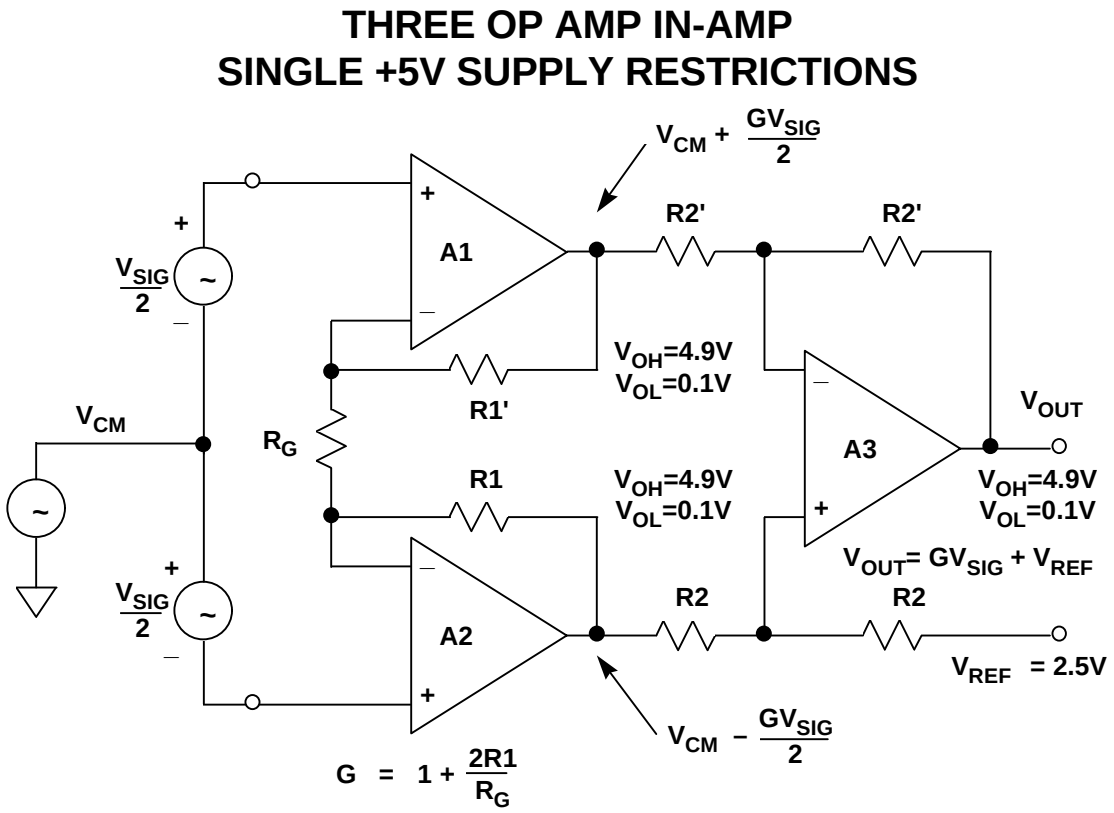


Figure 3.34

One way to achieve both high precision and single-supply operation takes advantage of the fact that several popular sensors (e.g. strain gauges) provide an output signal centered around the (approximate) mid-point of the supply voltage (or the reference voltage), where the inputs of the signal conditioning amplifier need not operate near "ground" or the positive supply voltage.

Under these conditions, a dual-supply instrumentation amplifier referenced to the supply mid-point followed by a "rail-to-rail" operational amplifier gain stage provides very high DC precision. Figure 3.35 illustrates one such high-performance instrumentation amplifier operating on a single, +5V supply. This circuit uses an AD620 low-cost precision instrumentation amplifier for the input stage, and an AD822 JFET-input dual rail-to-rail output operational amplifier for the output stage.

In this circuit, R3 and R4 form a voltage divider which splits the supply voltage in half to +2.5V, with fine adjustment provided by a trimming potentiometer, P1. This voltage is applied to the input of A1, an AD822 which buffers it and provides a low-impedance source needed to drive the AD620's reference pin. The AD620's Reference pin has a 10kΩ input resistance and an input signal current of up to 200μA. The other half of the AD822 is connected as a gain-of-3 inverter, so that it can output ±2.5V, "rail-to-rail," with only ±0.83V required of the AD620. This output voltage

level of the AD620 is well within the AD620's capability, thus ensuring high linearity for the "dual-supply" front end. *Note that the final output voltage must be measured with respect to the +2.5V reference, and not to GND.*

A PRECISION SINGLE-SUPPLY COMPOSITE IN-AMP WITH RAIL-TO-RAIL OUTPUT

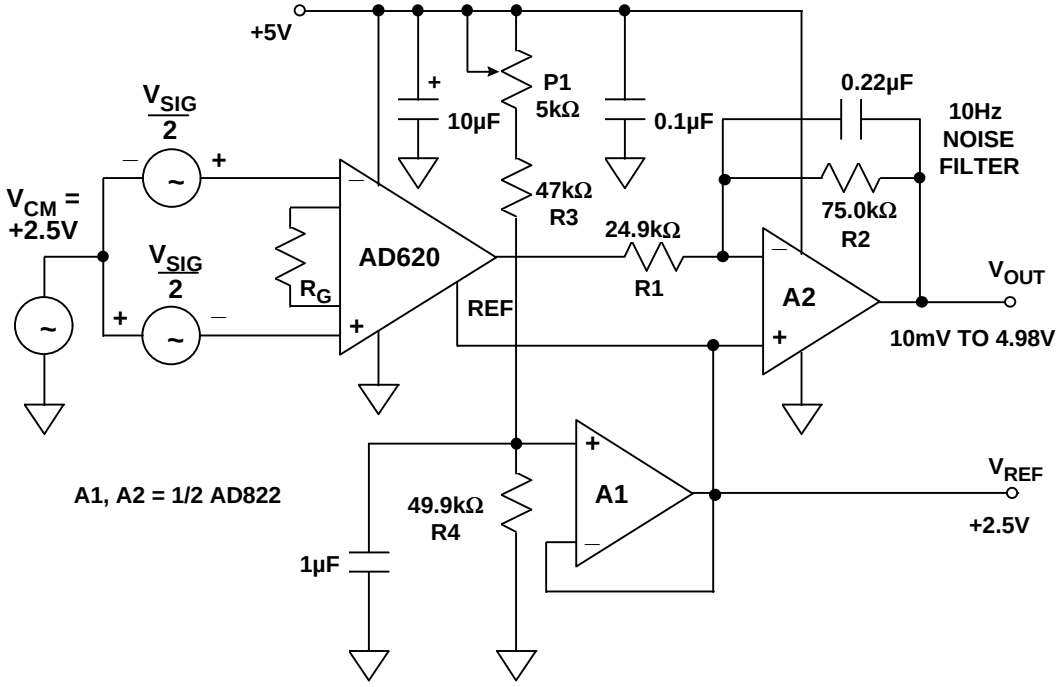


Figure 3.35

The general gain expression for this composite instrumentation amplifier is the product of the AD620 and the inverting amplifier gains:

$$\text{GAIN} = \left(\frac{49.4\,\text{k}\Omega}{\text{R}_\text{G}} + 1\right)\left(\frac{\text{R2}}{\text{R1}}\right).$$

For this example, an overall gain of 10 is realized with R_G = 21.5kΩ (closest standard value). The table (Figure 3.36) summarizes various R_G/gain values and performance.

In this application, the allowable input voltage on either input to the AD620 must lie between +2V and +3.5V in order to maintain linearity. For example, at an overall circuit gain of 10, the common mode input voltage range spans 2.25V to 3.25V, allowing room for the ±0.25V full-scale differential input voltage required to drive the output ±2.5V about V_{REF}.

The inverting configuration was chosen for the output buffer to facilitate system output offset voltage adjustment by summing currents into the A2 stage buffer's feedback summing node. These offset currents can be provided by an external DAC, or from a resistor connected to a reference voltage.

The AD822 rail-to-rail output stage exhibits a very clean transient response (not shown) and a small-signal bandwidth over 100kHz for gain configurations up to 300. Note that excellent linearity is maintained over 0.1V to 4.9V V_{OUT}. To reduce the effects of unwanted noise pickup, a capacitor is recommended across A2's feedback resistance to limit the circuit bandwidth to the frequencies of interest.

PERFORMANCE SUMMARY OF THE +5V SINGLE-SUPPLY AD620/AD822 COMPOSITE IN-AMP

CIRCUIT GAIN	R_G (Ω)	V_{OS}, RTI (µV)	TC V_{OS}, RTI (µV/°C)	NONLINEARITY (ppm) *	BANDWIDTH (kHz)**
10	21.5k	1000	1000	< 50	600
30	5.49k	430	430	< 50	600
100	1.53k	215	215	< 50	300
300	499	150	150	< 50	120
1000	149	150	150	< 50	30

*** Nonlinearity Measured Over Output Range: 0.1V < V_{OUT} < 4.90V**
**** Without 10Hz Noise Filter**

Figure 3.36

In cases where zero-volt inputs are required, the AD623 single supply in-amp configuration shown in Figure 3.37 offers an attractive solution. The PNP emitter follower level shifters, Q1/Q2, allow the input signal to go 150mV below the negative supply and to within 1.5V of the positive supply. The AD623 is fully specified for single power supplies between +3V and +12V and dual supplies between ±2.5V and ±6V (see Figure 3.38). The AD623 data sheet (available at http://www.analog.com) contains an excellent discussion of allowable input/output voltage ranges as a function of gain and power supply voltages.

AD623 SINGLE-SUPPLY IN-AMP ARCHITECTURE

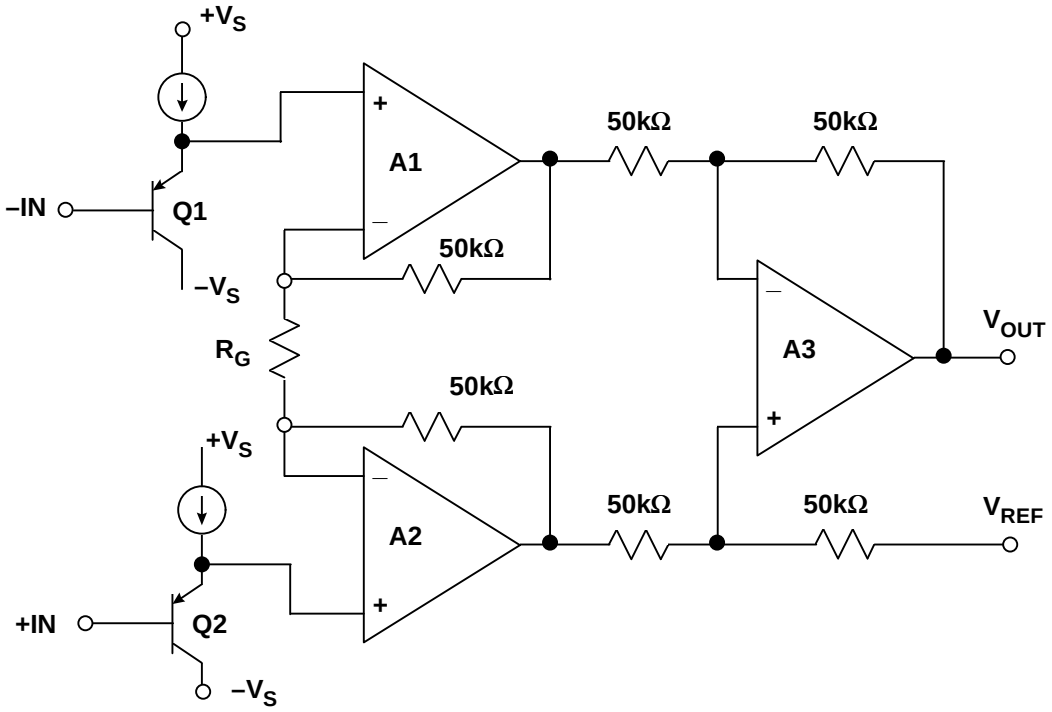


Figure 3.37

AD623 IN-AMP KEY SPECIFICATIONS

- Wide Supply Range: +3V to ±6V
- Input Voltage Range: $-V_S - 0.15V$ to $+V_S - 1.5V$
- 575µA Maximum Supply Current
- Gain Range: 1 to 1000
- 100µV Maximum Input Offset Voltage (AD623B)
- 1µV/°C Maximum Offset Voltage TC (AD623B)
- 50ppm Gain Nonlinearity
- 105dB CMR @ 60Hz, 1kΩ Source Imbalance, G ≥ 100
- 3µV p-p 0.1Hz to 10Hz Input Voltage Noise (G = 1)

Figure 3.38

Instrumentation Amplifier DC Error Sources

The DC and noise specifications for instrumentation amplifiers differ slightly from conventional op amps, so some discussion is required in order to fully understand the error sources.

The gain of an in-amp is usually set by a single resistor. If the resistor is external to the in-amp, its value is either calculated from a formula or chosen from a table on the data sheet, depending on the desired gain.

Absolute value laser wafer trimming allows the user to program gain accurately with this single resistor. The absolute accuracy and temperature coefficient of this resistor directly affects the in-amp gain accuracy and drift. Since the external resistor will never exactly match the internal thin film resistor tempcos, a low TC (<25ppm/°C) metal film resistor should be chosen, preferably with a 0.1% or better accuracy.

Often specified as having a gain range of 1 to 1000, or 1 to 10,000, many in-amps will work at higher gains, but the manufacturer will not guarantee a specific level of performance at these high gains. In practice, as the gain-setting resistor becomes smaller, any errors due to the resistance of the metal runs and bond wires become significant. These errors, along with an increase in noise and drift, may make higher single-stage gains impractical. In addition, input offset voltages can become quite sizable when reflected to output at high gains. For instance, a 0.5mV input offset voltage becomes 5V at the output for a gain of 10,000. For high gains, the best practice is to use an instrumentation amplifier as a preamplifier then use a post amplifier for further amplification.

In a pin-programmable gain in-amp such as the AD621, the gain setting resistors are internal, well matched, and the gain accuracy and gain drift specifications include their effects. The AD621 is otherwise generally similar to the externally gain-programmed AD620.

The *gain error* specification is the maximum deviation from the gain equation. Monolithic in-amps such as the AD624C have very low factory trimmed gain errors, with its maximum error of 0.02% at G = 1 and 0.25% at G = 500 being typical for this high quality in-amp. Notice that the gain error increases with increasing gain. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of the external resistors and the temperature differences between individual resistors within the network all contribute to the overall gain error. If the data is eventually digitized and presented to a digital processor, it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

Nonlinearity is defined as the maximum deviation from a straight line on the plot of output versus input. The straight line is drawn between the end-points of the actual transfer function. Gain nonlinearity in a high quality in-amp is usually 0.01% (100ppm) or less, and is relatively insensitive to gain over the recommended gain range.

The total input offset voltage of an in-amp consists of two components (see Figure 3.39). Input offset voltage, V_{OSI}, is that component of input offset which is reflected to the output of the in-amp by the gain G. Output offset voltage, V_{OSO}, is independent of gain. At low gains, output offset voltage is dominant, while at high gains input offset dominates. The output offset voltage drift is normally specified as drift at G=1 (where input effects are insignificant), while input offset voltage drift is given by a drift specification at a high gain (where output offset effects are negligible). The total output offset error, referred to the input (RTI), is equal to $V_{OSI} + V_{OSO}/G$. In-amp data sheets may specify V_{OSI} and V_{OSO} separately or give the total RTI input offset voltage for different values of gain.

IN-AMP OFFSET VOLTAGE MODEL

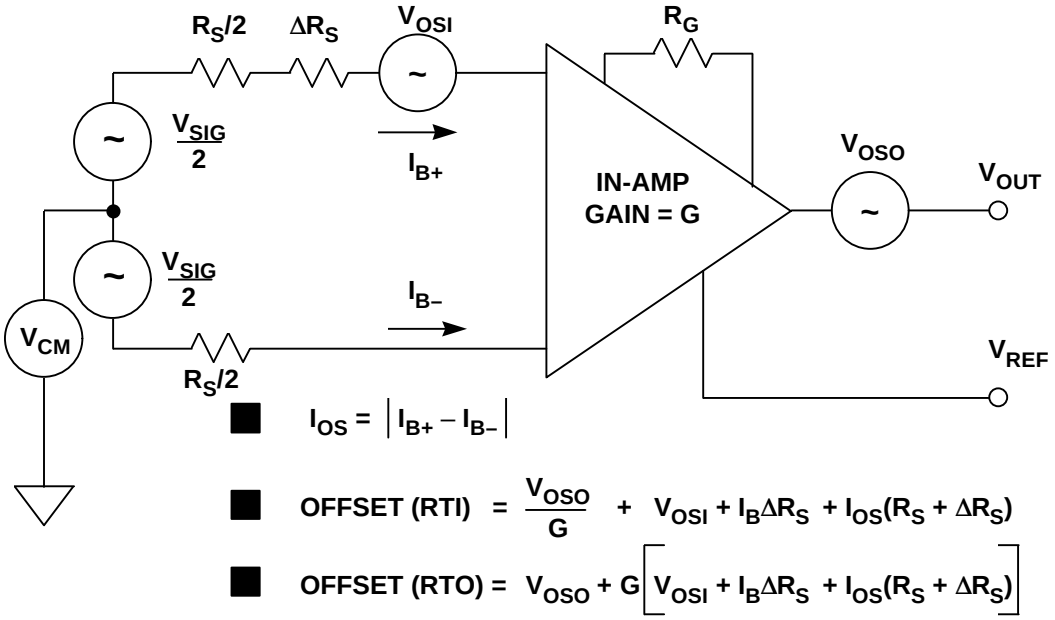


Figure 3.39

Input bias currents may also produce offset errors in in-amp circuits (see Figure 3.39). If the source resistance, R_S, is unbalanced by an amount, ΔR_S, (often the case in bridge circuits), then there is an additional input offset voltage error due to the bias current, equal to $I_B\Delta R_S$ (assuming that $I_{B+} \approx I_{B-} = I_B$). This error is reflected to the output, scaled by the gain G. The input offset current, I_{OS}, creates an input offset voltage error across the source resistance, $R_S+\Delta R_S$, equal to $I_{OS}(R_S+\Delta R_S)$, which is also reflected to the output by the gain, G.

In-amp common mode error is a function of both gain and frequency. Analog Devices specifies in-amp CMR for a 1kΩ source impedance unbalance at a frequency of 60Hz. The RTI common mode error is obtained by dividing the common mode voltage, V_{CM}, by the common mode rejection ratio, CMRR.

Power supply rejection (PSR) is also a function of gain and frequency. For in-amps, it is customary to specify the sensitivity to each power supply separately. Now that all DC error sources have been accounted for, a worst case DC error budget can be calculated by reflecting all the sources to the in-amp input (Figure 3.40).

INSTRUMENTATION AMPLIFIER AMPLIFIER DC ERRORS REFERRED TO THE INPUT (RTI)

ERROR SOURCE	RTI VALUE
Gain Accuracy (ppm)	Gain Accuracy × FS Input
Gain Nonlinearity (ppm)	Gain Nonlinearity × FS Input
Input Offset Voltage, V_{OSI}	V_{OSI}
Output Offset Voltage, V_{OSO}	$V_{OSO} \div G$
Input Bias Current, I_B, Flowing in ΔR_S	$I_B \Delta R_S$
Input Offset Current, I_{OS}, Flowing in R_S	$I_{OS}(R_S + \Delta R_S)$
Common Mode Input Voltage, V_{CM}	$V_{CM} \div CMRR$
Power Supply Variation, ΔV_S	$\Delta V_S \div PSRR$

Figure 3.40

Instrumentation Amplifier Noise Sources

Since in-amps are primarily used to amplify small precision signals, it is important to understand the effects of all the associated noise sources. The in-amp noise model is shown in Figure 3.41. There are two sources of input voltage noise. The first is represented as a noise source, V_{NI}, in series with the input, as in a conventional op amp circuit. This noise is reflected to the output by the in-amp gain, G. The second noise source is the output noise, V_{NO}, represented as a noise voltage in series with the in-amp output. The output noise, shown here referred to V_{OUT}, can be referred to the input by dividing by the gain, G.

There are two noise sources associated with the input noise currents I_{N+} and I_{N-}. Even though I_{N+} and I_{N-} are usually equal ($I_{N+} \approx I_{N-} = I_N$), they are uncorrelated, and therefore, the noise they each create must be summed in a root-sum-squares (RSS) fashion. I_{N+} flows through one half of R_S, and I_{N-} the other half. This generates two noise voltages, each having an amplitude, $I_N R_S/2$. Each of these two noise sources is reflected to the output by the in-amp gain, G.

The total output noise is calculated by combining all four noise sources in an RSS manner:

$$\text{NOISE (RTO)} = \sqrt{BW}\sqrt{V_{NO}^2 + G^2\left(V_{NI}^2 + \frac{I_{N+}^2 R_S^2}{4} + \frac{I_{N-}^2 R_S^2}{4}\right)} .$$

If $I_{N+} = I_{N-} = I_N$,

$$\text{NOISE (RTO)} = \sqrt{BW}\sqrt{V_{NO}^2 + G^2\left(V_{NI}^2 + \frac{I_N^2 R_S^2}{2}\right)}.$$

The total noise, referred to the input (RTI) is simply the above expression divided by the in-amp gain, G:

$$\text{NOISE (RTI)} = \sqrt{BW}\sqrt{\frac{V_{NO}^2}{G^2} + \left(V_{NI}^2 + \frac{I_N^2 R_S^2}{2}\right)}.$$

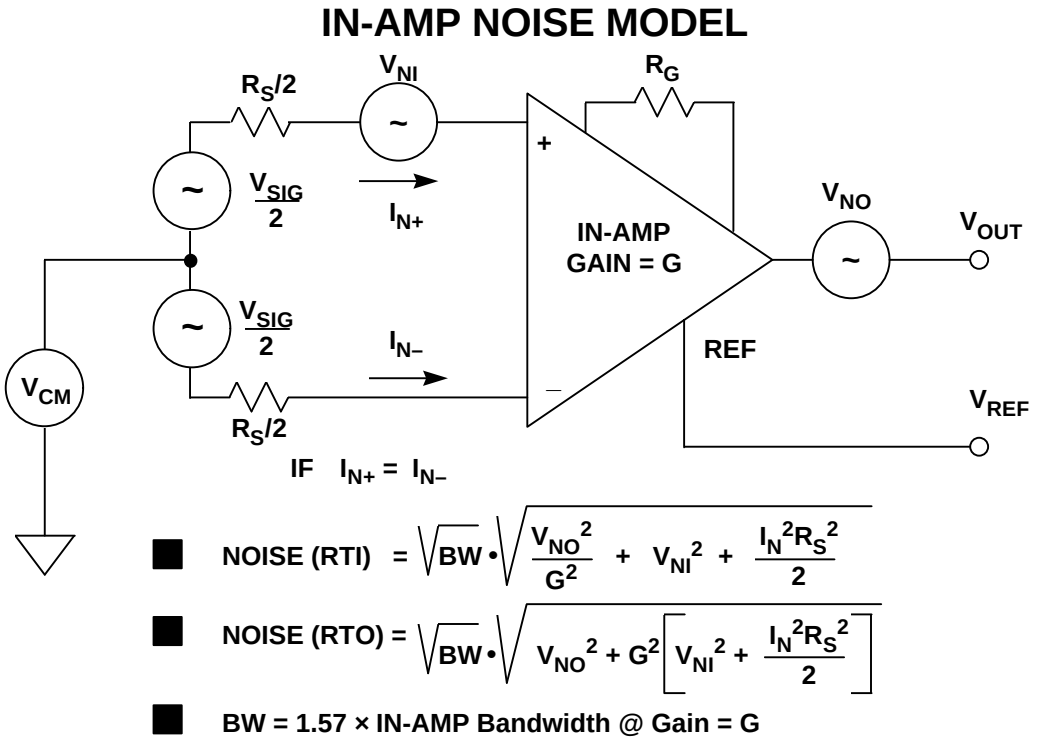


Figure 3.41

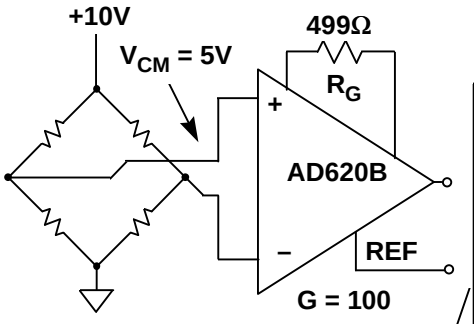
In-amp data sheets often present the total voltage noise RTI as a function of gain. This noise spectral density includes both the input (V_{NI}) and output (V_{NO}) noise contributions. The input current noise spectral density is specified separately. As in the case of op amps, the total noise RTI must be integrated over the in-amp closed-loop bandwidth to compute the RMS value. The bandwidth may be determined from data sheet curves which show frequency response as a function of gain.

In-Amp Bridge Amplifier Error Budget Analysis

It is important to understand in-amp error sources in a typical application. Figure 3.42 shows a 350Ω load cell which has a fullscale output of 100mV when excited with a 10V source. The AD620 is configured for a gain of 100 using the external 499Ω gain-setting resistor. The table shows how each error source contributes to the

total unadjusted error of 2145ppm. The gain, offset, and CMR errors can be removed with a system calibration. The remaining errors - gain nonlinearity and 0.1Hz to 10Hz noise - cannot be removed with calibration and limit the system resolution to 42.8ppm (approximately 14-bit accuracy).

AD620B BRIDGE AMPLIFIER DC ERROR BUDGET



AD620B SPECS @ +25°C, ±15V
V_{OSI} + V_{OSO}/G = 55µV max
I_{OS} = 0.5nA max
Gain Error = 0.15%
Gain Nonlinearity = 40ppm
0.1Hz to 10Hz Noise = 280nVp-p
CMR = 120dB @ 60Hz

MAXIMUM ERROR CONTRIBUTION, +25°C
FULLSCALE: V_{IN} = 100mV, V_{OUT} = 10V

V_{OS}	55µV ÷ 100mV	550ppm
I_{OS}	350Ω × 0.5nA ÷ 100mV	1.8ppm
Gain Error	0.15%	1500ppm
Gain Nonlinearity	40ppm	40ppm
CMR Error	120dB 1ppm × 5V ÷ 100mV	50ppm
0.1Hz to 10Hz 1/f Noise	280nV ÷ 100mV	2.8ppm
Total Unadjusted Error	≈ 9 Bits Accurate	2145ppm
Resolution Error	≈ 14 Bits Accurate	42.8ppm

Figure 3.42

In-Amp Performance Tables

Figure 3.43 shows a selection of precision in-amps designed primarily for operation on dual supplies. It should be noted that the AD620 is capable of single +5V supply operation (see Figure 3.35), but neither its input nor its output are capable of rail-to-rail swings.

Instrumentation amplifiers specifically designed for single supply operation are shown in Figure 3.44. It should be noted that although the specifications in the figure are given for a single +5V supply, all of the amplifiers are also capable of dual supply operation and are specified for both dual and single supply operation on their data sheets. In addition, the AD623 and AD627 will operate on a single +3V supply.

The AD626 is not a true in-amp but is a differential amplifier with a thin-film input attenuator which allows the common mode voltage to exceed the supply voltages. This device is designed primarily for high and low-side current-sensing applications. It will also operate on a single +3V supply.

PRECISION IN-AMPS: DATA FOR V_S = ±15V, G = 1000

	Gain Accuracy *	Gain Nonlinearity	V_{OS} Max	V_{OS} TC	CMR Min	0.1Hz to 10Hz p-p Noise
AD524C	0.5% / P	100ppm	50µV	0.5µV/°C	120dB	0.3µV
AD620B	0.5% / R	40ppm	50µV	0.6µV/°C	120dB	0.28µV
AD621B[1]	0.05% / P	10ppm	50µV	1.6µV/°C	100dB	0.28µV
AD622	0.5% / R	40ppm	125µV	1µV/°C	103dB	0.3µV
AD624C[2]	0.25% / R	50ppm	25µV	0.25µV/°C	130dB	0.2µV
AD625C	0.02% / R	50ppm	25µV	0.25µV/°C	125dB	0.2µV
AMP01A	0.6% / R	50ppm	50µV	0.3µV/°C	125dB	0.12µV
AMP02E	0.5% / R	60ppm	100µV	2µV/°C	115dB	0.4µV

* / P = Pin Programmable
* / R = Resistor Programmable

[1] G = 100
[2] G = 500

Figure 3.43

SINGLE SUPPLY IN-AMPS: DATA FOR V_S = +5V, G = 1000

	Gain Accuracy *	Gain Nonlinearity	V_{OS} Max	V_{OS} TC	CMR Min	0.1Hz to 10Hz p-p Noise	Supply Current
AD623B	0.5% / R	50ppm	100µV	1µV/°C	105dB	1.5µV	575µA
AD627B	0.35% / R	10ppm	75µV	1µV/°C	85dB	1.5µV	85µA
AMP04E	0.4% / R	250ppm	150µV	3µV/°C	90dB	0.7µV	290µA
AD626B[1]	0.6% / P	200ppm	2.5mV	6µV/°C	80dB	2µV	700µA

* / P = Pin Programmable
* / R = Resistor Programmable

[1] Differential Amplifier, G = 100

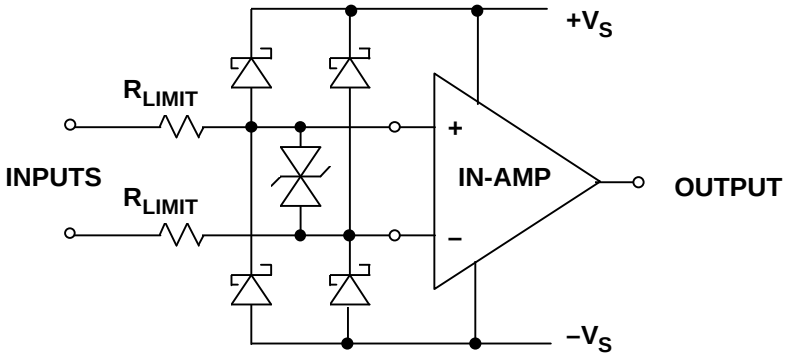
Figure 3.44

In-Amp Input Overvoltage Protection

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. The manufacturer's "absolute maximum" input ratings for the device should be closely observed. As with op amps, many in-amps have absolute maximum input voltage specifications equal to $\pm V_S$. External series resistors (for current limiting) and Schottky diode clamps may be used to prevent overload, if necessary. Some instrumentation amplifiers have built-in overload protection circuits in the form of series resistors (thin film) or series-protection FETs. In-amps such as the AMP-02 and the AD524 utilize series-protection FETs, because they act as a low impedance during normal operation, and a high impedance during fault conditions.

An additional Transient Voltage Suppresser (TVS) may be required across the input pins to limit the maximum differential input voltage. This is especially applicable to three op amp in-amps operating at high gain with low values of R_G. A more detailed discussion of input voltage and EMI/RFI protection can be found in Section 10 of this book.

INSTRUMENTATION AMPLIFIER
INPUT OVERVOLTAGE CONSIDERATIONS



- **Always Observe Absolute Maximum Data Sheet Specs!**
- **Schottky Diode Clamps to the Supply Rails Will Limit Input to Approximately $\pm V_S$ ±0.3V, TVSs Limit Differential Voltage**
- **External Resistors (or Internal Thin-Film Resistors) Can Limit Input Current, but will Increase Noise**
- **Some In-Amps Have Series-Protection Input FETs for Lower Noise and Higher Input Over-Voltages (up to ±60V, Depending on Device)**

Figure 3.45

CHOPPER STABILIZED AMPLIFIERS

For the lowest offset and drift performance, chopper-stabilized amplifiers may be the only solution. The best bipolar amplifiers offer offset voltages of 10µV and 0.1µV/ºC drift. Offset voltages less than 5µV with practically no measurable offset drift are obtainable with choppers, albeit with some penalties.

The basic chopper amplifier circuit is shown in Figure 3.46. When the switches are in the "Z" (auto-zero) position, capacitors C2 and C3 are charged to the amplifier input and output offset voltage, respectively. When the switches are in the "S" (sample) position, V_{IN} is connected to V_{OUT} through the path comprised of R1, R2, C2, the amplifier, C3, and R3. The chopping frequency is usually between a few hundred Hz and several kHz, and it should be noted that because this is a sampling system, the input frequency must be much less than one-half the chopping frequency in order to prevent errors due to aliasing. The R1/C1 combination serves as an antialiasing filter. It is also assumed that after a steady state condition is reached, there is only a minimal amount of charge transferred during the switching cycles. The output capacitor, C4, and the load, R_L, must be chosen such that there is minimal V_{OUT} droop during the auto-zero cycle.

CLASSIC CHOPPER AMPLIFIER

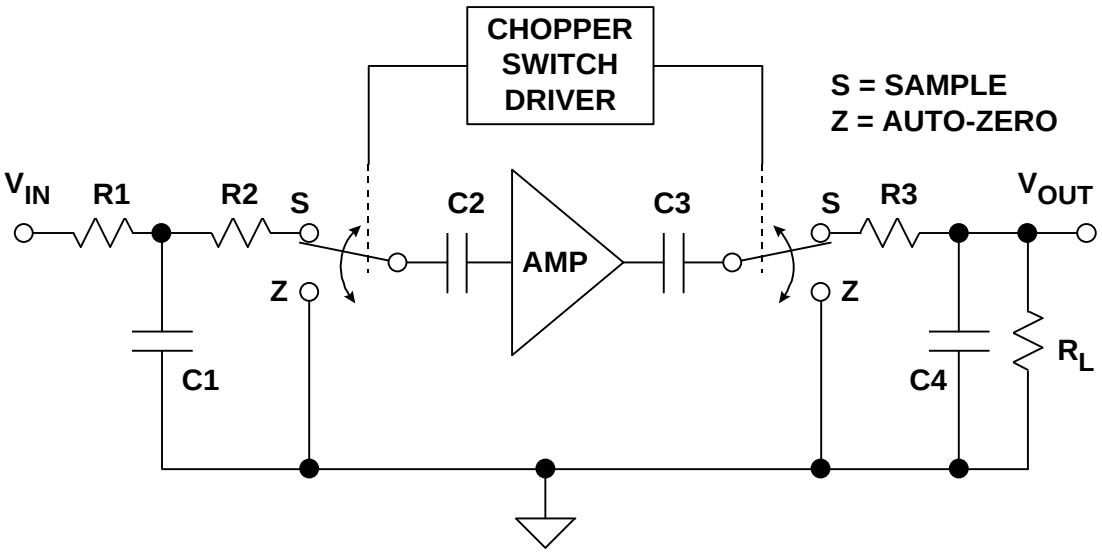


Figure 3.46

The basic chopper amplifier of Figure 3.46 can pass only very low frequencies because of the input filtering required to prevent aliasing. The *chopper-stabilized* architecture shown in Figure 3.47 is most often used in chopper amplifier implementations. In this circuit, A1 is the *main* amplifier, and A2 is the *nulling* amplifier. In the sample mode (switches in "S" position), the nulling amplifier, A2, monitors the input offset voltage of A1 and drives its output to zero by applying a suitable correcting voltage at A1's null pin. Note, however, that A2 also has an input offset voltage, so it must correct its own error before attempting to null A1's offset. This is achieved in the auto-zero mode (switches in "Z" position) by momentarily disconnecting A2 from A1, shorting its inputs together, and coupling its output to its own null pin. During the auto-zero mode, the correction voltage for A1 is momentarily held by C1. Similarly, C2 holds the correction voltage for A2 during the sample mode. In modern IC chopper-stabilized op amps, the storage capacitors C1 and C2 are on-chip.

CHOPPER STABILIZED AMPLIFIER

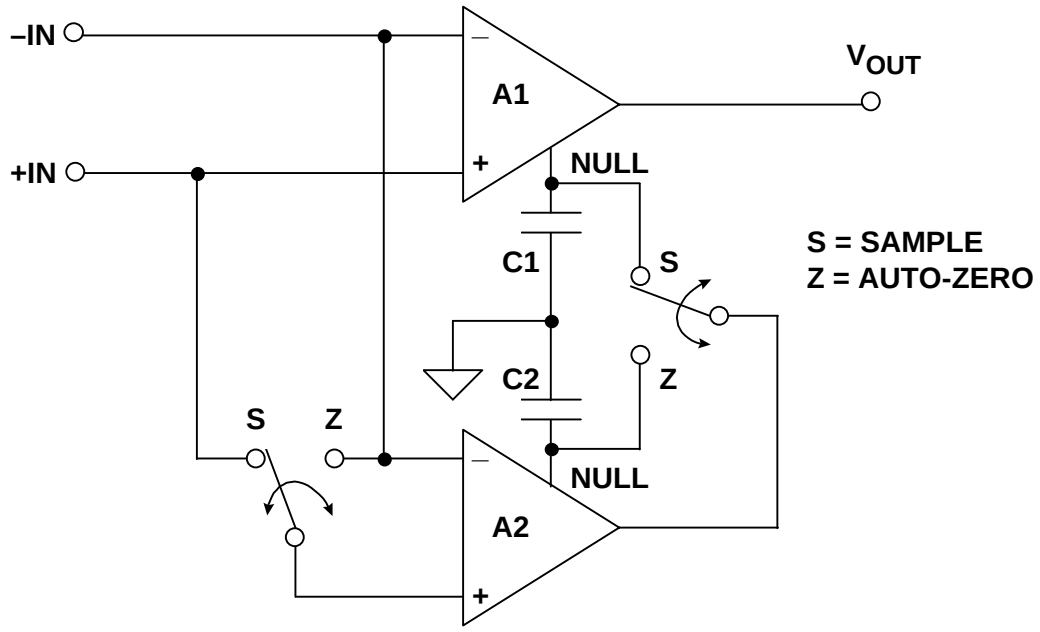
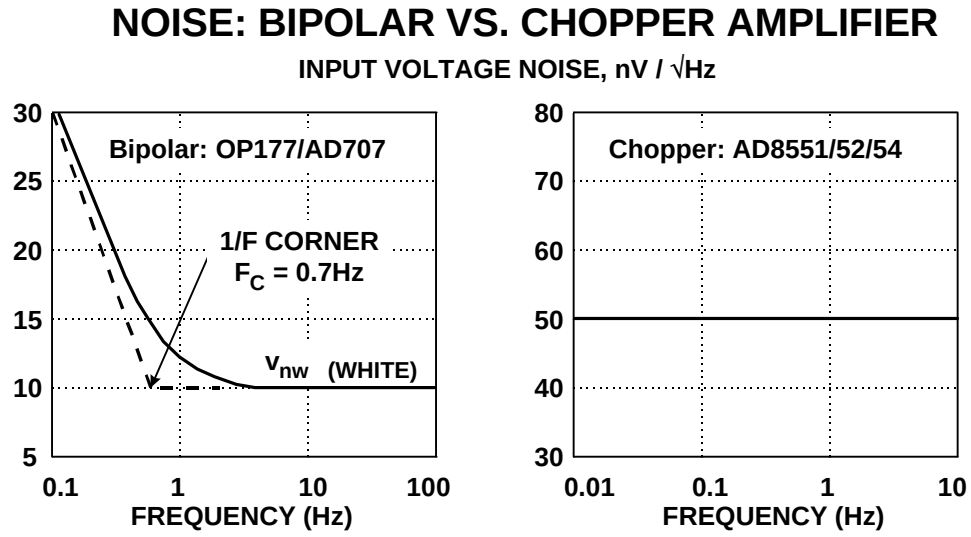


Figure 3.47

Note in this architecture that the input signal is always connected to the output through A1. The bandwidth of A1 thus determines the overall signal bandwidth, and the input signal is not limited to less than one-half the chopping frequency as in the case of the traditional chopper amplifier architecture. However, the switching action does produce small transients at the chopping frequency which can mix with the input signal frequency and produce in-band distortion.

It is interesting to consider the effects of a chopper amplifier on low frequency 1/f noise. If the chopping frequency is considerably higher than the 1/f corner frequency of the input noise, the chopper-stabilized amplifier continuously nulls out the 1/f noise on a sample-by-sample basis. Theoretically, a chopper op amp therefore has no 1/f noise. However, the chopping action produces wideband noise which is generally much worse than that of a precision bipolar op amp.

Figure 3.48 shows the noise of a precision bipolar amplifier (OP177/AD707) versus that of the AD8551/52/54 chopper-stabilized op amp. The peak-to-peak noise in various bandwidths is calculated for each in the table below the graphs. Note that as the frequency is lowered, the chopper amplifier noise continues to drop, while the bipolar amplifier noise approaches a limit determined by the 1/f corner frequency and its white noise (see Figure 3.9). At a very low frequency, the noise performance of the chopper is superior to that of the bipolar op amp.



NOISE BW	BIPOLAR (OP177/AD707)	CHOPPER (AD8551/52/54)
0.1Hz to 10Hz	0.238µV p-p	1.04 µV p-p
0.01Hz to 1Hz	0.135µV p-p	0.33µV p-p
0.001Hz to 0.1Hz	0.120µV p-p	0.104µV p-p
0.0001Hz to 0.01Hz	0.118µV p-p	0.033µV p-p

Figure 3.48

The AD8551/8552/8554 family of chopper-stabilized op amps offers rail-to-rail input and output single supply operation, low offset voltage, and low offset drift. The storage capacitors are internal to the IC, and no external capacitors other than standard decoupling capacitors are required. Key specifications for the devices are given in Figure 3.49. It should be noted that extreme care must be taken when applying these devices to avoid parasitic thermocouple effects in order to fully realize the offset and drift performance. A further discussion of parasitic thermocouples can be found in Section 10.

AD8551/52/54 CHOPPER STABILIZED RAIL-TO-RAIL INPUT/OUTPUT AMPLIFIERS

- **Single Supply: +3V to +5V**
- **5µV Max. Input Offset Voltage**
- **0.04µV/°C Input Offset Voltage Drift**
- **120dB CMR, PSR**
- **800µA Supply Current / Op Amp**
- **100µs Overload Recovery Time**
- **50nV/√Hz Input Voltage Noise**
- **1.5MHz Gain-Bandwidth Product**
- **Single (AD8551), Dual (AD8552) and Quad (AD8554)**

Figure 3.49

ISOLATION AMPLIFIERS

There are many applications where it is desirable, or even essential, for a sensor to have no direct ("galvanic") electrical connection with the system to which it is supplying data, either in order to avoid the possibility of dangerous voltages or currents from one half of the system doing damage in the other, or to break an intractable ground loop. Such a system is said to be "isolated", and the arrangement which passes a signal without galvanic connections is known as an "isolation barrier".

The protection of an isolation barrier works in both directions, and may be needed in either, or even in both. The obvious application is where a sensor may accidentally encounter high voltages, and the system it is driving must be protected. Or a sensor may need to be isolated from accidental high voltages arising downstream, in order to protect its environment: examples include the need to prevent the ignition of explosive gases by sparks at sensors and the protection from electric shock of patients whose ECG, EEG or EMG is being monitored. The ECG case is interesting, as protection may be required in *both* directions: the patient must be protected from accidental electric shock, but if the patient's heart should stop, the ECG machine must be protected from the very high voltages (>7.5 kV) applied to the patient by the defibrillator which will be used to attempt to restart it.

APPLICATIONS FOR ISOLATION AMPLIFIERS

- **Sensor is at a High Potential Relative to Other Circuitry (or may become so under Fault Conditions)**
- **Sensor May Not Carry Dangerous Voltages, Irrespective of Faults in Other Circuitry (e.g. Patient Monitoring and Intrinsically Safe Equipment for use with Explosive Gases)**
- **To Break Ground Loops**

Figure 3.50

Just as interference, or *unwanted* information, may be coupled by electric or magnetic fields, or by electromagnetic radiation, these phenomena may be used for the transmission of *wanted* information in the design of isolated systems. The most common isolation amplifiers use transformers, which exploit magnetic fields, and another common type uses small high voltage capacitors, exploiting electric fields. Opto-isolators, which consist of an LED and a photocell, provide isolation by using light, a form of electromagnetic radiation. Different isolators have differing performance: some are sufficiently linear to pass high accuracy analog signals across an isolation barrier, with others the signal may need to be converted to digital form before transmission, if accuracy is to be maintained, a common application for V/F converters.

Transformers are capable of analog accuracy of 12-16 bits and bandwidths up to several hundred kHz, but their maximum voltage rating rarely exceeds 10kV, and is often much lower. Capacitively coupled isolation amplifiers have lower accuracy, perhaps 12-bits maximum, lower bandwidth, and lower voltage ratings - but they are cheap. Optical isolators are fast and cheap, and can be made with very high voltage ratings (4 -7kV is one of the more common ratings), but they have poor analog domain linearity, and are not usually suitable for direct coupling of precision analog signals.

Linearity and isolation voltage are not the only issues to be considered in the choice of isolation systems. Power is essential. Both the input and the output circuitry must be powered, and unless there is a battery on the isolated side of the isolation barrier (which is possible, but rarely convenient), some form of isolated power must be provided. Systems using transformer isolation can easily use a transformer (either the signal transformer or another one) to provide isolated power, but it is impractical to transmit useful amounts of power by capacitive or optical means. Systems using these forms of isolation must make other arrangements to obtain isolated power supplies - this is a powerful consideration in favor of choosing transformer isolated isolation amplifiers: they almost invariably include an isolated power supply.

The isolation amplifier has an input circuit that is galvanically isolated from the power supply and the output circuit. In addition, there is minimal capacitance

between the input and the rest of the device. Therefore, there is no possibility for DC current flow, and minimum AC coupling. Isolation amplifiers are intended for applications requiring safe, accurate measurement of low frequency voltage or current (up to about 100kHz) in the presence of high common-mode voltage (to thousands of volts) with high common mode rejection. They are also useful for line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements, where DC and line-frequency leakage must be maintained at levels well below certain mandated minimums. Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process control systems.

In the basic two-port form, the output and power circuits are not isolated from one another. In the three-port isolator shown in Figure 3.51, the input circuits, output circuits, and power source are all isolated from one another. The figure shows the circuit architecture of a self-contained isolator, the AD210. An isolator of this type requires power from a two-terminal DC power supply. An internal oscillator (50kHz) converts the DC power to AC, which is transformer-coupled to the shielded input section, then converted to DC for the input stage and the auxiliary power output. The AC carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered, and buffered using isolated DC power derived from the carrier. The AD210 allows the user to select gains from 1 to 100 using an external resistor. Bandwidth is 20kHz, and voltage isolation is 2500V RMS (continuous) and ± 3500V peak (continuous).

AD210 3-PORT ISOLATION AMPLIFIER

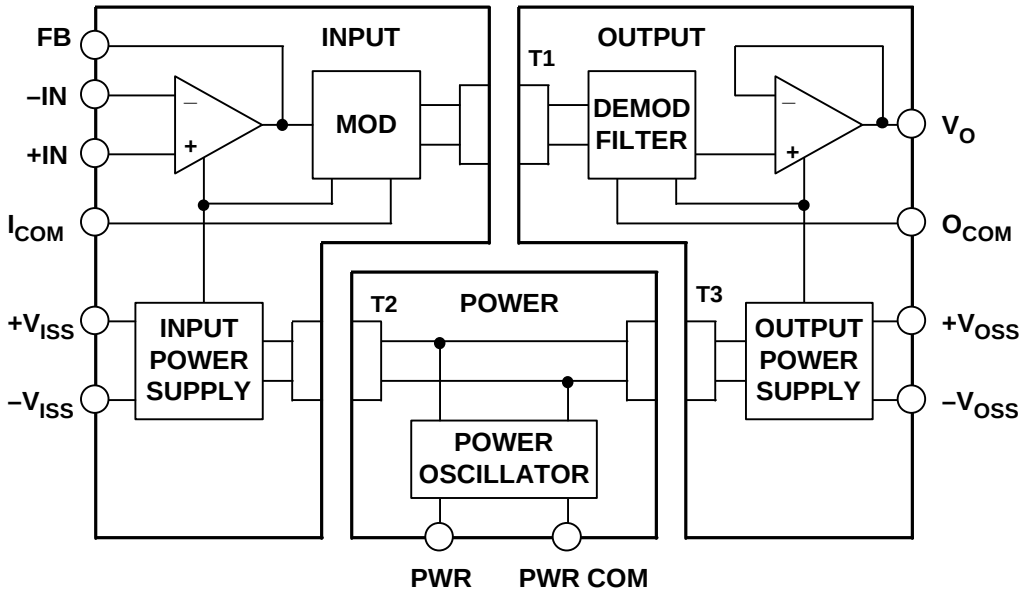


Figure 3.51

The AD210 is a 3-port isolation amplifier: the power circuitry is isolated from both the input and the output stages and may therefore be connected to either - or to neither. It uses transformer isolation to achieve 3500V isolation with 12-bit accuracy. Key specifications for the AD210 are summarized in Figure 3.52.

AD210 ISOLATION AMPLIFIER KEY FEATURES

- **Transformer Coupled**
- **High Common Mode Voltage Isolation:**
  - **2500V RMS Continuous**
  - **±3500V Peak Continuous**
- **Wide Bandwidth: 20kHz (Full Power)**
- **0.012% Maximum Linearity Error**
- **Input Amplifier: Gain 1 to 100**
- **Isolated Input and Output Power Supplies, ±15V, ±5mA**

Figure 3.52

A typical isolation amplifier application using the AD210 is shown in Figure 3.53. The AD210 is used with an AD620 instrumentation amplifier in a current-sensing system for motor control. The input of the AD210, being isolated, can be connected to a 110 or 230 V power line without any protection, and the isolated ±15 V powers the AD620, which senses the voltage drop in a small current sensing resistor. The 110 or 230V RMS common-mode voltage is ignored by the isolated system. The AD620 is used to improve system accuracy: the V_{OS} of the AD210 is 15mV, while the AD620 has V_{OS} of 30μV and correspondingly lower drift. If higher DC offset and drift are acceptable, the AD620 may be omitted, and the AD210 used directly at a closed loop gain of 100.

MOTOR CONTROL CURRENT SENSING

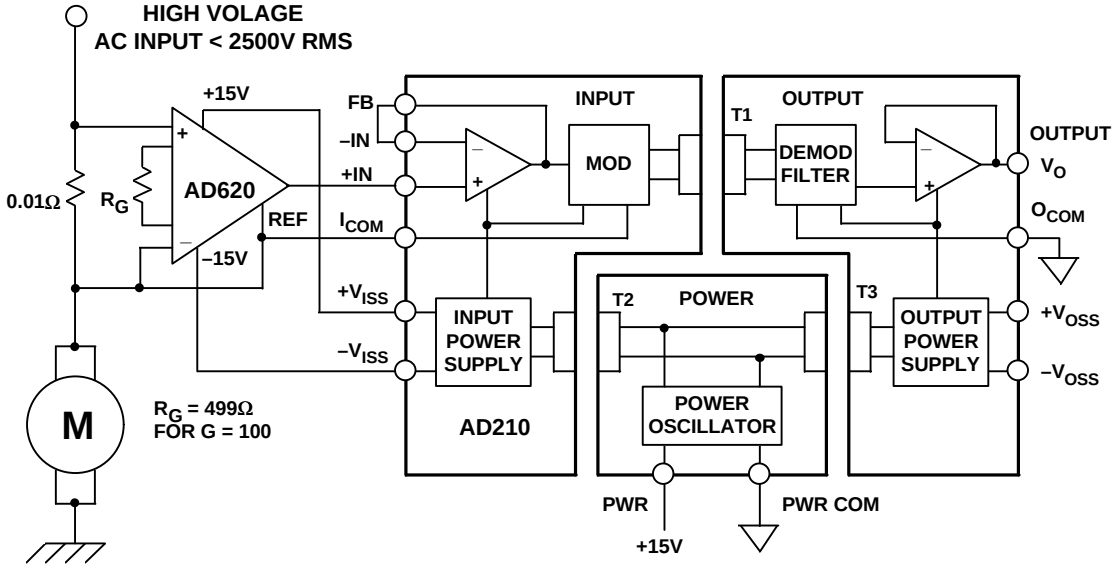


Figure 3.53

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SECTION 4
STRAIN, FORCE, PRESSURE, AND FLOW MEASUREMENTS

Walt Kester

STRAIN GAGES

The most popular electrical elements used in force measurements include the resistance strain gage, the semiconductor strain gage, and piezoelectric transducers. The strain gage measures force indirectly by measuring the deflection it produces in a calibrated carrier. Pressure can be converted into a force using an appropriate transducer, and strain gage techniques can then be used to measure pressure. Flow rates can be measured using differential pressure measurements which also make use of strain gage technology.

STRAIN GAGE BASED MEASUREMENTS

- **Strain:** **Strain Gage, PiezoElectric Transducers**
- **Force:** **Load Cell**
- **Pressure:** **Diaphragm to Force to Strain Gage**
- **Flow:** **Differential Pressure Techniques**

Figure 4.1

The resistance strain gage is a resistive element which changes in length, hence resistance, as the force applied to the base on which it is mounted causes stretching or compression. It is perhaps the most well known transducer for converting force into an electrical variable.

Unbonded strain gages consist of a wire stretched between two points as shown in Figure 4.2. Force acting on the wire (area = A, length = L, resistivity = ρ) will cause the wire to elongate or shorten, which will cause the resistance to increase or decrease proportionally according to:

$$R = \rho L/A$$

and

$$\Delta R/R = GF \cdot \Delta L/L,$$

where GF = Gage factor (2.0 to 4.5 for metals, and more than 150 for semiconductors).

The dimensionless quantity $\Delta L/L$ is a measure of the force applied to the wire and is expressed in *microstrains* ($1\mu\varepsilon = 10^{-6}$ cm/cm) which is the same as parts-per-million (ppm). From this equation, note that larger gage factors result in proportionally larger resistance changes, hence, more sensitivity.

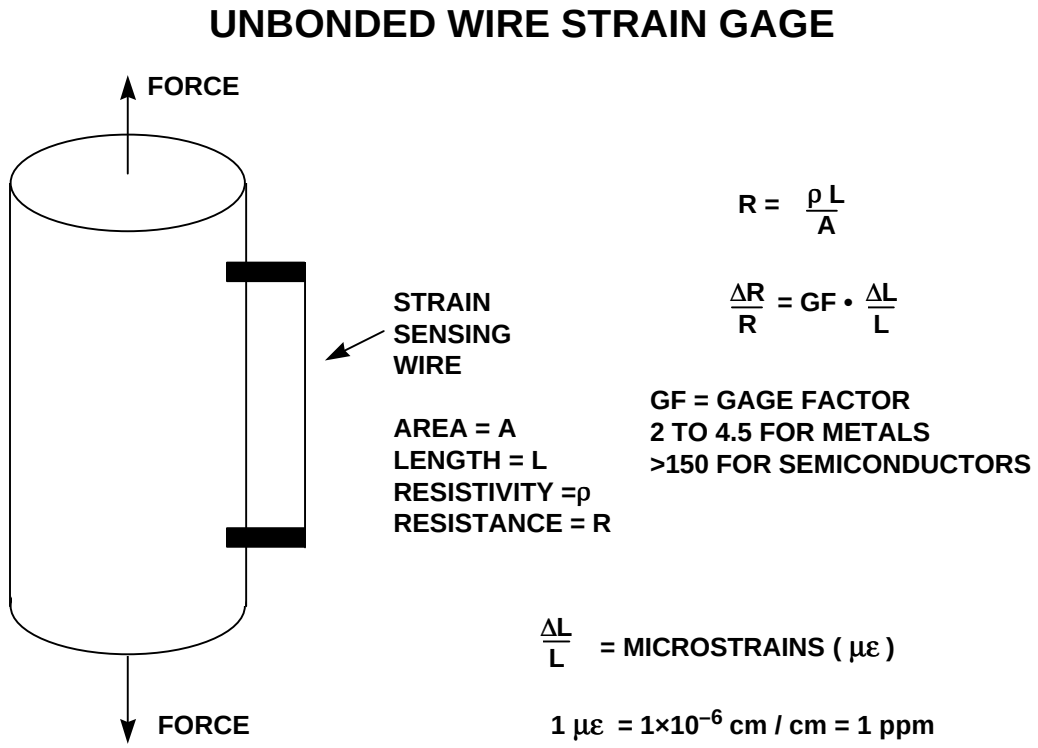
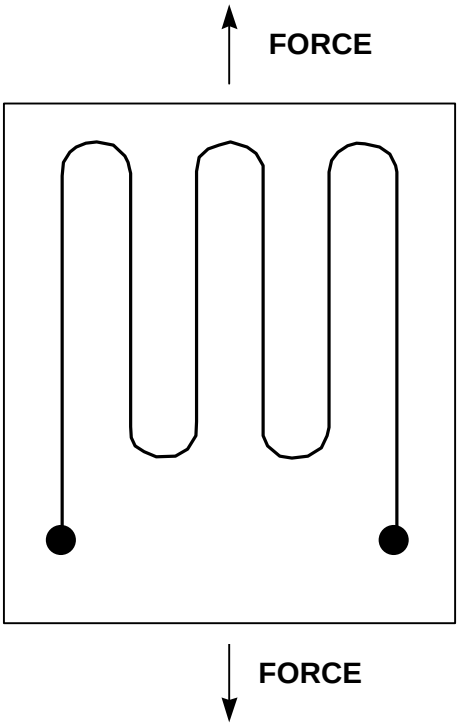


Figure 4.2

Bonded strain gages consist of a thin wire or conducting film arranged in a coplanar pattern and cemented to a base or carrier. The gage is normally mounted so that as much as possible of the length of the conductor is aligned in the direction of the stress that is being measured. Lead wires are attached to the base and brought out for interconnection. Bonded devices are considerably more practical and are in much wider use than unbonded devices.

Perhaps the most popular version is the foil-type gage, produced by photo-etching techniques, and using similar metals to the wire types (alloys of copper-nickel (Constantan), nickel-chromium (Nichrome), nickel-iron, platinum-tungsten, etc. (see Figure 4.4). Gages having wire sensing elements present a small surface area to the specimen; this reduces leakage currents at high temperatures and permits higher isolation potentials between the sensing element and the specimen. Foil sensing elements, on the other hand, have a large ratio of surface area to cross-sectional area and are more stable under extremes of temperature and prolonged loading. The large surface area and thin cross section also permit the device to follow the specimen temperature and facilitate the dissipation of self-induced heat.

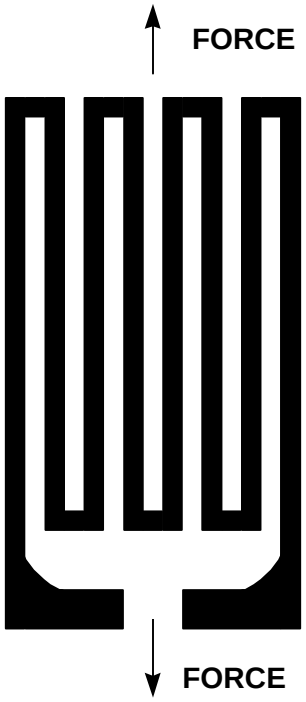
BONDED WIRE STRAIN GAGE



- SMALL SURFACE AREA
- LOW LEAKAGE
- HIGH ISOLATION

Figure 4.3

METAL FOIL STRAIN GAGE



- PHOTO ETCHING TECHNIQUE
- LARGE AREA
- STABLE OVER TEMPERATURE
- THIN CROSS SECTION
- GOOD HEAT DISSIPATION

Figure 4.4

Semiconductor strain gages make use of the piezoresistive effect in certain semiconductor materials such as silicon and germanium in order to obtain greater sensitivity and higher-level output. Semiconductor gages can be produced to have either positive or negative changes when strained. They can be made physically small while still maintaining a high nominal resistance. Semiconductor strain gage bridges may have 30 times the sensitivity of bridges employing metal films, but are temperature sensitive and difficult to compensate. Their change in resistance with strain is also nonlinear. They are not in as widespread use as the more stable metal-film devices for precision work; however, where sensitivity is important and temperature variations are small, they may have some advantage. Instrumentation is similar to that for metal-film bridges but is less critical because of the higher signal levels and decreased transducer accuracy.

COMPARISON BETWEEN METAL AND SEMICONDUCTOR STRAIN GAGES

PARAMETER	METAL STRAIN GAGE	SEMICONDUCTOR STRAIN GAGE
Measurement Range	0.1 to 40,000 με	0.001 to 3000 με
Gage Factor	2.0 to 4.5	50 to 200
Resistance, Ω	120, 350, 600, …, 5000	1000 to 5000
Resistance Tolerance	0.1% to 0.2%	1% to 2%
Size, mm	0.4 to 150 Standard: 3 to 6	1 to 5

Figure 4.5

Piezoelectric force transducers are employed where the forces to be measured are dynamic (i.e., continually changing over the period of interest - usually of the order of milliseconds). These devices utilize the effect that changes in charge are produced in certain materials when they are subjected to physical stress. In fact, piezoelectric transducers are *displacement* transducers with quite large charge outputs for very small displacements, but they are invariably used as force transducers on the assumption that in an elastic material, displacement is proportional to force. Piezoelectric devices produce substantial output voltage in instruments such as accelerometers for vibration studies. Output impedance is high, and charge amplifier configurations, with low input capacitance, are required for signal conditioning. Conditioning a piezoelectric sensor output is discussed in further detail in Section 5.

Strain gages can be used to measure force, as in Figure 4.6 where a cantilever beam is slightly deflected by the applied force. Four strain gages are used to measure the flex of the beam, two on the top side, and two on the bottom side. The gages are connected in an all-element bridge configuration. Recall from Section 2 that this configuration gives maximum sensitivity and is inherently linear. This configuration also offers first-order correction for temperature drift in the individual strain gages.

STRAIN GAGE BEAM FORCE SENSOR

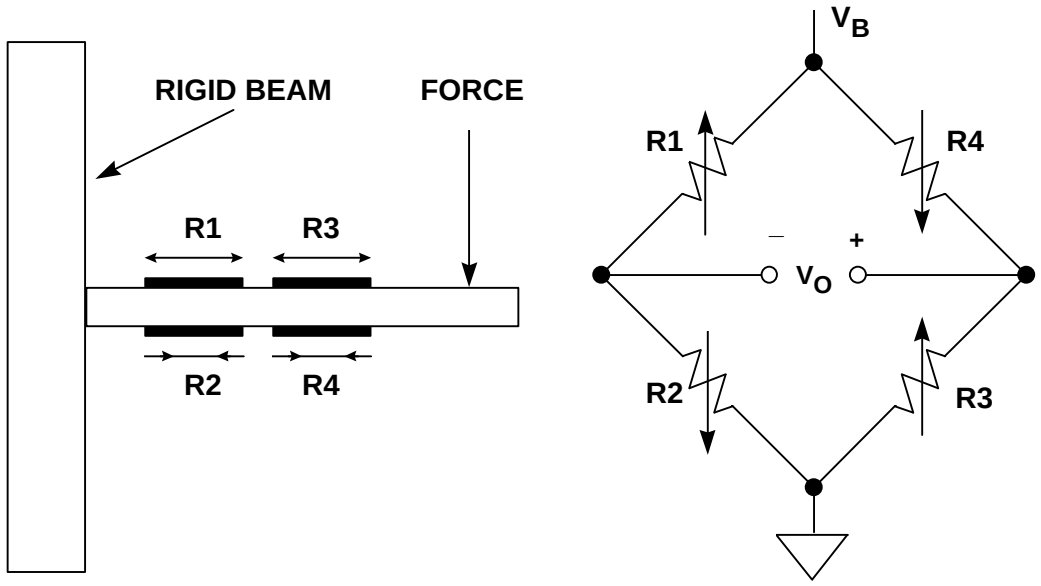


Figure 4.6

Strain gages are low-impedance devices; they require significant excitation power to obtain reasonable levels of output voltage. A typical strain-gage based load cell bridge will have (typically) a 350Ω impedance and is specified as having a sensitivity in terms of millivolts full scale per volt of excitation. The load cell is composed of four individual strain gages arranged as a bridge as shown in Figure 4.7. For a 10V bridge excitation voltage with a rating of 3mV/V, 30 millivolts of signal will be available at full scale loading. The output can be increased by increasing the drive to the bridge, but self-heating effects are a significant limitation to this approach: they can cause erroneous readings or even device destruction. Many load cells have "sense" connections to allow the signal conditioning electronics to compensate for DC drops in the wires. Some load cells have additional internal resistors which are selected for temperature compensation.

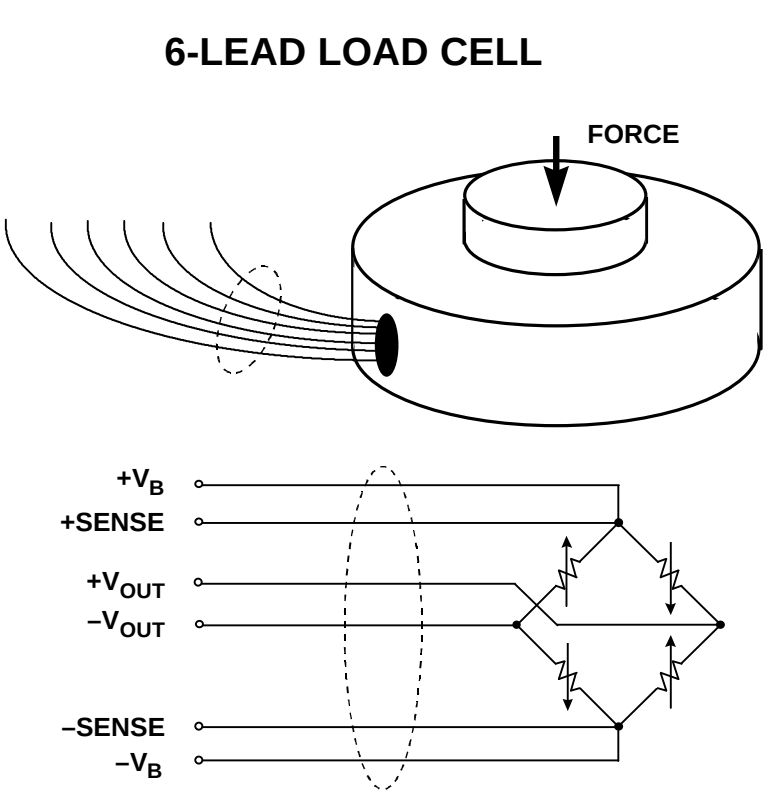


Figure 4.7

Pressures in liquids and gases are measured electrically by a variety of pressure transducers. A variety of mechanical converters (including diaphragms, capsules, bellows, manometer tubes, and Bourdon tubes) are used to measure pressure by measuring an associated length, distance, or displacement, and to measure pressure changes by the motion produced.

The output of this mechanical interface is then applied to an electrical converter such as a strain gage or piezoelectric transducer. Unlike strain gages, piezoelectric pressure transducers are typically used for high-frequency pressure measurements (such as sonar applications or crystal microphones).

PRESSURE SENSORS

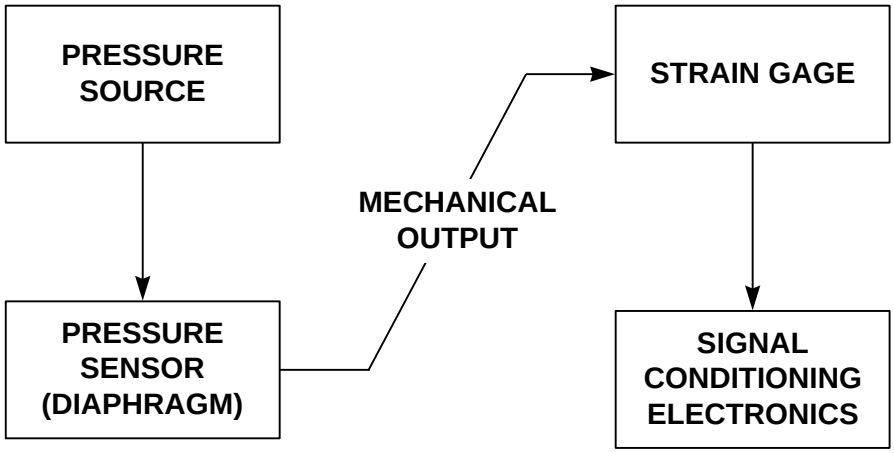


Figure 4.8

There are many ways of defining flow (mass flow, volume flow, laminar flow, turbulent flow). Usually the *amount* of a substance flowing (mass flow) is the most important, and if the fluid's density is constant, a volume flow measurement is a useful substitute that is generally easier to perform. One commonly used class of transducers, which measure flow rate indirectly, involves the measurement of pressure.

Flow can be derived by taking the differential pressure across two points in a flowing medium - one at a static point and one in the flow stream. *Pitot tubes* are one form of device used to perform this function. The flow rate is obtained by measuring the differential pressure with standard pressure transducers as shown in Figure 4.9. Differential pressure can also be used to measure flow rate using the *venturi* effect by placing a restriction in the flow as shown in Figure 4.10. Figure 4.11 shows a bending vane with an attached strain gage placed in the flow to measure flow rate.

PITOT TUBE USED TO MEASURE FLOW RATE

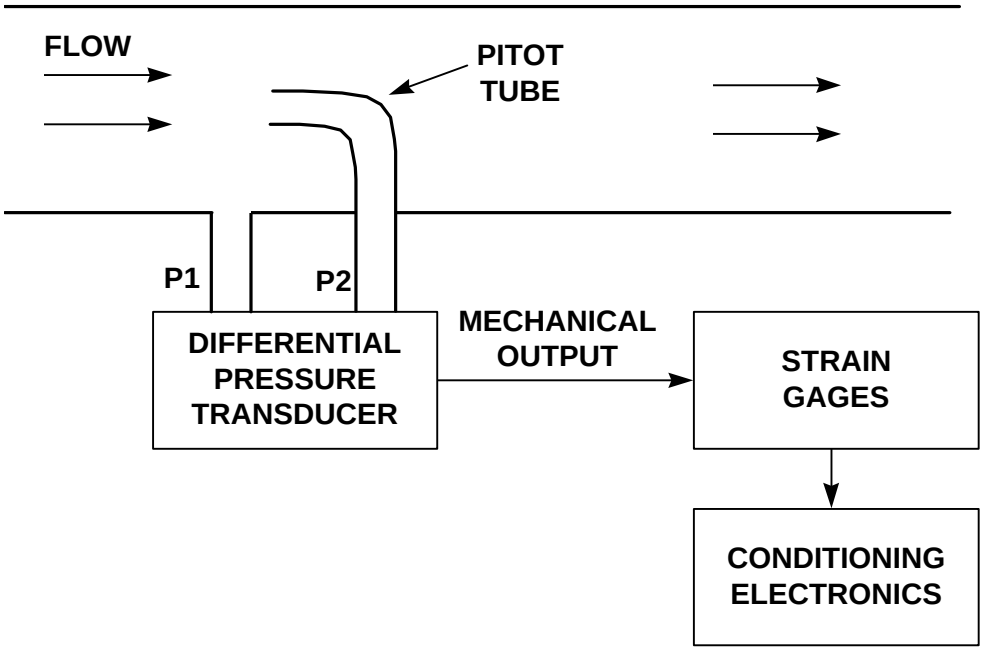


Figure 4.9

MEASURING FLOW RATE USING THE VENTURI EFFECT

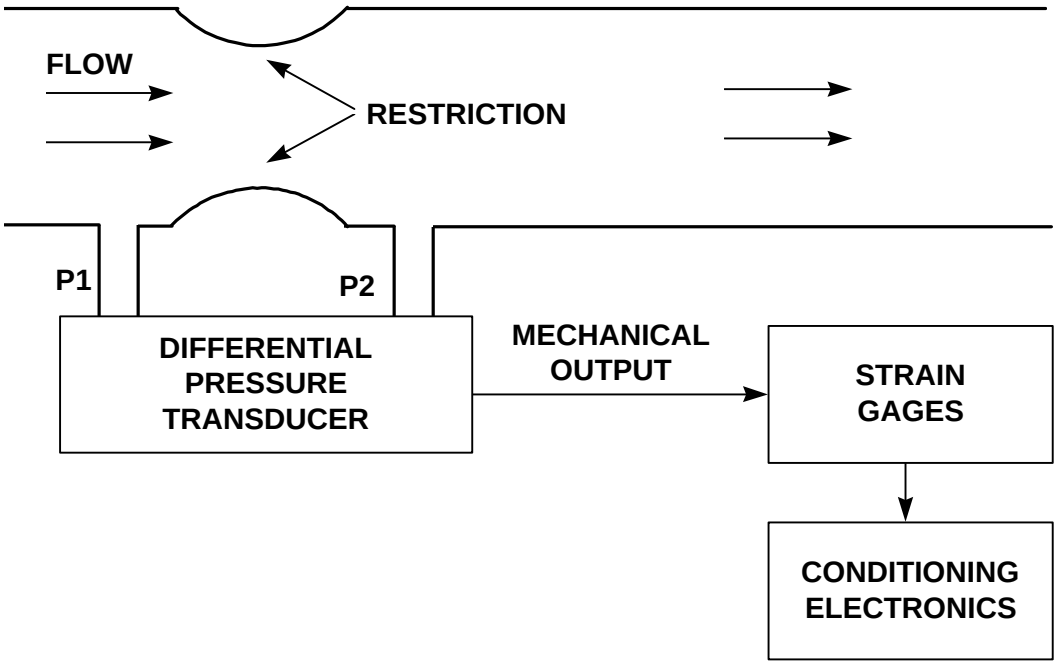


Figure 4.10

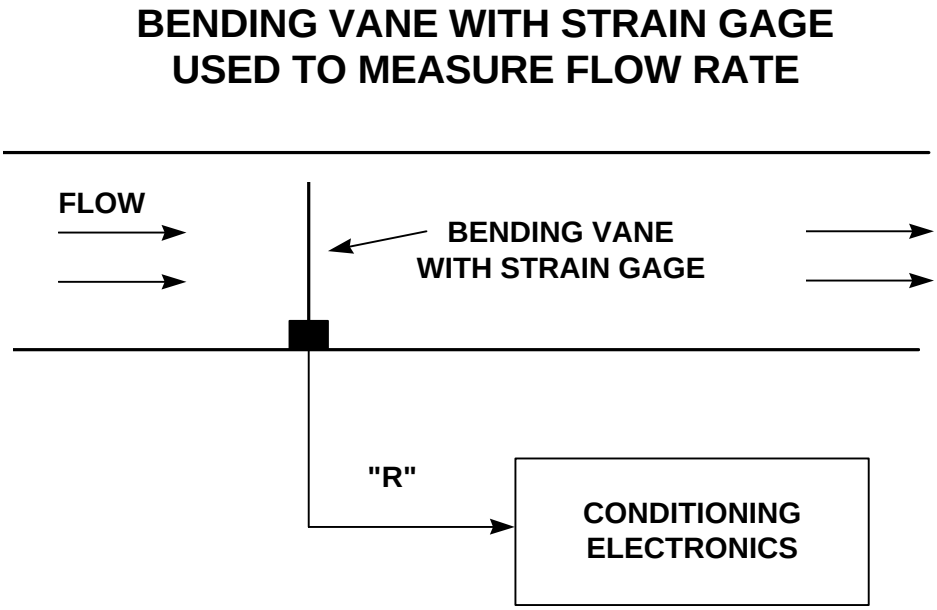


Figure 4.11

BRIDGE SIGNAL CONDITIONING CIRCUITS

An example of an all-element varying bridge circuit is a fatigue monitoring strain sensing circuit as shown in Figure 4.12. The full bridge is an integrated unit that can be attached to the surface on which the strain or flex is to be measured. In order to facilitate remote sensing, current excitation is used. The OP177 servos the bridge current to 10mA around a reference voltage of 1.235V. The strain gauge produces an output of 10.25mV/1000με. The signal is amplified by the AD620 instrumentation amplifier which is configured for a gain of 100. Full-scale strain voltage may be set by adjusting the 100Ω gain potentiometer such that, for a strain of –3500με, the output reads –3.500V; and for a strain of +5000με, the output registers a +5.000V. The measurement may then be digitized with an ADC which has a 10V fullscale input range. The 0.1μF capacitor across the AD620 input pins serves as an EMI/RFI filter in conjunction with the bridge resistance of 1kΩ. The corner frequency of the filter is approximately 1.6kHz.

PRECISION STRAIN GAGE SENSOR AMPLIFIER

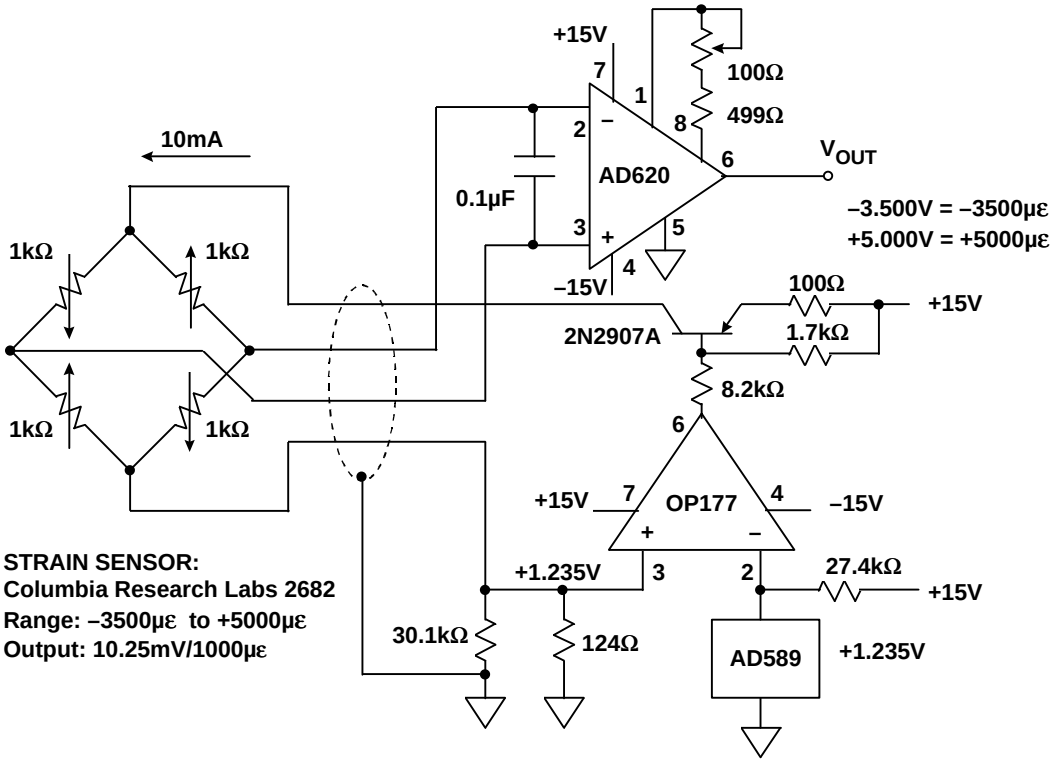


Figure 4.12

Another example is a load cell amplifier circuit shown in Figure 4.13. A typical load cell has a bridge resistance of 350Ω. A 10.000V bridge excitation is derived from an AD588 precision voltage reference with an OP177 and 2N2219A used as a buffer. The 2N2219A is within the OP177 feedback loop and supplies the necessary bridge drive current (28.57mA). To ensure this linearity is preserved, an instrumentation amplifier is used. This design has a minimum number of critical resistors and amplifiers, making the entire implementation accurate, stable, and cost effective. The only requirement is that the 475Ω resistor and the 100Ω potentiometer have low temperature coefficients so that the amplifier gain does not drift over temperature.

PRECISION LOAD CELL AMPLIFIER

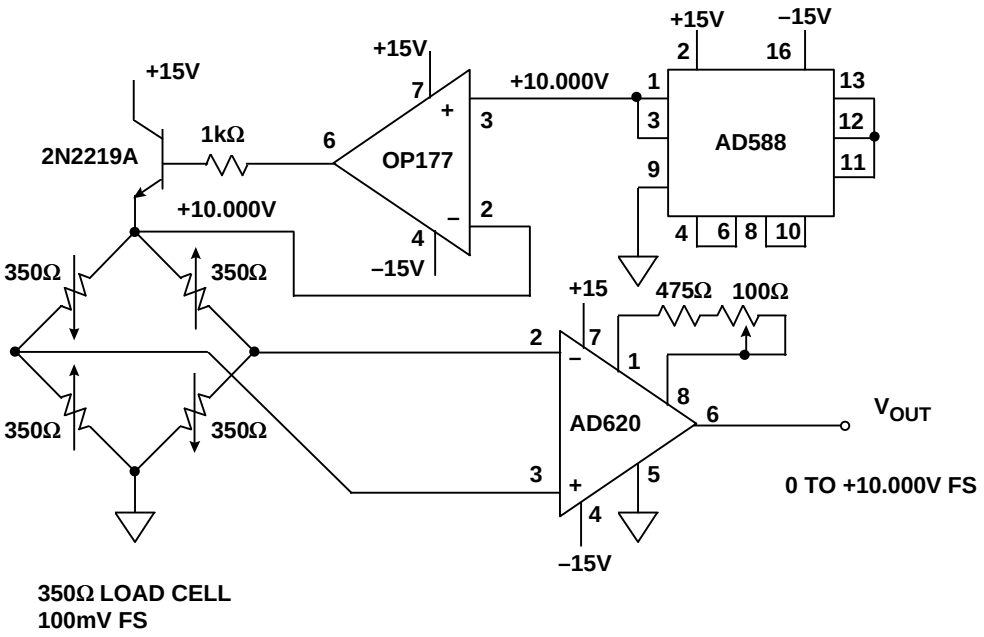


Figure 4.13

As has been previously shown, a precision load cell is usually configured as a 350Ω bridge. Figure 4.14 shows a precision load-cell amplifier that is powered from a single supply. The excitation voltage to the bridge must be precise and stable, otherwise it introduces an error in the measurement. In this circuit, a precision REF195 5V reference is used as the bridge drive. The REF195 reference can supply more than 30mA to a load, so it can drive the 350Ω bridge without the need of a buffer. The dual OP213 is configured as a two op amp in-amp with a gain of 100. The resistor network sets the gain according to the formula:

$$G = 1 + \frac{10\,k\Omega}{1\,k\Omega} + \frac{20\,k\Omega}{196\Omega + 28.7\Omega} = 100\,.$$

For optimum common-mode rejection, the resistor ratios must be precise. High tolerance resistors (±0.5% or better) should be used.

For a zero volt bridge output signal, the amplifier will swing to within 2.5mV of 0V. This is the minimum output limit of the OP213. Therefore, if an offset adjustment is required, the adjustment should start from a positive voltage at V_{REF} and adjust V_{REF} downward until the output (V_{OUT}) stops changing. This is the point where the amplifier limits the swing. Because of the single supply design, the amplifier cannot sense signals which have negative polarity. If linearity at zero volts input is required, or if negative polarity signals must be processed, the V_{REF} connection can be connected to a voltage which is mid-supply (2.5V) rather than ground. Note that when V_{REF} is not at ground, the output must be referenced to V_{REF}.

SINGLE SUPPLY LOAD CELL AMPLIFIER

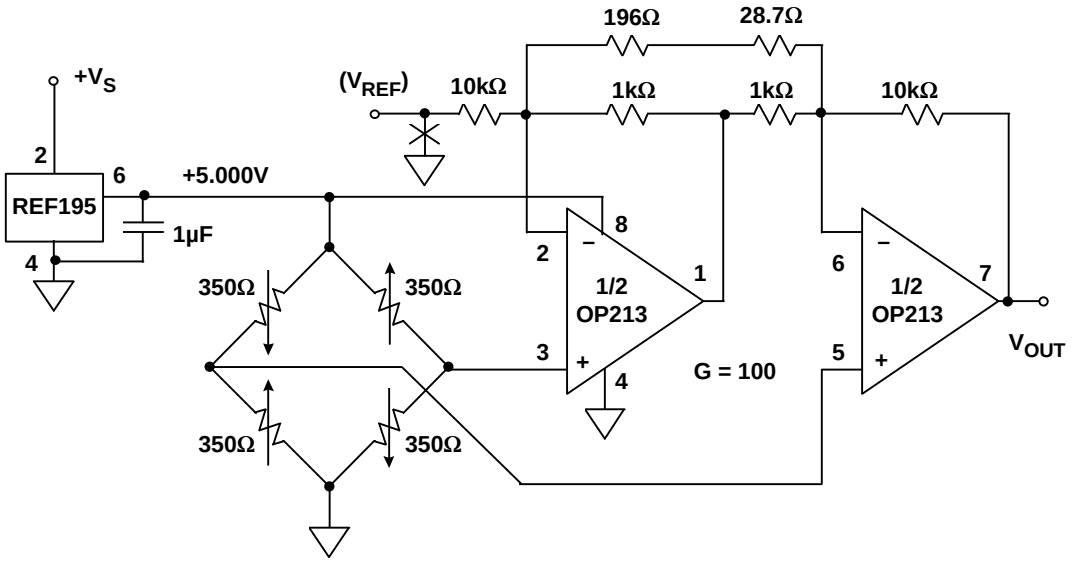


Figure 4.14

The AD7730 24-bit sigma-delta ADC is ideal for direct conditioning of bridge outputs and requires no interface circuitry. The simplified connection diagram is shown in Figure 4.15. The entire circuit operates on a single +5V supply which also serves as the bridge excitation voltage. Note that the measurement is ratiometric because the sensed bridge excitation voltage is also used as the ADC reference. Variations in the +5V supply do not affect the accuracy of the measurement.

The AD7730 has an internal programmable gain amplifier which allows a fullscale bridge output of ±10mV to be digitized to 16-bit accuracy. The AD7730 has self and system calibration features which allow offset and gain errors to be minimized with periodic recalibrations. A "chop" mode option minimizes the offset voltage and drift and operates similarly to a chopper-stabilized amplifier. The effective input voltage noise RTI is approximately 40nV rms, or 264nV peak-to-peak. This corresponds to a resolution of 13 ppm, or approximately 16.5-bits . Gain linearity is also approximately 16-bits. Further discussion of this type of ADC can be found in Section 8.

LOAD CELL APPLICATION USING THE AD7730 ADC

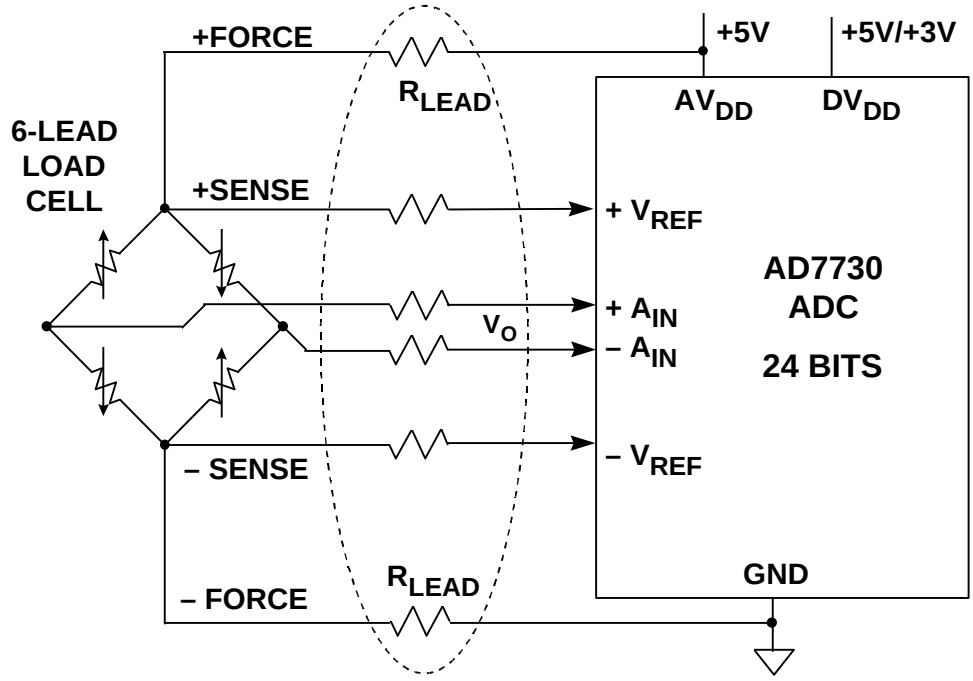


Figure 4.15

PERFORMANCE OF AD7730 LOAD CELL ADC

- **Assume:**
  - **Fullscale Bridge Output of ±10mV, +5V Excitation**
  - **"Chop Mode" Activated**
  - **System Calibration Performed: Zero and Fullscale**

- **Performance:**
  - **Noise RTI: 40nV rms, 264nV p-p**
  - **Noise-Free Resolution: ≈80,000 Counts (16.5 bits)**
  - **Gain Nonlinearity: 18ppm**
  - **Gain Accuracy: < 1µV**
  - **Offset Voltage: <1µV**
  - **Offset Drift: 0.5 µV/°C**
  - **Gain Drift: 2ppm/°C**
  - **Note: Gain and Offset Drift Removable with System Recalibration**

Figure 4.16

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SECTION 5
HIGH IMPEDANCE SENSORS

Walt Kester, Scott Wurcer, Chuck Kitchin

Many popular sensors have output impedances greater than several MΩ, and the associated signal conditioning circuitry must be carefully designed to meet the challenges of low bias current, low noise, and high gain. A large portion of this section is devoted to the analysis of a photodiode preamplifier. This application points out many of the problems associated with high impedance sensor signal conditioning circuits and offers practical solutions which can be applied to practically all such sensors. Other examples of high impedance sensors discussed are piezoelectric sensors, charge output sensors, and charge coupled devices (CCDs).

HIGH IMPEDANCE SENSORS

- **Photodiode Preamplifiers**
- **Piezoelectric Sensors**
  - **Accelerometers**
  - **Hydrophones**
- **Humidity Monitors**
- **pH Monitors**
- **Chemical Sensors**
- **Smoke Detectors**
- **Charge Coupled Devices and Contact Image Sensors for Imaging**

Figure 5.1

PHOTODIODE PREAMPLIFIER DESIGN

Photodiodes generate a small current which is proportional to the level of illumination. They have many applications ranging from precision light meters to high-speed fiber optic receivers.

The equivalent circuit for a photodiode is shown in Figure 5.3. One of the standard methods for specifying the sensitivity of a photodiode is to state its short circuit photocurrent (I_{SC}) at a given light level from a well defined light source. The most commonly used source is an incandescent tungsten lamp running at a color

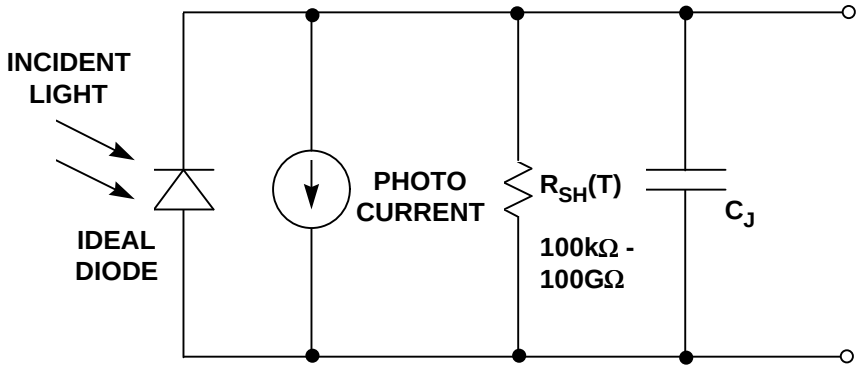
temperature of 2850K. At 100 fc (foot-candles) illumination (approximately the light level on an overcast day), the short circuit current is usually in the picoamps to hundreds of microamps range for small area (less than $1mm^2$) diodes.

PHOTODIODE APPLICATIONS

- **Optical: Light Meters, Auto-Focus, Flash Controls**
- **Medical: CAT Scanners (X-Ray Detection), Blood Particle Analyzers**
- **Automotive: Headlight Dimmers, Twilight Detectors**
- **Communications: Fiber Optic Receivers**
- **Industrial: Bar Code Scanners, Position Sensors, Laser Printers**

Figure 5.2

PHOTODIODE EQUIVALENT CIRCUIT



NOTE: R_{SH} HALVES EVERY 10°C TEMPERATURE RISE

Figure 5.3

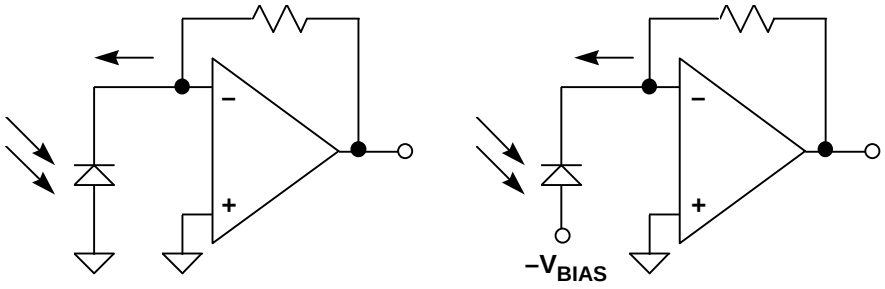
The short circuit current is very linear over 6 to 9 decades of light intensity, and is therefore often used as a measure of absolute light levels. The open circuit forward voltage drop across the photodiode varies logarithmically with light level, but,

because of its large temperature coefficient, the diode voltage is seldom used as an accurate measure of light intensity.

The shunt resistance R_{SH} is usually in the order of 1000MΩ at room temperature, and decreases by a factor of 2 for every 10ºC rise in temperature. Diode capacitance C_J is a function of junction area and the diode bias voltage. A value of 50pF at zero bias is typical for small area diodes.

Photodiodes may either be operated with zero bias (*photovoltaic* mode, left) or reverse bias (*photoconductive* mode, right) as shown in Figure 5.4. The most precise linear operation is obtained in the photovoltaic mode, while higher switching speeds are realizable when the diode is operated in the photoconductive mode at the expense of linearity. Under these reverse bias conditions, a small amount of current called *dark current* will flow even when there is no illumination. There is no dark current in the photovoltaic mode. In the photovoltaic mode, the diode noise is basically the thermal noise generated by the shunt resistance. In the photoconductive mode, shot noise due to conduction is an additional source of noise. Photodiodes are usually optimized during the design process for use in either the photovoltaic mode or the photoconductive mode, but not both. Figure 5.5 shows the photosensitivity for a small photodiode (Silicon Detector Part Number SD-020-12-001), and specifications for the diode are summarized in Figure 5.6. This diode was chosen for the design example to follow.

PHOTODIODE MODES OF OPERATION



PHOTOVOLTAIC	PHOTOCONDUCTIVE
■ Zero Bias	■ Reverse Bias
■ No "Dark" Current	■ Has "Dark" Current
■ Linear	■ Nonlinear
■ Low Noise (Johnson)	■ Higher Noise (Johnson + Shot)
■ Precision Applications	■ High Speed Applications

Figure 5.4

PHOTODIODE SPECIFICATIONS
Silicon Detector Part Number SD-020-12-001

- **Area: 0.2mm^2**
- **Capacitance: 50pF**
- **Shunt Resistance @ 25°C: 1000MΩ**
- **Maximum Linear Output Current: 40µA**
- **Response Time: 12ns**
- **Photosensitivity: 0.03µA / foot candle (fc)**

Figure 5.5

SHORT CIRCUIT CURRENT VERSUS LIGHT INTENSITY FOR PHOTODIODE (PHOTOVOLTAIC MODE)

ENVIRONMENT	ILLUMINATION (fc)	SHORT CIRCUIT CURRENT
Direct Sunlight	1000	30µA
Overcast Day	100	3µA
Twilight	1	0.03µA
Full Moonlit Night	0.1	3000pA
Clear Night / No Moon	0.001	30pA

Figure 5.6

A convenient way to convert the photodiode current into a usable voltage is to use an op amp as a current-to-voltage converter as shown in Figure 5.7. The diode bias is maintained at zero volts by the virtual ground of the op amp, and the short circuit current is converted into a voltage. At maximum sensitivity, the amplifier must be able to detect a diode current of 30pA. This implies that the feedback resistor must be very large, and the amplifier bias current very small. For example, 1000MΩ will

yield a corresponding voltage of 30mV for this amount of current. Larger resistor values are impractical, so we will use 1000MΩ for the most sensitive range. This will give an output voltage range of 10mV for 10pA of diode current and 10V for 10nA of diode current. This yields a range of 60dB. For higher values of light intensity, the gain of the circuit must be reduced by using a smaller feedback resistor. For this range of maximum sensitivity, we should be able to easily distinguish between the light intensity on a clear moonless night (0.001fc) and that of a full moon (0.1fc)!

CURRENT-TO-VOLTAGE CONVERTER (SIMPLIFIED)

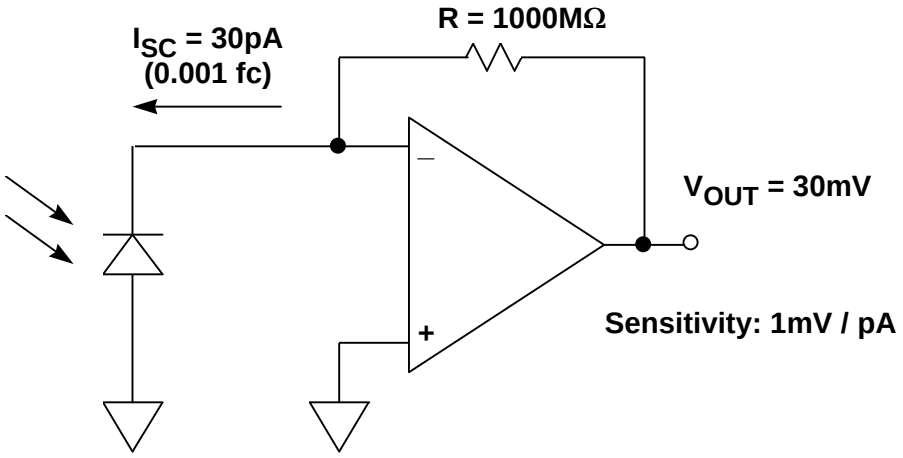


Figure 5.7

Notice that we have chosen to get as much gain as possible from one stage, rather than cascading two stages. This is in order to maximize the signal-to-noise ratio (SNR). If we halve the feedback resistor value, the signal level decreases by a factor of 2, while the noise due to the feedback resistor ($\sqrt{4kTR \cdot Bandwidth}$) decreases by only $\sqrt{2}$. This reduces the SNR by 3dB, assuming the closed loop bandwidth remains constant. Later in the analysis, we will see that the resistors are one of the largest contributors to the overall output noise.

To accurately measure photodiode currents in the tens of picoamps range, the bias current of the op amp should be no more than a few picoamps. This narrows the choice considerably. The industry-standard OP07 is an ultra-low offset voltage (10μV) bipolar op amp , but its bias current is 4nA (4000pA!). Even super-beta bipolar op amps with bias current compensation (such as the OP97) have bias currents on the order of 100pA at room temperature, but may be suitable for very high temperature applications, as these currents do not double every 10ºC rise like FETs. A FET-input electrometer-grade op amp is chosen for our photodiode preamp, since it must operate only over a limited temperature range. Figure 5.8 summarizes the performance of several popular "electrometer grade" FET input op amps. These devices are fabricated on a BiFET process and use P-Channel JFETs as the input stage (see Figure 5.9). The rest of the op amp circuit is designed using bipolar devices. The BiFET op amps are laser trimmed at the wafer level to minimize offset voltage and offset voltage drift. The offset voltage drift is minimized by first trimming the input stage for equal currents in the two JFETs which comprise the

differential pair. A second trim of the JFET source resistors minimizes the input offset voltage. The AD795 was selected for the photodiode preamplifier, and its key specifications are summarized in Figure 5.10.

LOW BIAS CURRENT PRECISION BiFET OP AMPS (ELECTROMETER GRADE)

PART #	V_{OS}, MAX*	TC V_{OS}, MAX	I_B, MAX*	0.1Hz TO 10Hz NOISE	PACKAGE
AD549	250µV	5µV/°C	100fA	4µV p-p	TO-99
AD645	250µV	1µV/°C	1.5pA	2µV p-p	TO-99, DIP
AD795	250µV	3µV/°C	1pA	2.5µV p-p	SOIC, DIP

*** 25°C SPECIFICATION**

Figure 5.8

BiFET OP AMP INPUT STAGE

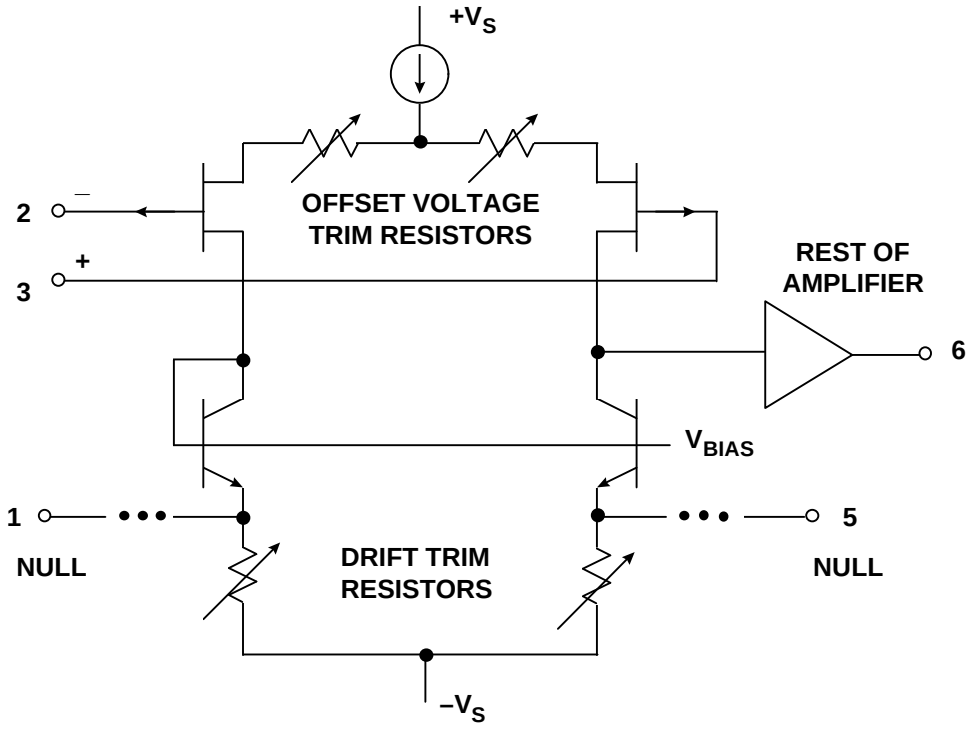


Figure 5.9

AD795 BiFET OP AMP KEY SPECIFICATIONS

- **Offset Voltage: 250µV Max. @ 25°C (K Grade)**
- **Offset Voltage Drift: 3µV / °C Max (K Grade)**
- **Input Bias Current: 1pA Max @ 25°C (K Grade)**
- **0.1Hz to 10Hz Voltage Noise: 2.5µV p-p**
- **1/f Corner Frequency: 12Hz**
- **Voltage Noise: 10nV / √Hz @ 100Hz**
- **Current Noise: 0.6fA / √Hz @ 100Hz**
- **40mW Power Dissipation @ ±15V**
- **1MHz Gain Bandwidth Product**

Figure 5.10

Since the diode current is measured in terms of picoamperes, extreme attention must be given to potential leakage paths in the actual circuit. Two parallel conductor stripes on a high-quality well-cleaned epoxy-glass PC board 0.05 inches apart running parallel for 1 inch have a leakage resistance of approximately 10^{11} ohms at $+125^{o}$C. If there is 15 volts between these runs, there will be a current flow of 150pA.

The critical leakage paths for the photodiode circuit are enclosed by the dotted lines in Figure 5.11. The feedback resistor should be thin film on ceramic or glass with glass insulation. The compensation capacitor across the feedback resistor should have a polypropylene or polystyrene dielectric. All connections to the summing junction should be kept short. If a cable is used to connect the photodiode to the preamp, it should be kept as short as possible and have Teflon insulation.

Guarding techniques can be used to reduce parasitic leakage currents by isolating the amplifier's input from large voltage gradients across the PC board. Physically, a guard is a low impedance conductor that surrounds an input line and is raised to the line's voltage. It serves to buffer leakage by diverting it away from the sensitive nodes.

LEAKAGE CURRENT PATHS

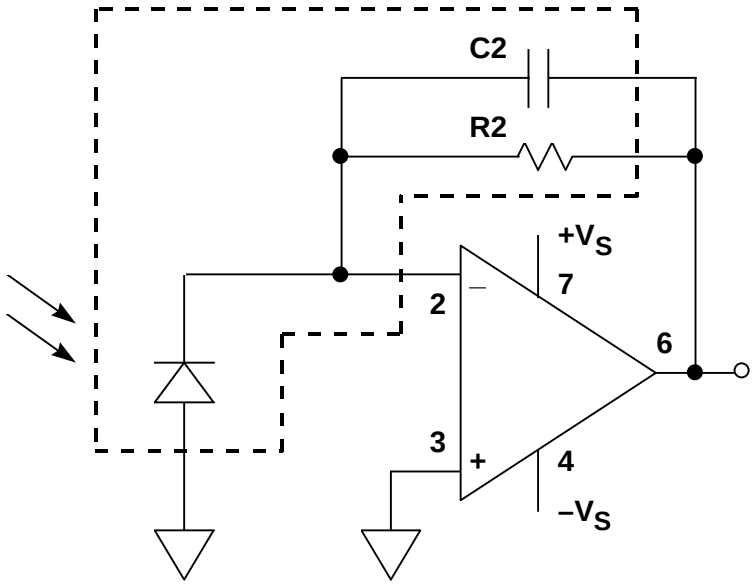


Figure 5.11

The technique for guarding depends on the mode of operation, i.e., inverting or non-inverting. Figure 5.12 shows a PC board layout for guarding the inputs of the AD795 op amp in the DIP ("N") package. Note that the pin spacing allows a trace to pass between the pins of this package. In the inverting mode, the guard traces surround the inverting input (pin 2) and run parallel to the input trace. In the follower mode, the guard voltage is the feedback voltage to pin 2, the inverting input. In both modes, the guard traces should be located on both sides of the PC board if at all possible and connected together.

Things are slightly more complicated when using guarding techniques with the SOIC surface mount ("R") package because the pin spacing does not allow for PC board traces between the pins. Figure 5.13 shows the preferred method. In the SOIC "R" package, pins 1, 5, and 8 are "no connect" pins and can be used to route signal traces as shown. In the case of the follower, the guard trace must be routed around the $-V_S$ pin.

For extremely low bias current applications (such as using the AD549 with an input bias current of 100fA), all connections to the input of the op amp should be made to a virgin Teflon standoff insulator ("Virgin" Teflon is a solid piece of new Teflon material which has been machined to shape and has not been welded together from powder or grains). If mechanical and manufacturing considerations allow, the inverting input pin of the op amp should be soldered directly to the Teflon standoff (see Figure 5.14) rather than going through a hole in the PC board. The PC board itself must be cleaned carefully and then sealed against humidity and dirt using a high quality conformal coating material.

PCB LAYOUT FOR GUARDING DIP PACKAGE

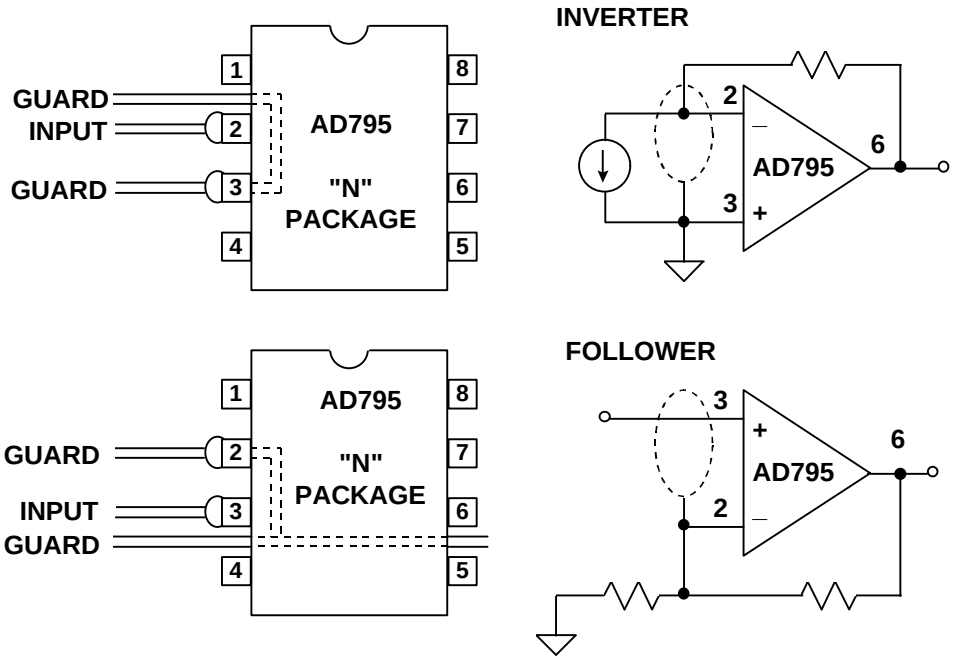


Figure 5.12

PCB LAYOUT FOR GUARDING SOIC PACKAGE

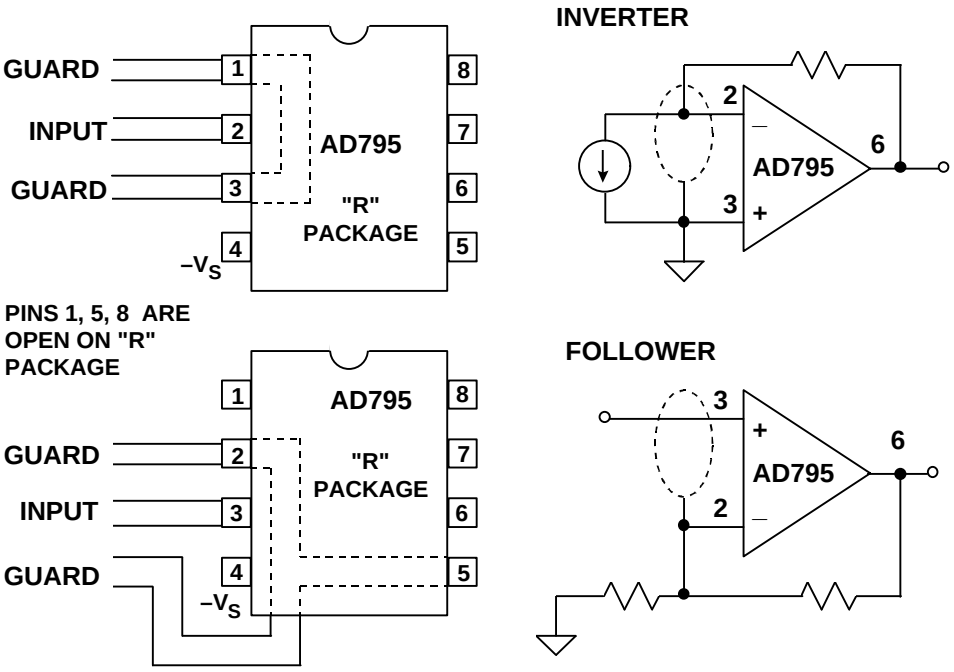


Figure 5.13

INPUT PIN CONNECTED TO "VIRGIN" TEFLON INSULATED STANDOFF

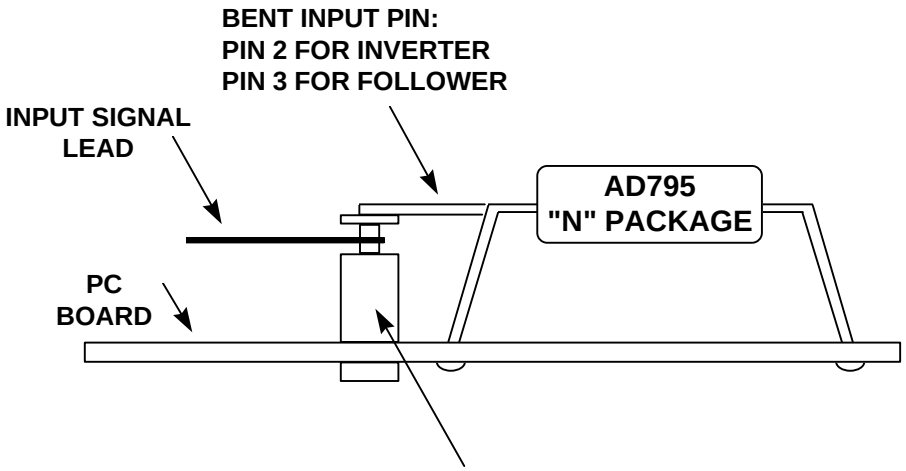


Figure 5.14

In addition to minimizing leakage currents, the entire circuit should be well shielded with a grounded metal shield to prevent stray signal pickup.

PREAMPLIFIER OFFSET VOLTAGE AND DRIFT ANALYSIS

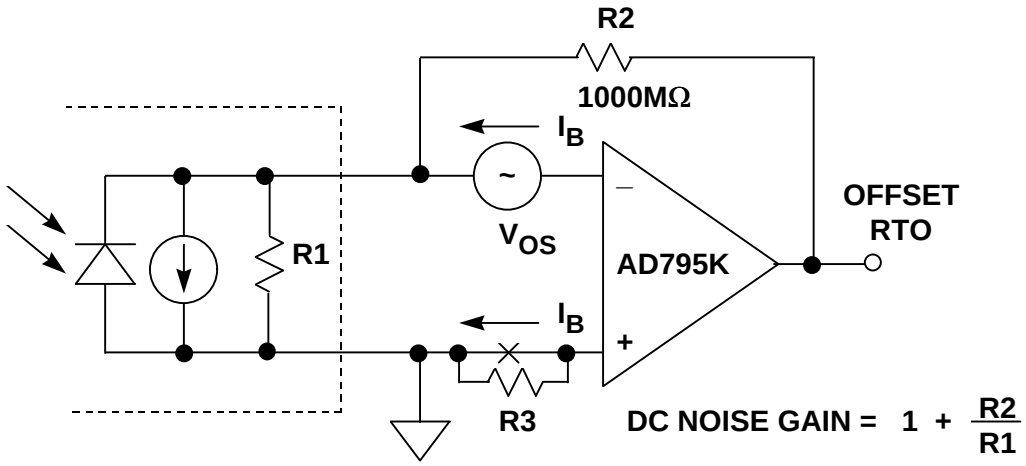
An offset voltage and bias current model for the photodiode preamp is shown in Figure 5.15. There are two important considerations in this circuit. First, the diode shunt resistance (R1) is a function of temperature - it halves every time the temperature increases by 10ºC. At room temperature (+25ºC) , R1 = 1000MΩ, but at +70ºC it decreases to 43MΩ. This has a drastic impact on the circuit DC noise gain and hence the output offset voltage. In the example, at +25ºC the DC noise gain is 2, but at +70ºC it increases to 24.

The second difficulty with the circuit is that the input bias current doubles every 10ºC rise in temperature. The bias current produces an output offset error equal to $I_B R2$. At +70ºC the bias current increases to 24pA compared to its room temperature value of 1pA. Normally, the addition of a resistor (R3) between the non-inverting input of the op amp and ground having a value of R1||R2 would yield a first-order cancellation of this effect. However, because R1 changes with temperature, this method is not effective. In addition, the bias current develops a voltage across the R3 cancellation resistor, which in turn is applied to the photodiode, thereby causing the diode response to become nonlinear.

The total referred to output (RTO) offset voltage errors are summarized in Figure 5.16. Notice that at +70ºC the total error is 33.24mV. This error is acceptable for the design under consideration. The primary contributor to the error at high temperature is of course the bias current. Operating the amplifier at reduced supply voltages, minimizing output drive requirements, and heat sinking are some ways to

reduce this error source. The addition of an external offset nulling circuit would minimize the error due to the initial input offset voltage.

AD795 PREAMPLIFIER DC OFFSET ERRORS



- I_B DOUBLES EVERY 10°C TEMPERATURE RISE
- R1 = 1000MΩ @ 25°C (DIODE SHUNT RESISTANCE)
- R1 HALVES EVERY 10°C TEMPERATURE RISE
- R3 CANCELLATION RESISTOR NOT EFFECTIVE

Figure 5.15

AD795K PREAMPLIFIER TOTAL OUTPUT OFFSET ERROR

	0°C	25°C	50°C	70°C
V_{OS}	0.325mV	0.250mV	0.325mV	0.385mV
Noise Gain	1.1	2	7	24
V_{OS} Error RTO	0.358mV	0.500mV	2.28mV	9.24mV
I_B	0.2pA	1.0pA	6.0pA	24pA
I_B Error RTO	0.2mV	1mV	6.0mV	24mV
Total Error RTO	0.558mV	1.50mV	8.28mV	33.24mV

Figure 5.16

THERMOELECTRIC VOLTAGES AS SOURCES OF INPUT OFFSET VOLTAGE

Thermoelectric potentials are generated by electrical connections which are made between different metals at different temperatures. For example, the copper PC board electrical contacts to the kovar input pins of a TO-99 IC package can create an offset voltage of 40μV/^{o}C when the two metals are at different temperatures. Common lead-tin solder, when used with copper, creates a thermoelectric voltage of 1 to 3μV/^{o}C. Special cadmium-tin solders are available that reduce this to 0.3μV/^{o}C. (Reference 8, p. 127). The solution to this problem is to ensure that the connections to the inverting and non-inverting input pins of the IC are made with the same material and that the PC board thermal layout is such that these two pins remain at the same temperature. In the case where a Teflon standoff is used as an insulated connection point for the inverting input (as in the case of the photodiode preamp), prudence dictates that connections to the non-inverting inputs be made in a similar manner to minimize possible thermoelectric effects.

PREAMPLIFIER AC DESIGN, BANDWIDTH, AND STABILITY

The key to the preamplifier AC design is an understanding of the circuit noise gain as a function of frequency. Plotting gain versus frequency on a log-log scale makes the analysis relatively simple (see Figure 5.17). This type of plot is also referred to as a Bode plot. The noise gain is the gain seen by a small voltage source in series with the op amp input terminals. It is also the same as the non-inverting signal gain (the gain from "A" to the output). In the photodiode preamplifier, the signal current from the photodiode passes through the C2/R2 network. It is important to distinguish between the signal gain and the noise gain, because it is the noise gain characteristic which determines stability regardless of where the actual signal is applied.

Stability of the system is determined by the net slope of the noise gain and the open loop gain where they intersect. For unconditional stability, the noise gain curve must intersect the open loop response with a net slope of less than 12dB/octave (20dB per decade). The dotted line shows a noise gain which intersects the open loop gain at a net slope of 12dB/octave, indicating an unstable condition. This is what would occur in our photodiode circuit if there were no feedback capacitor (i.e. C2 = 0).

GENERALIZED NOISE GAIN (NG) BODE PLOT

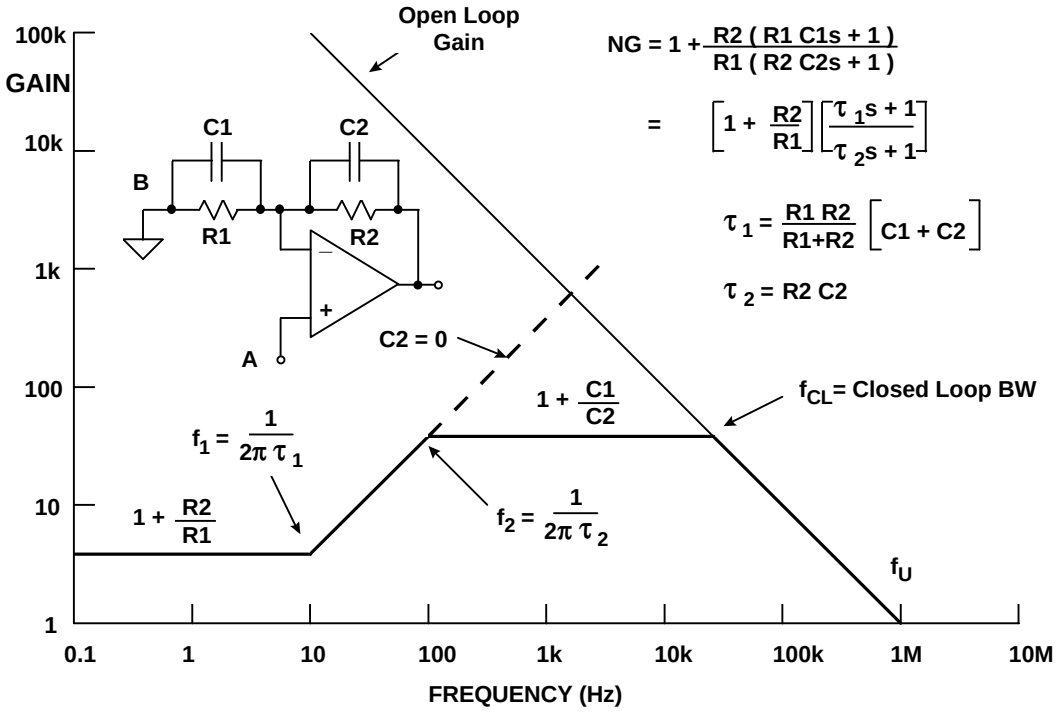


Figure 5.17

The general equations for determining the break points and gain values in the Bode plot are also given in Figure 5.17. A zero in the noise gain transfer function occurs at a frequency of $1/2\pi\tau_1$, where $\tau_1 = R1||R2(C1 + C2)$. The pole of the transfer function occurs at a corner frequency of $1/2\pi\tau_2$, where $\tau_2 = R2C2$ which is also equal to the signal bandwidth if the signal is applied at point "B". At low frequencies, the noise gain is 1 + R2/R1. At high frequencies, it is 1 + C1/C2. Plotting the curve on the log-log graph is a simple matter of connecting the breakpoints with a line having a slope of 45º. The point at which the noise gain intersects the op amp open loop gain is called the *closed loop bandwidth*. Notice that the *signal bandwidth* for a signal applied at point "B" is much less, and is $1/2\pi R2C2$.

Figure 5.18 shows the noise gain plot for the photodiode preamplifier using the actual circuit values. The choice of C2 determines the actual signal bandwidth and also the phase margin. In the example, a signal bandwidth of 16Hz was chosen. Notice that a smaller value of C2 would result in a higher signal bandwidth and a corresponding reduction in phase margin. It is also interesting to note that although the signal bandwidth is only 16Hz, the closed loop bandwidth is 167kHz. This will have important implications with respect to the output noise voltage analysis to follow.

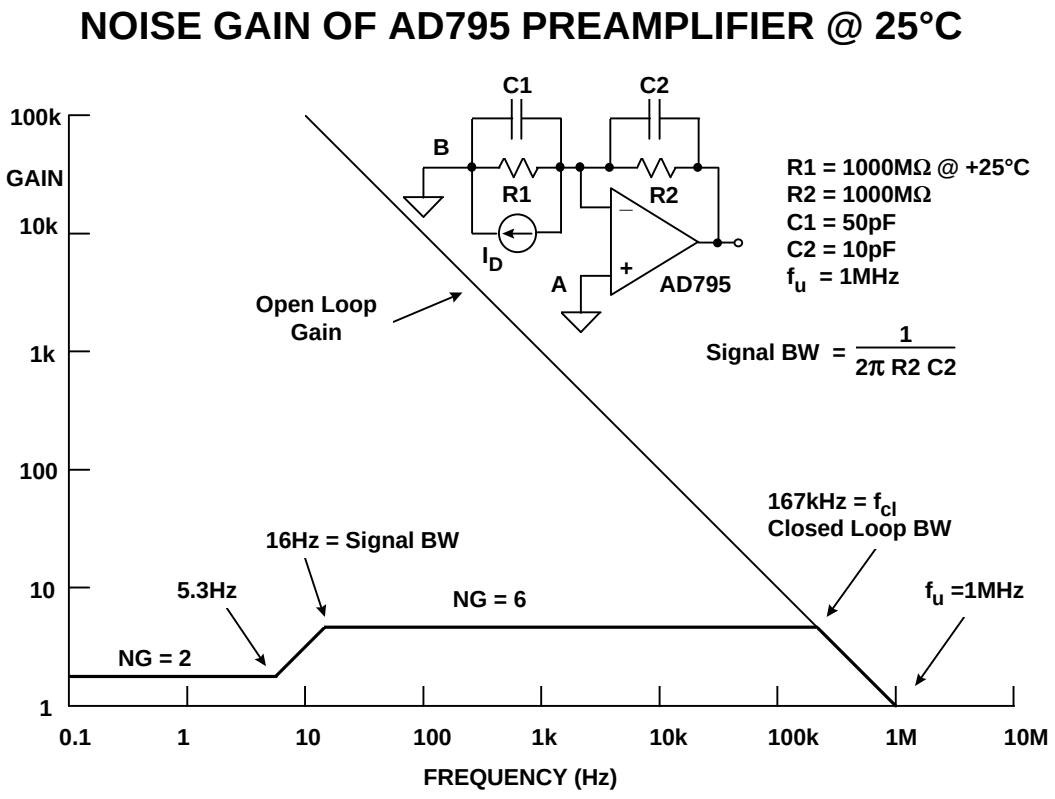


Figure 5.18

It is important to note that temperature changes do not significantly affect the stability of the circuit. Changes in R1 (the photodiode shunt resistance) only affect the low frequency noise gain and the frequency at which the zero in the noise gain response occurs. The high frequency noise gain is determined by the C1/C2 ratio.

PHOTODIODE PREAMPLIFIER NOISE ANALYSIS

To begin the analysis, we consider the AD795 input voltage and current noise spectral densities shown in Figure 5.19. The AD795 performance is truly impressive for a JFET input op amp: 2.5μV p-p 0.1Hz to 10Hz noise, and a 1/f corner frequency of 12Hz, comparing favorably with all but the best bipolar op amps. As shown in the figure, the current noise is much lower than bipolar op amps, making it an ideal choice for high impedance applications.

The complete noise model for an op amp is shown in Figure 5.20. This model includes the reactive elements C1 and C2. Each individual output noise contributor is calculated by integrating the square of its spectral density over the appropriate frequency bandwidth and then taking the square root:

$$\text{RMS OUTPUT NOISE DUE TO } V_1 = \sqrt{\int V_1(f)^2 df}\ .$$

In most cases, this integration can be done by inspection of the graph of the individual spectral densities superimposed on a graph of the noise gain. The total output noise is then obtained by combining the individual components in a root-sum-squares manner. The table below the diagram in Figure 5.20 shows how each individual source is reflected to the output and the corresponding bandwidth for integration. The factor of 1.57 ($\pi/2$) is required to convert the single pole bandwidth into its equivalent noise bandwidth. The resistor Johnson noise spectral density is given by:

$$V_R = \sqrt{4kTR}\ ,$$

where k is Boltzmann's constant (1.38×10^{-23} J/K) and T is the absolute temperature in K. A simple way to compute this is to remember that the noise spectral density of a 1kΩ resistor is 4nV/√Hz at +25ºC. The Johnson noise of another resistor value can be found by multiplying by the square root of the ratio of the resistor value to 1000Ω. Johnson noise is broadband, and its spectral density is constant with frequency.

VOLTAGE AND CURRENT NOISE OF AD795

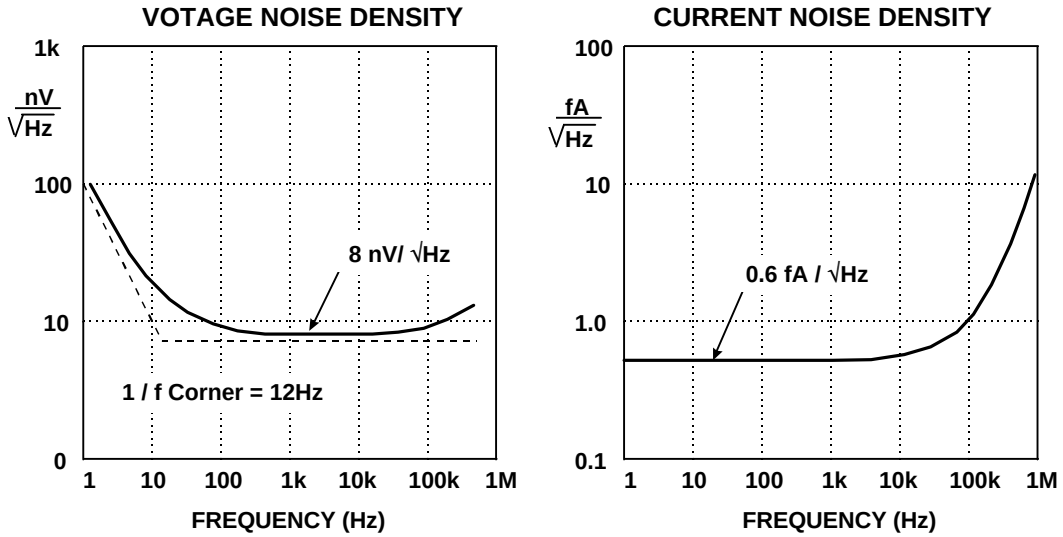
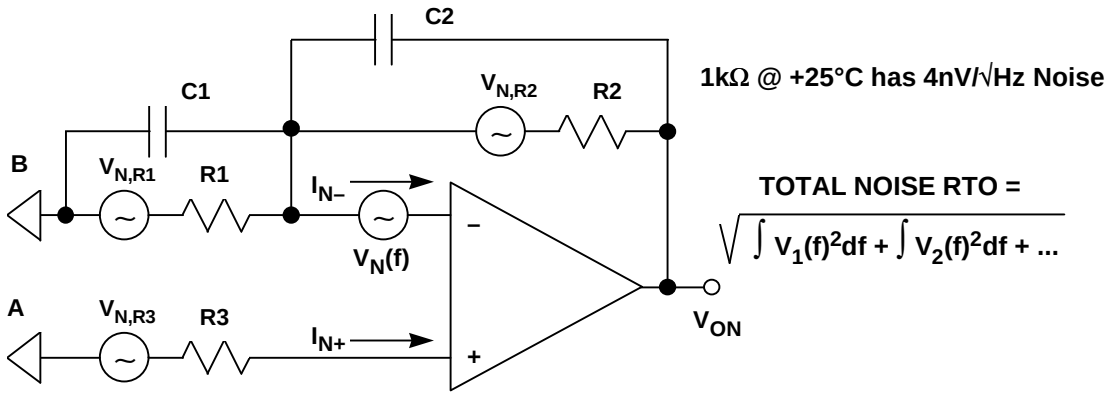


Figure 5.19

AMPLIFIER NOISE MODEL



NOISE SOURCE	RTO	INTEGRATION BW
$V_N(f)$	$V_N(f)$•Noise Gain	1.57•Closed Loop BW
I_{N+}	I_{N+}•R3• Noise Gain	1.57•Closed Loop BW
I_{N-}	I_{N-}•R2	1.57 •Signal BW
R1	$V_{N,R1}$•(R2/R1)	1.57 •Signal BW
R2	$V_{N,R2}$	1.57 •Signal BW
R3	$V_{N,R3}$ •Noise Gain	1.57•Closed Loop BW

Figure 5.20

Input Voltage Noise

In order to obtain the output voltage noise spectral density plot due to the input voltage noise, the input voltage noise spectral density plot is multiplied by the noise gain plot. This is easily accomplished using the Bode plot on a log-log scale. The total RMS output voltage noise due to the input voltage noise is then obtained by integrating the square of the output voltage noise spectral density plot and then taking the square root. In most cases, this integration may be approximated. A lower frequency limit of 0.01Hz in the 1/f region is normally used. If the bandwidth of integration for the input voltage noise is greater than a few hundred Hz, the input voltage noise spectral density may be assumed to be constant. Usually, the value of the input voltage noise spectral density at 1kHz will provide sufficient accuracy.

It is important to note that the input voltage noise contribution must be integrated over the entire closed loop bandwidth of the circuit (the closed loop bandwidth, f_{Cl}, is the frequency at which the noise gain intersects the op amp open loop response). This is also true of the other noise contributors which are reflected to the output by the noise gain (namely, the non-inverting input current noise and the non-inverting input resistor noise).

The inverting input noise current flows through the feedback network to produce a noise voltage contribution at the output The input noise current is approximately constant with frequency, therefore, the integration is accomplished by multiplying the noise current spectral density (measured at 1kHz) by the noise bandwidth which is 1.57 times the signal bandwidth ($1/2\pi R2C2$). The factor of 1.57 ($\pi/2$) arises when single-pole 3dB bandwidth is converted to equivalent noise bandwidth.

Johnson Noise Due to Feedforward Resistor R1

The noise current produced by the feedforward resistor R1 also flows through the feedback network to produce a contribution at the output. The noise bandwidth for integration is also 1.57 times the signal bandwidth.

Non-Inverting Input Current Noise

The non-inverting input current noise, I_{N+}, develops a voltage noise across R3 which is reflected to the output by the noise gain of the circuit. The bandwidth for integration is therefore the closed loop bandwidth of the circuit. However, there is no contribution at the output if R3 = 0 or if R3 is bypassed with a large capacitor which is usually desirable when operating the op amp in the inverting mode.

Johnson Noise Due to Resistor in Non-Inverting Input

The Johnson voltage noise due to R3 is also reflected to the output by the noise gain of the circuit. If R3 is bypassed sufficiently, it makes no significant contribution to the output noise.

Summary of Photodiode Circuit Noise Performance

Figure 5.21 shows the output noise spectral densities for each of the contributors at +25ºC. Note that there is no contribution due to I_{N+} or R3 since the non-inverting input of the op amp is grounded.

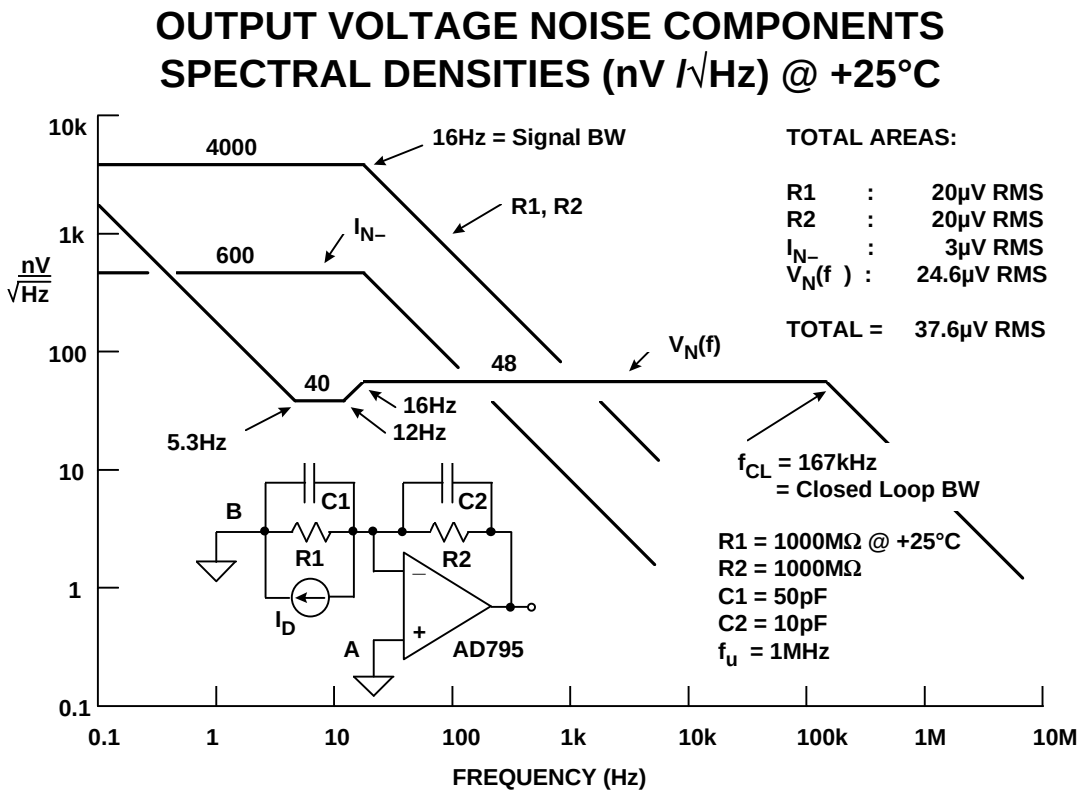


Figure 5.21

Noise Reduction Using Output Filtering

From the above analysis, the largest contributor to the output noise voltage at +25°C is the input voltage noise of the op amp reflected to the output by the noise gain. This contributor is large primarily because the noise gain over which the integration is performed extends to a bandwidth of 167kHz (the intersection of the noise gain curve with the open-loop response of the op amp). If the op amp output is filtered by a single pole filter (as shown in Figure 5.22) with a 20Hz cutoff frequency (R = 80MΩ, C = 0.1µF), this contribution is reduced to less than 1µV rms. Notice that the same results would not be achieved simply by increasing the feedback capacitor, C2. Increasing C2 lowers the high frequency noise gain, but the integration bandwidth becomes proportionally higher. Larger values of C2 may also decrease the signal bandwidth to unacceptable levels. The addition of the simple filter reduces the output noise to 28.5µV rms; approximately 75% of its former value. After inserting the filter, the resistor noise and current noise are now the largest contributors to the output noise.

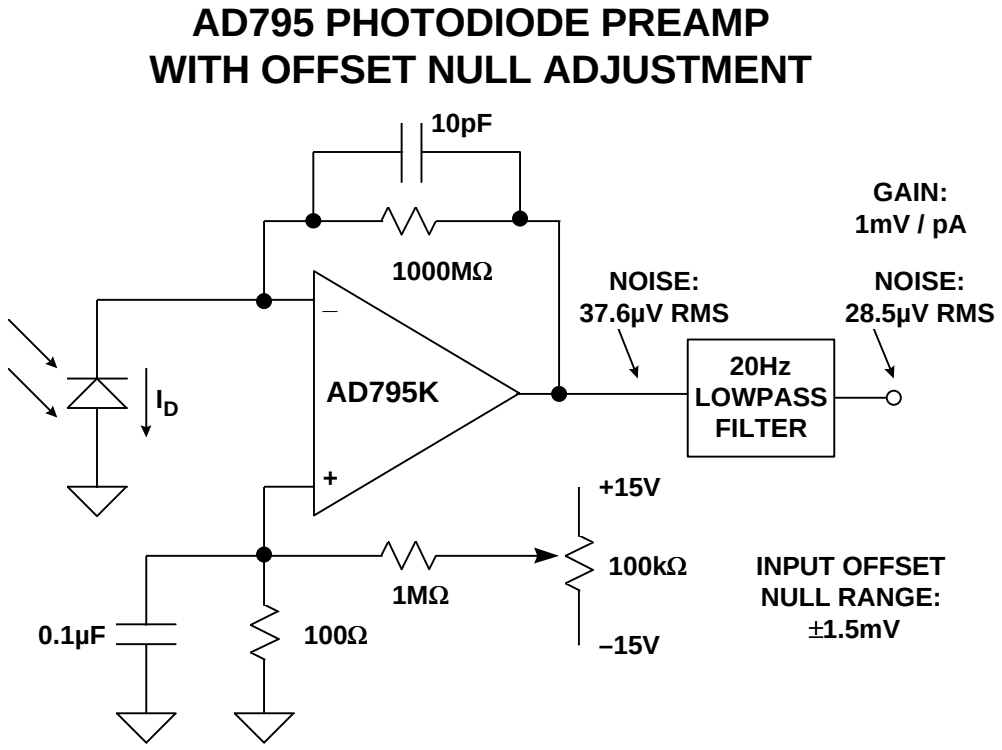


Figure 5.22

SUMMARY OF CIRCUIT PERFORMANCE

The diagram for the final optimized design of the photodiode circuit is shown in Figure 5.22. Performance characteristics are summarized in Figure 5.23. The total output voltage drift over 0 to +70ºC is 33mV. This corresponds to 33pA of diode current, or approximately 0.001 foot-candles. (The level of illumination on a clear moonless night). The offset nulling circuit shown on the non-inverting input can be used to null out the room temperature offset. Note that this method is better than

using the offset null pins because using the offset null pins will increase the offset voltage TC by about 3µV/ºC for each millivolt nulled. In addition, the AD795 SOIC package does not have offset nulling pins.

The input sensitivity based on a total output voltage noise of 44µV is obtained by dividing the output voltage noise by the value of the feedback resistor R2. This yields a minimum detectable diode current of 44fA. If a 12 bit ADC is used to digitize the 10V fullscale output, the weight of the least significant bit (LSB) is 2.5mV. The output noise level is much less than this.

AD795 PHOTODIODE CIRCUIT PERFORMANCE SUMMARY

- **Output Offset Error (0°C to +70°C) : 33mV**
- **Output Sensitivity: 1mV / pA**
- **Output Photosensitivity: 30V / foot-candle**
- **Total Output Noise @ +25°C : 28.5µV RMS**
- **Total Noise RTI @ +25°C : 44fA RMS, or 26.4pA p-p**
- **Range with R2 = 1000MΩ : 0.001 to 0.33 foot-candles**
- **Bandwidth: 16Hz**

Figure 5.23

PHOTODIODE CIRCUIT TRADEOFFS

There are many tradeoffs which could be made in the basic photodiode circuit design we have described. More signal bandwidth can be achieved in exchange for a larger output noise level. Reducing the feedback capacitor C2 to 1pF increases the signal bandwidth to approximately 160Hz. Further reductions in C2 are not practical because the parasitic capacitance is probably in the order of 1 to 2pF. A small amount of feedback capacitance is also required to maintain stability.

If the circuit is to be operated at higher levels of illumination (greater than approximately 0.3 fc), the value of the feedback resistor can be reduced thereby resulting in further increases in circuit bandwidth and less resistor noise. If gain-ranging is to be used to measure the higher light levels, extreme care must be taken in the design and layout of the additional switching networks to minimize leakage paths.

COMPENSATION OF A HIGH SPEED PHOTODIODE I/V CONVERTER

A classical I/V converter is shown in Figure 5.24. Note that it is the same as the photodiode preamplifier if we assume that R1 >> R2. The total input capacitance, C1, is the sum of the diode capacitance and the op amp input capacitance. This is a classical second-order system, and the following guidelines can be applied in order to determine the proper compensation.

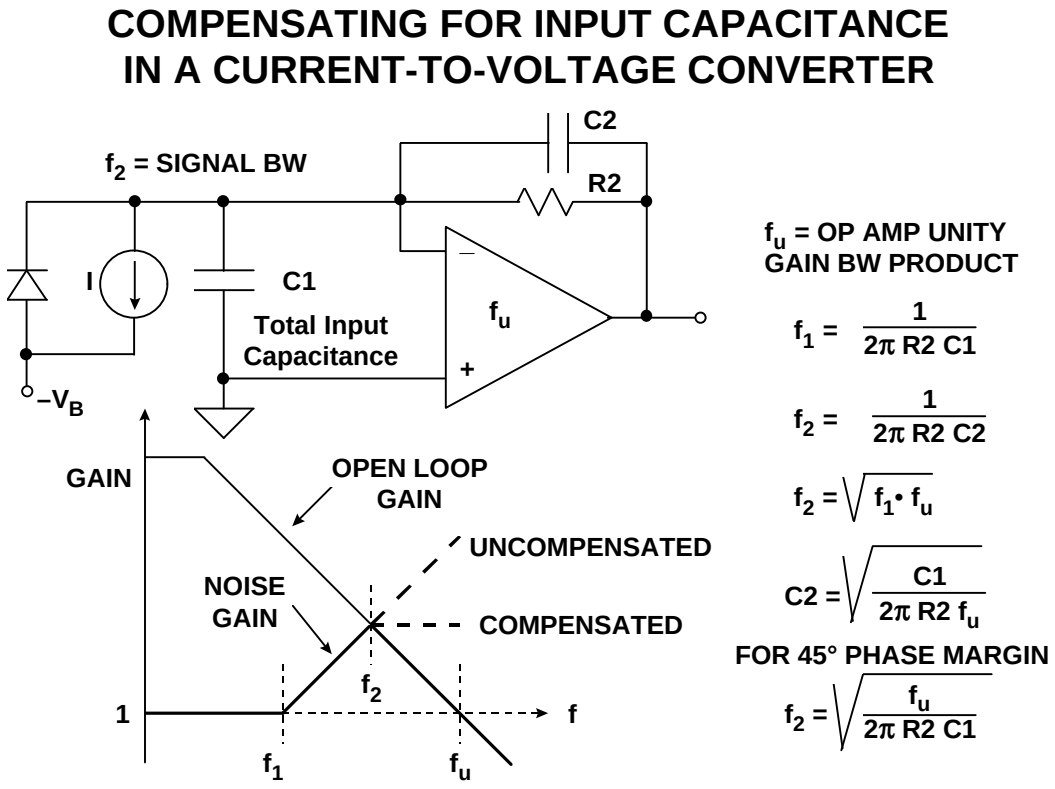


Figure 5.24

The net input capacitance, C1, forms a zero at a frequency f_1 in the noise gain transfer function as shown in the Bode plot.

$$f_1 = \frac{1}{2\pi R2C1}.$$

Note that we are neglecting the effects of the compensation capacitor C2 and are assuming that it is small relative to C1 and will not significantly affect the zero frequency f_1 when it is added to the circuit. In most cases, this approximation yields results which are close enough, considering the other variables in the circuit.

If left uncompensated, the phase shift at the frequency of intersection, f_2, will cause instability and oscillation. Introducing a pole at f_2 by adding the feedback capacitor C2 stabilizes the circuit and yields a phase margin of about 45 degrees.

$$f_2 = \frac{1}{2\pi R2C2}.$$

Since f_2 is the geometric mean of f_1 and the unity-gain bandwidth frequency of the op amp, f_u,

$$f_2 = \sqrt{f_1 \cdot f_u}.$$

These equations can be combined and solved for C2:

$$C2 = \sqrt{\frac{C1}{2\pi R2 \cdot f_u}}.$$

This value of C2 will yield a phase margin of about 45 degrees. Increasing the capacitor by a factor of 2 increases the phase margin to about 65 degrees.

In practice, the optimum value of C2 should be determined experimentally by varying it slightly to optimize the output pulse response.

SELECTION OF THE OP AMP FOR WIDEBAND PHOTODIODE I/V CONVERTERS

The op amp in the high speed photodiode I/V converter should be a wideband FET-input one in order to minimize the effects of input bias current and allow low values of photocurrents to be detected. In addition, if the equation for the 3dB bandwidth, f_2, is rearranged in terms of f_u, R2, and C1, then

$$f_2 = \sqrt{\frac{f_u}{2\pi R2C1}},$$

where C1 is the sum of the diode capacitance ,C_D, and the op amp input capacitance, C_{IN}. In a high speed application, the diode capacitance will be much smaller than that of the low frequency preamplifier design previously discussed - perhaps as low as a few pF.

By inspection of this equation, it is clear that in order to maximize f_2, the FET-input op amp should have both a high unity gain-bandwidth product, f_u, and a low input capacitance, C_{IN}. In fact, the ratio of f_u to C_{IN} is a good figure-of-merit when evaluating different op amps for this application.

Figure 5.25 compares a number of FET-input op amps suitable for photodiode preamps. By inspection, the AD823 op amp has the highest ratio of unity gain-bandwidth product to input capacitance, in addition to relatively low input bias current. For these reasons, it was chosen for the wideband photodiode preamp design.

FET-INPUT OP AMP COMPARISON TABLE FOR WIDE BANDWIDTH PHOTODIODE PREAMPS

	Unity GBW Product fu (MHz)	Input Capacitance C_{IN} (pF)	f_u/C_{IN} (MHz/pF)	Input Bias Current I_B (pA)	Voltage Noise @ 10kHz (nV/√Hz)
AD823	16	1.8	8.9	3	16
AD843	34	6	5.7	600	19
AD744	13	5.5	2.4	100	16
AD845	16	8	2	500	18
OP42	10	6	1.6	100	12
AD745*	20	20	1	250	2.9
AD795	1	1	1	1	8
AD820	1.9	2.8	0.7	2	13
AD743	4.5	20	0.2	250	2.9

***Stable for Noise Gains ≥ 5, Usually the Case, Since High Frequency Noise Gain = 1 + C1/C2, and C1 Usually ≥ 4C2**

Figure 5.25

HIGH SPEED PHOTODIODE PREAMP DESIGN

The HP 5082-4204 PIN Photodiode will be used as an example for our discussion. Its characteristics are given in Figure 5.26. It is typical of many commercially available PIN photodiodes. As in most high-speed photodiode applications, the diode is operated in the reverse-biased or *photoconductive* mode. This greatly lowers the diode junction capacitance, but causes a small amount of *dark current* to flow even when the diode is not illuminated (we will show a circuit which compensates for the dark current error later in the section).

This photodiode is linear with illumination up to approximately 50 to 100µA of output current. The dynamic range is limited by the total circuit noise and the diode dark current (assuming no dark current compensation).

HP 5082-4204 PHOTODIODE

- **Sensitivity: 350µA @ 1mW, 900nm**
- **Maximum Linear Output Current: 100µA**
- **Area: 0.002cm^2 (0.2mm^2)**
- **Capacitance: 4pF @ 10V Reverse Bias**
- **Shunt Resistance: $10^{11}\Omega$**
- **Risetime: 10ns**
- **Dark Current: 600pA @ 10V Reverse Bias**

Figure 5.26

Using the circuit shown in Figure 5.27, assume that we wish to have a full scale output of 10V for a diode current of 100µA. This determines the value of the feedback resistor R2 to be 10V/100µA = 100kΩ.

Using the diode capacitance, C_D=4pF, and the AD823 input capacitance, C_{IN} =1.8pF, the value of C1 = C_D+C_{IN} = 5.8pF. Solving the above equations using C1=5.8pF, R2=100kΩ, and f_u=16MHz, we find that:

f_1 = 274kHz
C2 = 0.76pF
f_2 = 2.1MHz.

In the final design (Figure 5.27), note that the 100kΩ resistor is replaced with three 33.2kΩ film resistors to minimize stray capacitance. The feedback capacitor, C2, is a variable 1.5pF ceramic and is adjusted in the final circuit for best bandwidth/pulse response. The overall circuit bandwidth is approximately 2MHz.

The full scale output voltage of the preamp for 100µA diode current is 10V, and the error (RTO) due to the photodiode dark current of 600pA is 60mV. The dark current error can be canceled using a second photodiode of the same type in the non-inverting input of the op amp as shown in Figure 5.27.

2MHz BANDWIDTH PHOTODIODE PREAMP WITH DARK CURRENT COMPENSATION

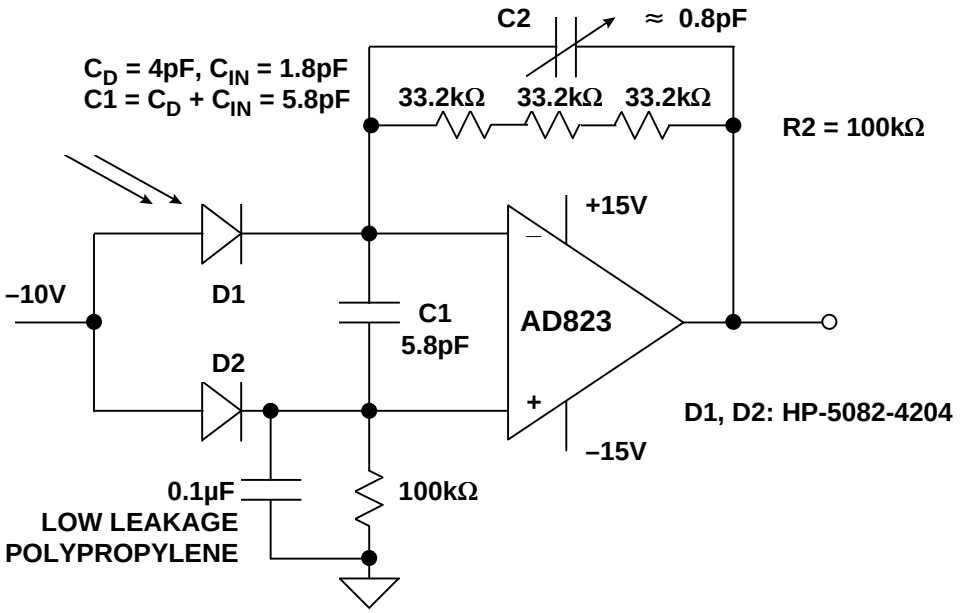


Figure 5.27

HIGH SPEED PHOTODIODE PREAMP NOISE ANALYSIS

As in most noise analyses, only the key contributors need be identified. Because the noise sources combine in an RSS manner, any single noise source that is at least three or four times as large as any of the others will dominate.

In the case of the wideband photodiode preamp, the dominant sources of output noise are the input voltage noise of the op amp, V_N, and the resistor noise due to R2, $V_{N,R2}$ (see Figure 5.28). The input current noise of the FET-input op amp is negligible. The shot noise of the photodiode (caused by the reverse bias) is negligible because of the filtering effect of the shunt capacitance C1. The resistor noise is easily calculated by knowing that a 1kΩ resistor generates about 4nV/√Hz, therefore, a 100kΩ resistor generates 40nV/√Hz. The bandwidth for integration is the signal bandwidth, 2.1MHz, yielding a total output rms noise of:

$$V_{N,R2}\ \text{RTO NOISE} = 40\sqrt{1.57 \cdot 2.1 \cdot 10^6} = 73\mu\text{Vrms}.$$

The factor of 1.57 converts the approximate single-pole bandwidth of 2.1MHz into the *equivalent noise bandwidth*.

The output noise due to the input voltage noise is obtained by multiplying the noise gain by the voltage noise and integrating the entire function over frequency. This would be tedious if done rigorously, but a few reasonable approximations can be made which greatly simplify the math. Obviously, the low frequency 1/f noise can be neglected in the case of the wideband circuit. The primary source of output noise is due to the high-frequency noise-gain peaking which occurs between f_1 and f_u. If we simply assume that the output noise is constant over the entire range of frequencies and use the maximum value for AC noise gain [1+(C1/C2)], then

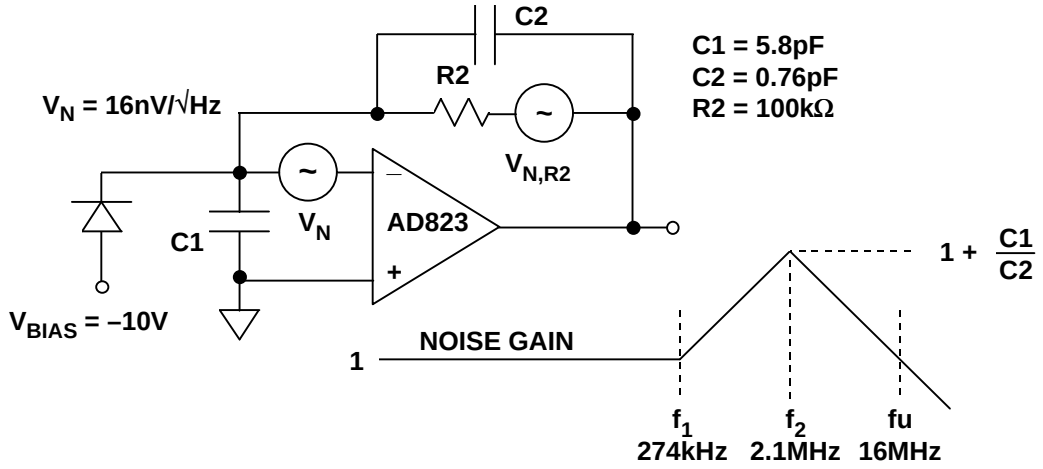
$$V_N \text{ RTO NOISE} \approx V_N\left(1+\frac{C1}{C2}\right)\sqrt{1.57f_2} = 250\mu Vrms\,.$$

The total rms noise referred to the output is then the RSS value of the two components:

$$\text{TOTAL RTO NOISE} = \sqrt{(73)^2+(250)^2} = 260\mu Vrms\,.$$

The total output dynamic range can be calculated by dividing the full scale output signal (10V) by the total output rms noise, 260μVrms, and converting to dB, yielding approximately 92dB.

EQUIVALENT CIRCUIT FOR OUTPUT NOISE ANALYSIS



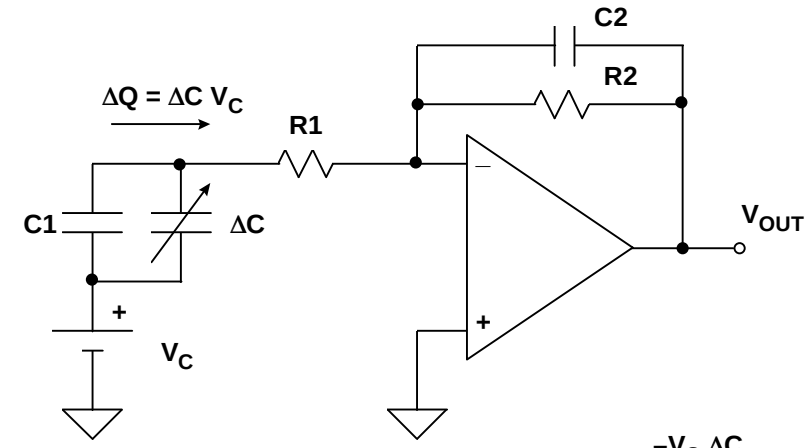
- V_N RTO NOISE $\approx V_N\left[1+\frac{C1}{C2}\right]\sqrt{1.57\,f_2}$ = 250μV RMS
- $V_{N,R2}$ RTO NOISE $\approx \sqrt{4kTR2 \bullet 1.57f_2}$ = 73μV RMS
- TOTAL RTO NOISE $= \sqrt{250^2 + 73^2}$ = 260μV RMS
- DYNAMIC RANGE = $20 \log\left[\frac{10V}{260\mu V}\right]$ = 92dB

Figure 5.28

HIGH IMPEDANCE CHARGE OUTPUT SENSORS

High impedance transducers such as piezoelectric sensors, hydrophones, and some accelerometers require an amplifier which converts a transfer of charge into a change of voltage. Because of the high DC output impedance of these devices, appropriate buffers are required. The basic circuit for an inverting charge sensitive amplifier is shown in Figure 5.29. There are basically two types of charge transducers: capacitive and charge-emitting. In a capacitive transducer, the voltage across the capacitor (V_C) is held constant. The change in capacitance, ΔC, produces a change in charge, $\Delta Q = \Delta C V_C$. This charge is transferred to the op amp output as a voltage, $\Delta V_{OUT} = -\Delta Q/C2 = -\Delta C V_C/C2$.

CHARGE AMPLIFIER FOR CAPACITIVE SENSOR



- FOR CAPACITIVE SENSORS: $\Delta V_{OUT} = \dfrac{-V_C\,\Delta C}{C2}$
- FOR CHARGE-EMITTING SENSORS: $\Delta V_{OUT} = \dfrac{-\Delta Q}{C2}$
- UPPER CUTOFF FREQUENCY = $f_2 = \dfrac{1}{2\pi\, R2\, C2}$
- LOWER CUTOFF FREQUENCY = $f_1 = \dfrac{1}{2\pi\, R1\, C1}$

Figure 5.29

Charge-emitting transducers produce an output charge, ΔQ, and their output capacitance remains constant. This charge would normally produce an open-circuit output voltage at the transducer output equal to $\Delta Q/C$. However, since the voltage across the transducer is held constant by the virtual ground of the op amp (R1 is usually small), the charge is transferred to capacitor C_2 producing an output voltage $\Delta V_{OUT} = -\Delta Q/C2$.

In an actual application, the charge amplifier only responds to AC inputs. The upper cutoff frequency is given by $f_2 = 1/2\pi R2C2$, and the lower by $f_1 = 1/2\pi R1C1$.

LOW NOISE CHARGE AMPLIFIER CIRCUIT CONFIGURATIONS

Figure 5.30 shows two ways to buffer and amplify the output of a charge output transducer. Both require using an amplifier which has a very high input impedance, such as the AD745. The AD745 provides both low voltage and low current noise. This combination makes this device particularly suitable in applications requiring very high charge sensitivity, such as capacitive accelerometers and hydrophones.

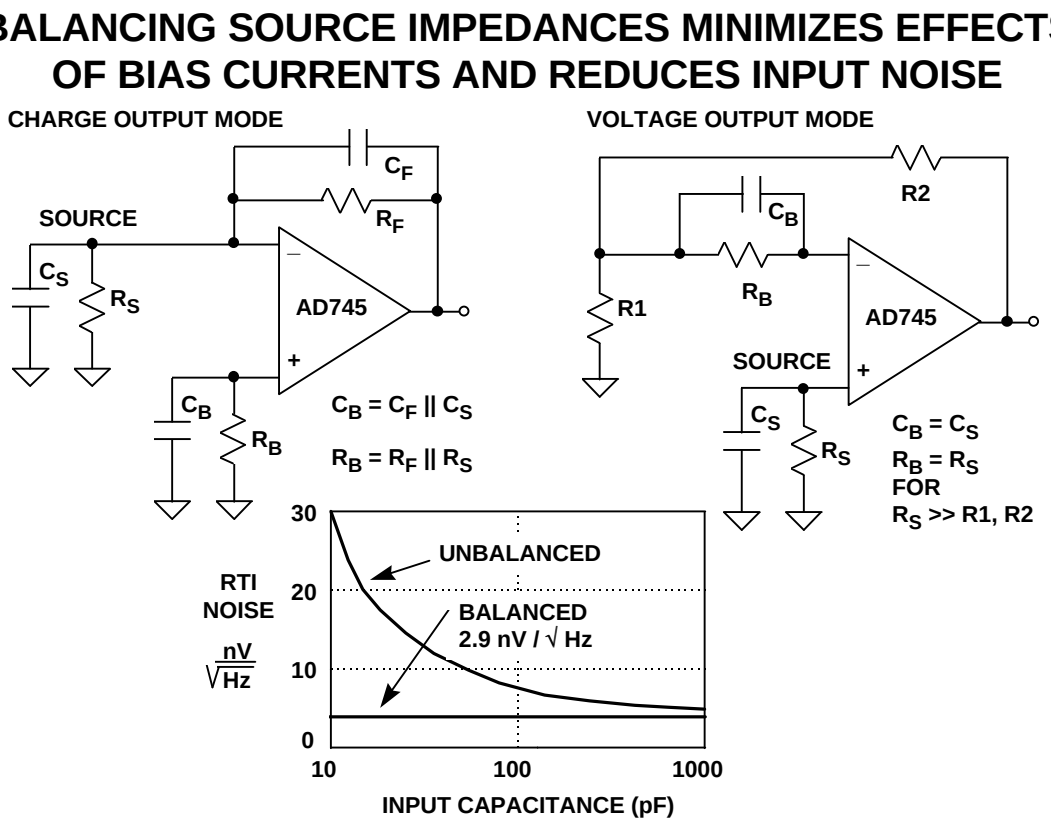


Figure 5.30

The first circuit (left) in Figure 5.30 uses the op amp in the inverting mode. Amplification depends on the principle of conservation of charge at the inverting input of the amplifier. The charge on capacitor C_S is transferred to capacitor C_F, thus yielding an output voltage of $\Delta Q/C_F$. The amplifier's input voltage noise will appear at the output amplified by the AC noise gain of the circuit, $1 + C_S/C_F$.

The second circuit (right) shown in Figure 5.30 is simply a high impedance follower with gain. Here the noise gain (1 + R2/R1) is the same as the gain from the transducer to the output. Resistor R_B , in both circuits, is required as a DC bias current return.

To maximize DC performance over temperature, the source resistances should be balanced on each input of the amplifier. This is represented by the resistor R_B shown in Figure 5.30. For best noise performance, the source capacitance should also be balanced with the capacitor C_B. In general, it is good practice to balance the source impedances (both resistive and reactive) as seen by the inputs of a precision low noise BiFET amplifiers such as the AD743/AD745. Balancing the resistive

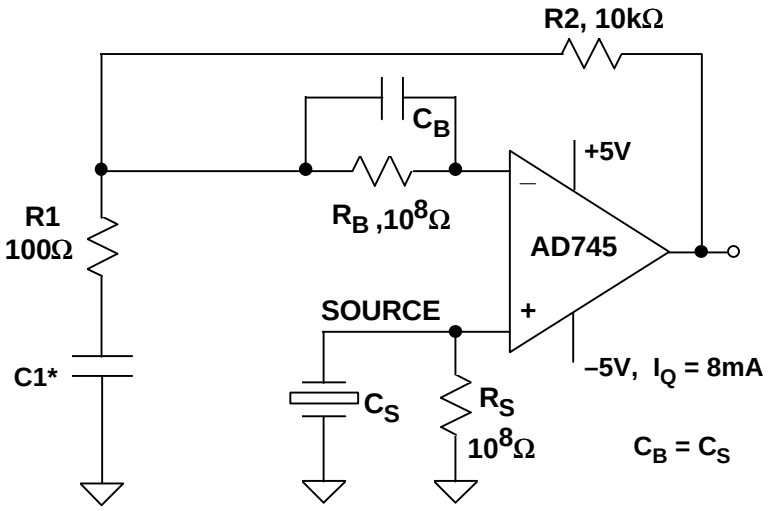
components will optimize DC performance over temperature because balancing will mitigate the effects of any bias current errors. Balancing the input capacitance will minimize AC response errors due to the amplifier's non-linear common mode input capacitance, and as shown in Figure 5.30, noise performance will be optimized. In any FET input amplifier, the current noise of the internal bias circuitry can be coupled to the inputs via the gate-to-source capacitances (20pF for the AD743 and AD745) and appears as excess input voltage noise. This noise component is correlated at the inputs, so source impedance matching will tend to cancel out its effect. Figure 5.30 shows the required external components for both inverting and noninverting configurations. For values of C_B greater than 300pF, there is a diminishing impact on noise, and C_B can then be simply a large mylar bypass capacitor of 0.01µF or greater.

A 40dB GAIN PIEZOELECTRIC TRANSDUCER AMPLIFIER OPERATES ON REDUCED SUPPLY VOLTAGES FOR LOWER BIAS CURRENT

Figure 5.31 shows a piezoelectric transducer amplifier connected in the voltage-output mode. Reducing the power supplies to ±5V reduces the effects of bias current in two ways: first, by lowering the total power dissipation and, second, by reducing the basic gate-to-junction leakage current. The addition of a clip-on heat sink such as the Aavid #5801will further limit the internal junction temperature rise.

Without the AC coupling capacitor C1, the amplifier will operate over a range of 0°C to +85°C. If the optional AC coupling capacitor C1 is used, the circuit will operate over the entire –55°C to +125°C temperature range, but DC information is lost.

GAIN OF 100 PIEZOELECTRIC SENSOR AMPLIFIER



- ±5V Power Supplies Reduce I_B for 0°C to +85°C Operation, P_D = 80mW
- C1 Allows –55°C to +125°C Operation

Figure 5.31

HYDROPHONES

Interfacing the outputs of highly capacitive transducers such as hydrophones, some accelerometers, and condenser microphones to the outside world presents many design challenges. Previously designers had to use costly hybrid amplifiers consisting of discrete low-noise JFETs in front of conventional op amps to achieve the low levels of voltage and current noise required by these applications. Now, using the AD743 and AD745, designers can achieve almost the same level of performance of the hybrid approach in a monolithic solution.

In sonar applications, a piezo-ceramic cylinder is commonly used as the active element in the hydrophone. A typical cylinder has a nominal capacitance of around 6,000pF with a series resistance of 10Ω. The output impedance is typically $10^8\Omega$ or 100MΩ.

Since the hydrophone signals of interest are inherently AC with wide dynamic range, noise is the overriding concern among sonar system designers. The noise floor of the hydrophone and the hydrophone preamplifier together limit the sensitivity of the system and therefore the overall usefulness of the hydrophone. Typical hydrophone bandwidths are in the 1kHz to 10kHz range. The AD743 and AD745 op amps, with their low noise figures of 2.9nV/$\sqrt{\text{Hz}}$ and high input impedance of $10^{10}\Omega$ (or 10GΩ) are ideal for use as hydrophone amplifiers.

The AD743 and AD745 are companion amplifiers with different levels of internal compensation. The AD743 is internally compensated for unity gain stability. The AD745, stable for noise gains of 5 or greater, has a much higher bandwidth and slew rate. This makes the AD745 especially useful as a high-gain preamplifier where it provides both high gain and wide bandwidth. The AD743 and AD745 also operate with extremely low levels of distortion: less than 0.0003% and 0.0002% (at 1kHz), respectively.

OP AMP PERFORMANCE: JFET VERSUS BIPOLAR

The AD743 and AD745 op amps are the first monolithic JFET devices to offer the low input voltage noise comparable to a bipolar op amp without the high input bias currents typically associated with bipolar op amps. Figure 5.32 shows input voltage noise versus input source resistance of the bias-current compensated OP27 and the JFET-input AD745 op amps. Note that the noise levels of the AD743 and the AD745 are identical. From this figure, it is clear that at high source impedances, the low current noise of the AD745 also provides lower overall noise than a high performance bipolar op amp. It is also important to note that, with the AD745, this noise reduction extends all the way down to low source impedances. At high source impedances, the lower DC current errors of the AD745 also reduce errors due to offset and drift as shown in Figure 5.32.

EFFECTS OF SOURCE RESISTANCE ON NOISE AND OFFSET VOLTAGE FOR OP27(BIPOLAR) AND AD745 (BiFET) OP AMPS

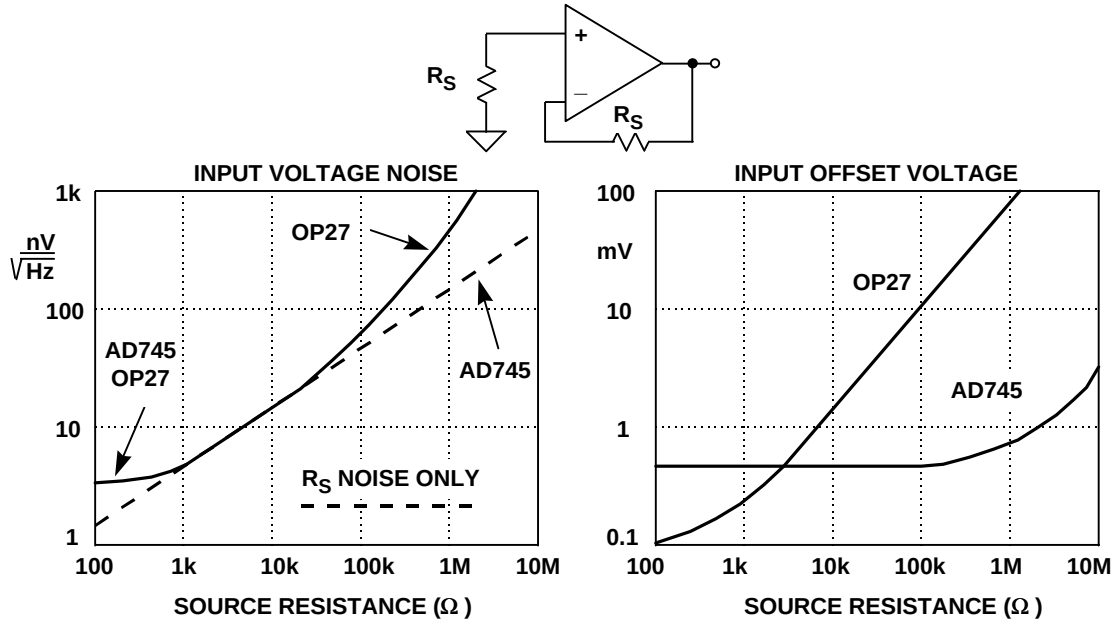


Figure 5.32

A pH PROBE BUFFER AMPLIFIER

A typical pH probe requires a buffer amplifier to isolate its 10^6 to 10^9 Ω source resistance from external circuitry. Such an amplifier is shown in Figure 5.33. The low input current of the AD795 allows the voltage error produced by the bias current and electrode resistance to be minimal. The use of guarding, shielding, high insulation resistance standoffs, and other such standard picoamp methods used to minimize leakage are all needed to maintain the accuracy of this circuit.

The slope of the pH probe transfer function, 50mV per pH unit at room temperature, has an approximate +3500ppm/°C temperature coefficient. The buffer shown in Figure 5.33 provides a gain of 20 and yields an output voltage equal to 1volt/pH unit. Temperature compensation is provided by resistor RT which is a special temperature compensation resistor,1kΩ, 1%, +3500ppm/°C, #PT146 available from Precision Resistor Co., Inc. (Reference 18).

A pH PROBE BUFFER AMPLIFIER WITH A GAIN OF 20 USING THE AD795 PRECISION BiFET OP AMP

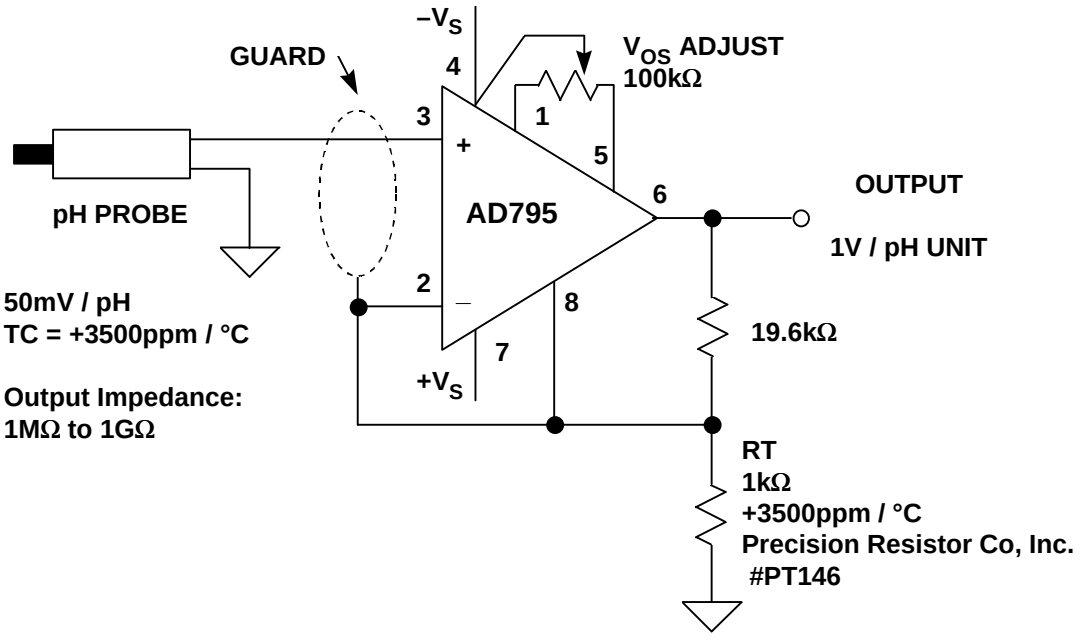


Figure 5.33

CCD/CIS IMAGE PROCESSING

The c*harge-coupled-device* (CCD) and *contact-image-sensor* (CIS) are widely used in consumer imaging systems such as scanners and digital cameras. A generic block diagram of an imaging system is shown in Figure 5.34. The imaging sensor (CCD, CMOS, or CIS) is exposed to the image or picture much like film is exposed in a camera. After exposure, the output of the sensor undergoes some analog signal processing and then is digitized by an ADC. The bulk of the actual image processing is performed using fast digital signal processors. At this point, the image can be manipulated in the digital domain to perform such functions as contrast or color enhancement/correction, etc.

The building blocks of a CCD are the individual light sensing elements called pixels (see Figure 5.35). A single pixel consists of a photo sensitive element, such as a photodiode or photocapacitor, which outputs a charge (electrons) proportional to the light (photons) that it is exposed to. The charge is accumulated during the exposure or integration time, and then the charge is transferred to the CCD shift register to be sent to the output of the device. The amount of accumulated charge will depend on the light level, the integration time, and the quantum efficiency of the photo sensitive element. A small amount of charge will accumulate even without light present; this is called dark signal or dark current and must be compensated for during the signal processing.

The pixels can be arranged in a linear or area configuration as shown in Figure 5.36. Clock signals transfer the charge from the pixels into the analog shift registers, and then more clocks are applied to shift the individual pixel charges to the output stage

of the CCD. Scanners generally use the linear configuration, while digital cameras use the area configuration. The analog shift register typically operates at frequencies between 1 and 10MHz for linear sensors, and 5 to 25MHz for area sensors.

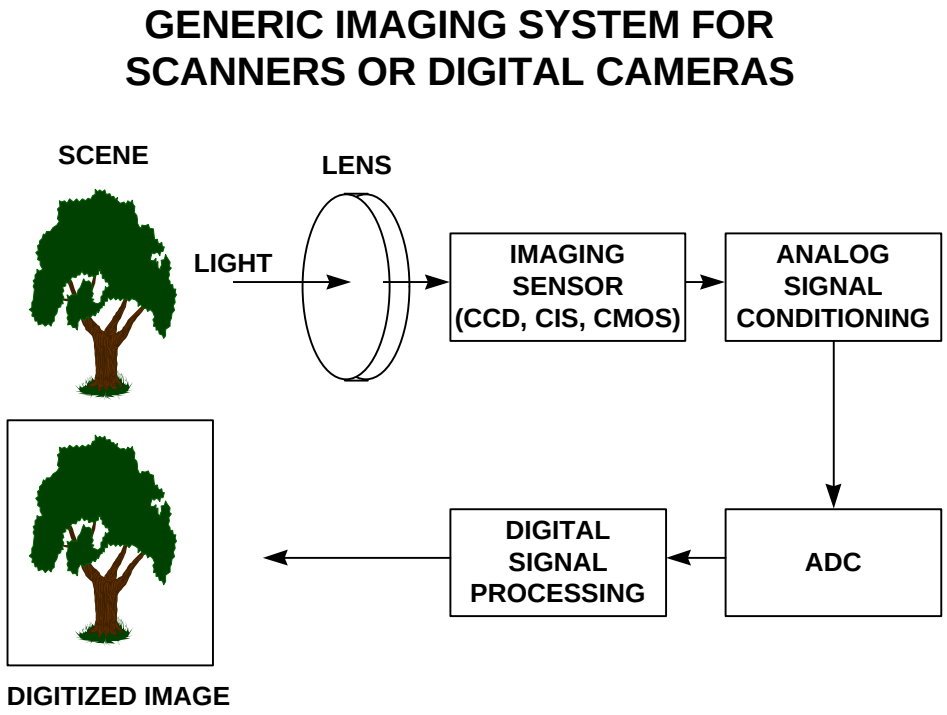


Figure 5.34

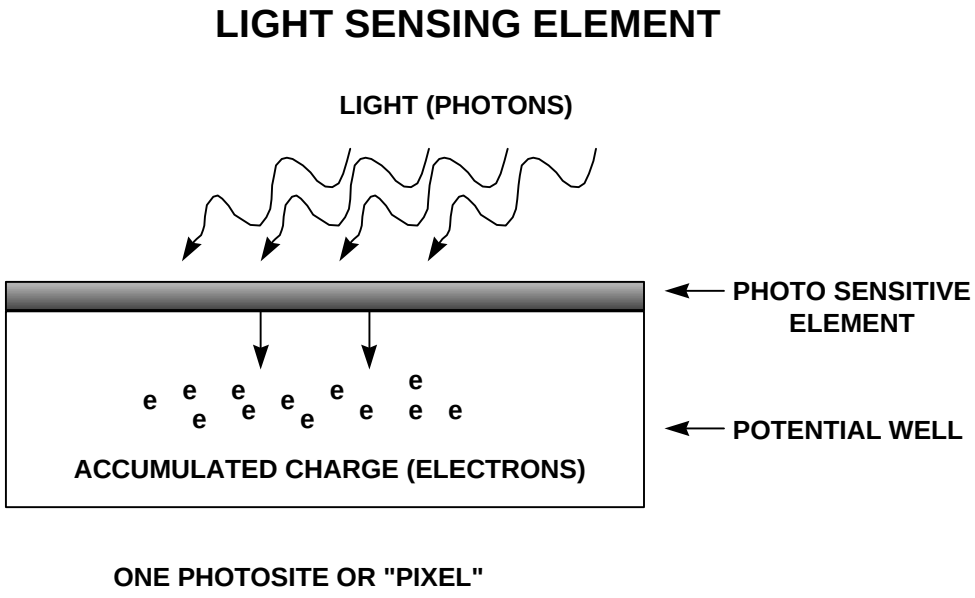


Figure 5.35

LINEAR AND AREA CCD ARRAYS

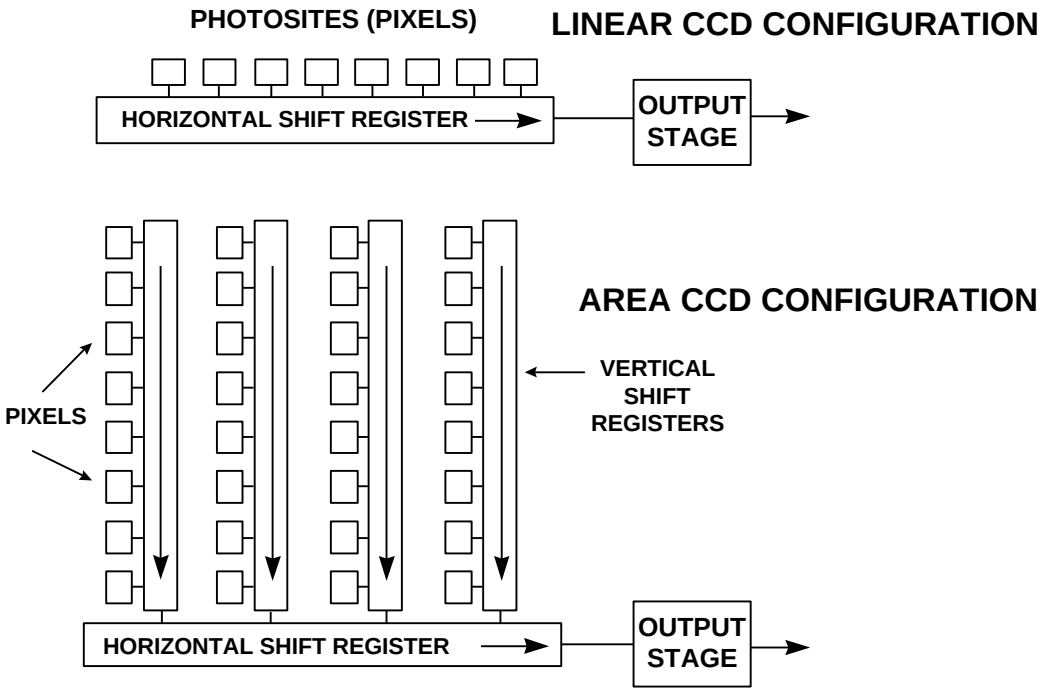


Figure 5.36

A typical CCD output stage is shown in Figure 5.37 along with the associated voltage waveforms. The output stage of the CCD converts the charge of each pixel to a voltage via the sense capacitor, C_S. At the start of each pixel period, the voltage on C_S is reset to the reference level, V_{REF} causing a reset glitch to occur. The amount of light sensed by each pixel is measured by the difference between the reference and the video level, ΔV. CCD charges may be as low as 10 electrons, and a typical CCD output has a sensitivity of 0.6μV/electron. Most CCDs have a saturation output voltage of about 500mV to 1V for area sensors and 2V to 4V for linear sensors. The DC level of the waveform is between 3 to 7V.

Since CCDs are generally fabricated on CMOS processes, they have limited capability to perform on-chip signal conditioning. Therefore the CCD output is generally processed by external conditioning circuits. The nature of the CCD output requires that it be clamped before being digitized by the ADC. In addition, offset and gain functions are generally part of the analog signal processing.

CCD output voltages are small and quite often buried in noise. The largest source of noise is the thermal noise in the resistance of the FET reset switch. This noise may have a typical value of 100 to 300 electrons rms (approximately 60 to 180mV rms). This noise, called "kT/C" noise, is illustrated in Figure 5.38. During the reset interval, the storage capacitor C_S is connected to V_{REF} via a CMOS switch. The on-resistance of the switch (R_{ON}) produces thermal noise given by the well known equation:

$$\text{Thermal Noise} = \sqrt{4kT \cdot BW \cdot R_{ON}} \ .$$

The noise occurs over a finite bandwidth determined by the R_{ON} C_S time constant. This bandwidth is then converted into equivalent noise bandwidth by multiplying the single-pole bandwidth by $\pi/2$ (1.57):

$$\text{Noise BW} = \frac{\pi}{2}\left[\frac{1}{2\pi R_{ON} C_S}\right] = \frac{1}{4 R_{ON} C_S}.$$

Substituting into the formula for the thermal noise, note that the R_{ON} factor cancels, and the final expression for the thermal noise becomes:

$$\text{Thermal Noise} = \sqrt{\frac{kT}{C}}.$$

This is somewhat intuitive, because smaller values of R_{ON} decrease the thermal noise but increase the noise bandwidth, so only the capacitor value determines the noise.

Note that when the reset switch opens, the kT/C noise is stored on C_S and remains constant until the next reset interval. It therefore occurs as a *sample-to-sample* variation in the CCD output level and is common to both the reset level and the video level for a given pixel period.

OUTPUT STAGE AND WAVEFORMS

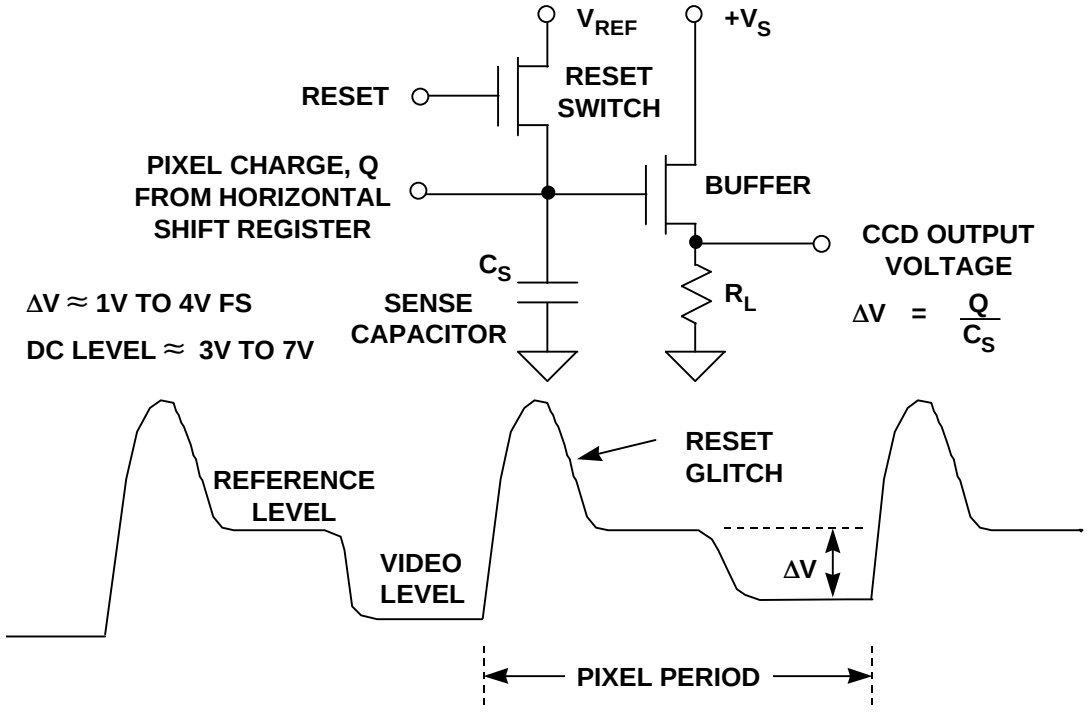
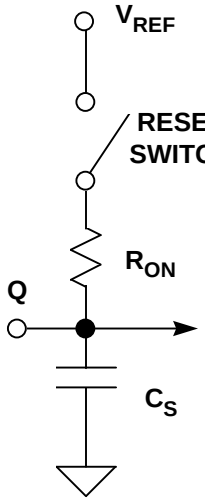


Figure 5.37

kT/C NOISE



$$\text{THERMAL NOISE} = \sqrt{4kT \cdot BW \cdot R_{ON}}$$

$$\text{NOISE BW} = \frac{\pi}{2}\left[\frac{1}{2\pi R_{ON}C_S}\right] = \frac{1}{4 R_{ON}C_S}$$

$$\text{THERMAL NOISE} = \sqrt{\frac{kT}{C_S}}$$

SAME VALUE PRESENT DURING REFERENCE AND VIDEO LEVELS WHILE RESET SWITCH IS OPEN

Figure 5.38

A technique called *correlated double sampling* (CDS) is often used to reduce the effect of this noise. Figure 5.39 shows one circuit implementation of the CDS scheme, though many other implementations exist. The CCD output drives both SHAs. At the end of the reset interval, SHA1 holds the reset voltage level plus the kT/C noise. At the end of the video interval, SHA2 holds the video level plus the kT/C noise. The SHA outputs are applied to a difference amplifier which subtracts one from the other. In this scheme, there is only a short interval during which both SHA outputs are stable, and their difference represents ΔV, so the difference amplifier must settle quickly. Note that the final output is simply the difference between the reference level and the video level, ΔV, and that the kT/C noise is removed.

Contact Image Sensors (CIS) are linear sensors often used in facsimile machines and low-end document scanners instead of CCDs. Although a CIS does not offer the same potential image quality as a CCD, it does offer lower cost and a more simplified optical path. The output of a CIS is similar to the CCD output except that it is referenced to or near ground (see Figure 5.40), eliminating the need for a clamping function. Furthermore, the CIS output does not contain correlated reset noise within each pixel period, eliminating the need for a CDS function. Typical CIS output voltages range from a few hundred mV to about 1V fullscale. Note that although a clamp and CDS is not required, the CIS waveform must be sampled by a sample-and-hold before digitization.

CORRELATED DOUBLE SAMPLING (CDS)

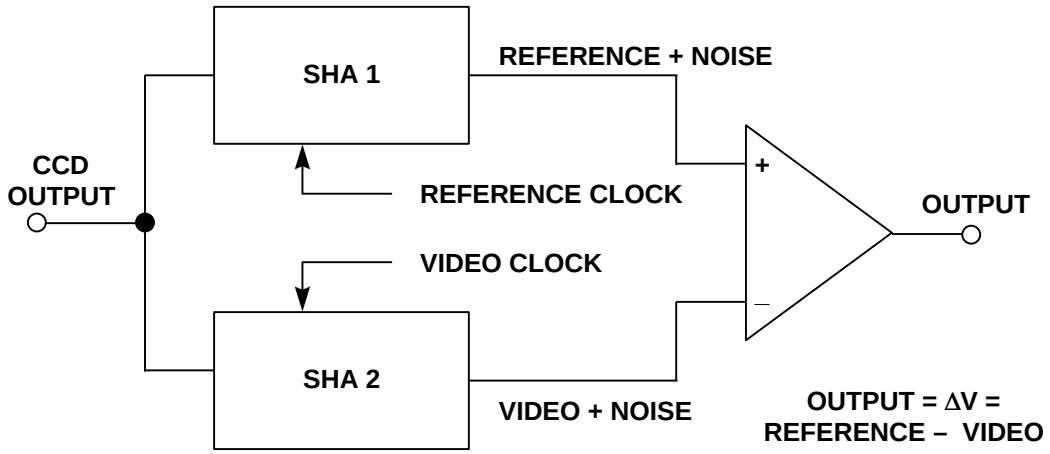


Figure 5.39

CONTACT IMAGE SENSOR (CIS) WAVEFORMS

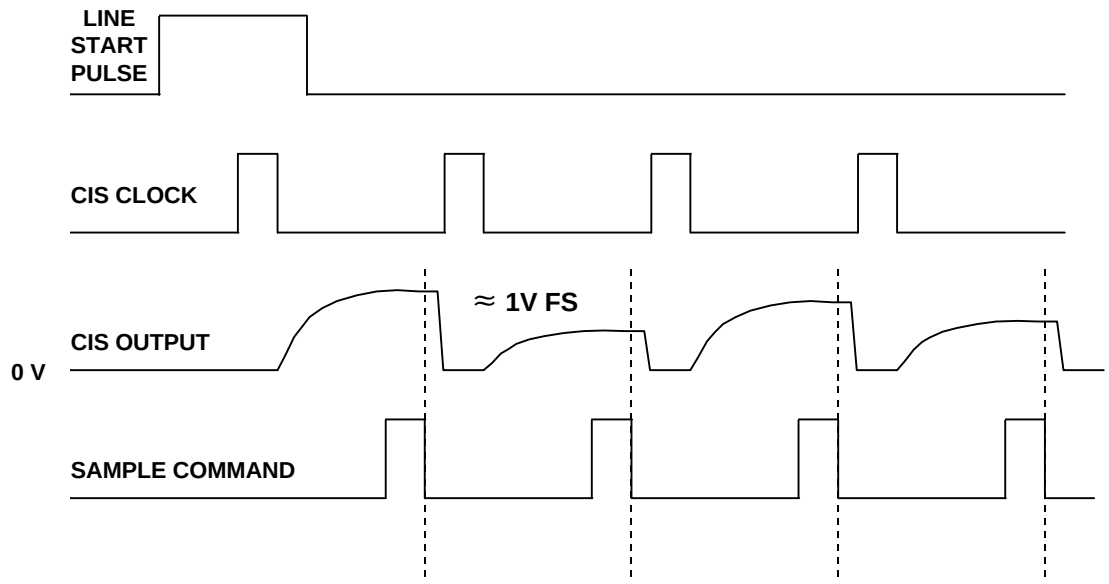


Figure 5.40

Analog Devices offers several *analog-front-end* (AFE) integrated solutions for the scanner, digital camera, and camcorder markets. They all comprise the signal processing steps described above. Advances in process technology and circuit topologies have made this level of integration possible in foundry CMOS without sacrificing performance. By combining successful ADC architectures with high performance CMOS analog circuitry, it is possible to design complete low cost CCD/CIS signal processing ICs.

The AD9816 integrates an analog-front-end (AFE) that integrates a 12-bit, 6MSPS ADC with the analog circuitry needed for three-channel (RGB) image processing and sampling (see Figure 5.41). The AD9816 can be programmed through a serial interface, and includes offset and gain adjustments that gives users the flexibility to perform all the signal processing necessary for applications such as mid- to high-end desktop scanners, digital still cameras, medical x-rays, security cameras, and any instrumentation applications that must "read" images from CIS or CCD sensors. The signal chain of the AD9816 consists of an input clamp, correlated double sampler (CDS), offset adjust DAC, programmable gain amplifier (PGA), and the 12-bit ADC core with serial interfacing to the external DSP. The CDS and clamp functions can be disabled for CIS applications.

The AD9814, Analog Devices' latest AFE product, takes the level of performance a step higher. For the most demanding applications, the AD9814 offers the same basic functionality as the AD9816 but with 14-bit performance. As with the AD9816, the signal path includes three input channels, each with input clamping, CDS, offset adjustment, and programmable gain. The three channels are multiplexed into a high performance 14-bit 6MSPS ADC. High-end document and film scanners can benefit from the AD9814's combination of performance and integration.

AD9816 ANALOG FRONT END CCD/CIS PROCESSOR

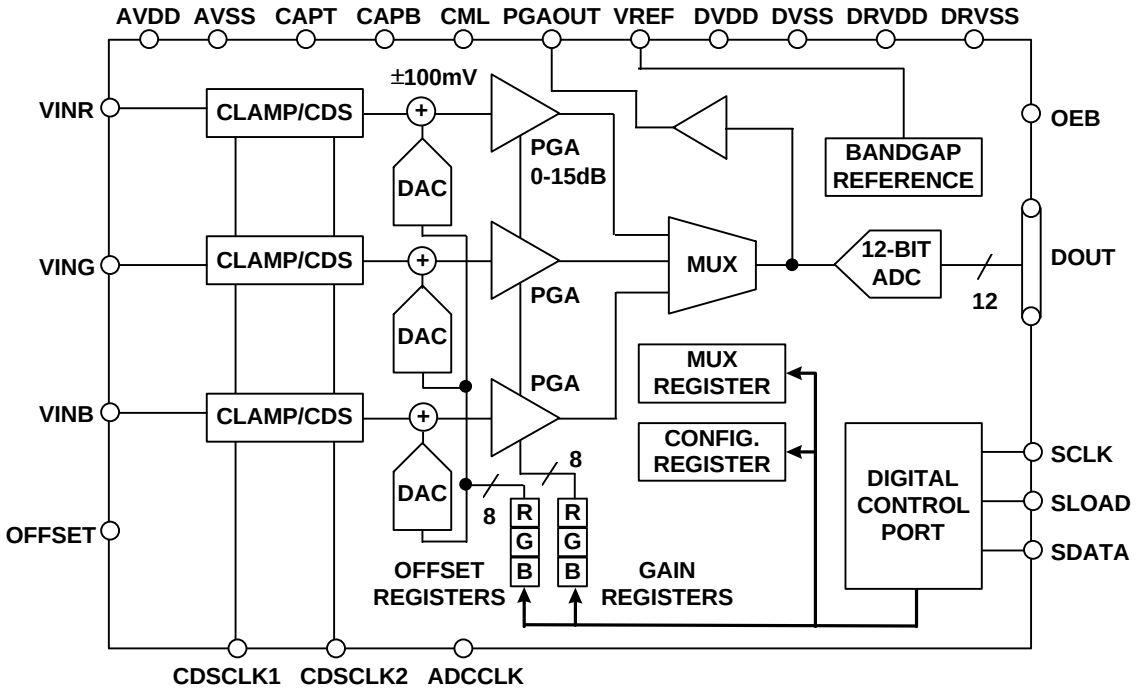


Figure 5.41

AD9816 KEY SPECIFICATIONS

- Complete 12-Bit 6MSPS CCD/CIS Signal Processor
- 3-Channel or 1-Channel Operation
- On-Chip Correlated Double Sampling (CDS)
- 8-Bit Programmable Gain and 8-Bit Offset Adjustment
- Internal Voltage Reference
- Good Linearity: DNL = ±0.4LSB Typical, INL = ±1.5 LSB Typical
- Low Output Noise: 0.5 LSB RMS
- Coarse Offset Removal for CIS Applications
- 3-Wire Serial Interface
- Single +5V Supply, 420mW Power Dissipation
- 44-Lead MQFP Package

Figure 5.42

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SECTION 6
POSITION AND MOTION SENSORS
Walt Kester

Modern linear and digital integrated circuit technology is used throughout the field of position and motion sensing. Fully integrated solutions which combine linear and digital functions have resulted in cost effective solutions to problems which in the past have been solved using expensive electro-mechanical techniques. These systems are used in many applications including robotics, computer-aided manufacturing, factory automation, avionics, and automotive.

This section is an overview of linear and rotary position sensors and their associated conditioning circuits. An interesting application of mixed-signal IC integration is illustrated in the field of AC motor control. A discussion of micromachined accelerometers ends the section.

POSITION AND MOTION SENSORS

- **Linear Position: Linear Variable Differential Transformers (LVDT)**
- **Hall Effect Sensors**
  - **Proximity Detectors**
  - **Linear Output (Magnetic Field Strength)**
- **Rotational Position:**
  - **Rotary Variable Differential Transformers (RVDT)**
  - **Optical Rotational Encoders**
  - **Synchros and Resolvers**
  - **Inductosyns (Linear and Rotational Position)**
  - **Motor Control Applications**
- **Acceleration and Tilt: Accelerometers**

Figure 6.1

LINEAR VARIABLE DIFFERENTIAL TRANSFORMERS (LVDTS)

The linear variable differential transformer (LVDT) is an accurate and reliable method for measuring linear distance. LVDTs find uses in modern machine-tool, robotics, avionics, and computerized manufacturing. By the end of World War II, the LVDT had gained acceptance as a sensor element in the process control industry largely as a result of its use in aircraft, torpedo, and weapons systems. The publication of *The Linear Variable Differential Transformer* by Herman Schaevitz in

1946 (Proceedings of the SASE, Volume IV, No. 2) made the user community at large aware of the applications and features of the LVDT.

The LVDT (see Figure 6.2) is a position-to-electrical sensor whose output is proportional to the position of a movable magnetic core. The core moves linearly inside a transformer consisting of a center primary coil and two outer secondary coils wound on a cylindrical form. The primary winding is excited with an AC voltage source (typically several kHz), inducing secondary voltages which vary with the position of the magnetic core within the assembly. The core is usually threaded in order to facilitate attachment to a nonferromagnetic rod which in turn in attached to the object whose movement or displacement is being measured.

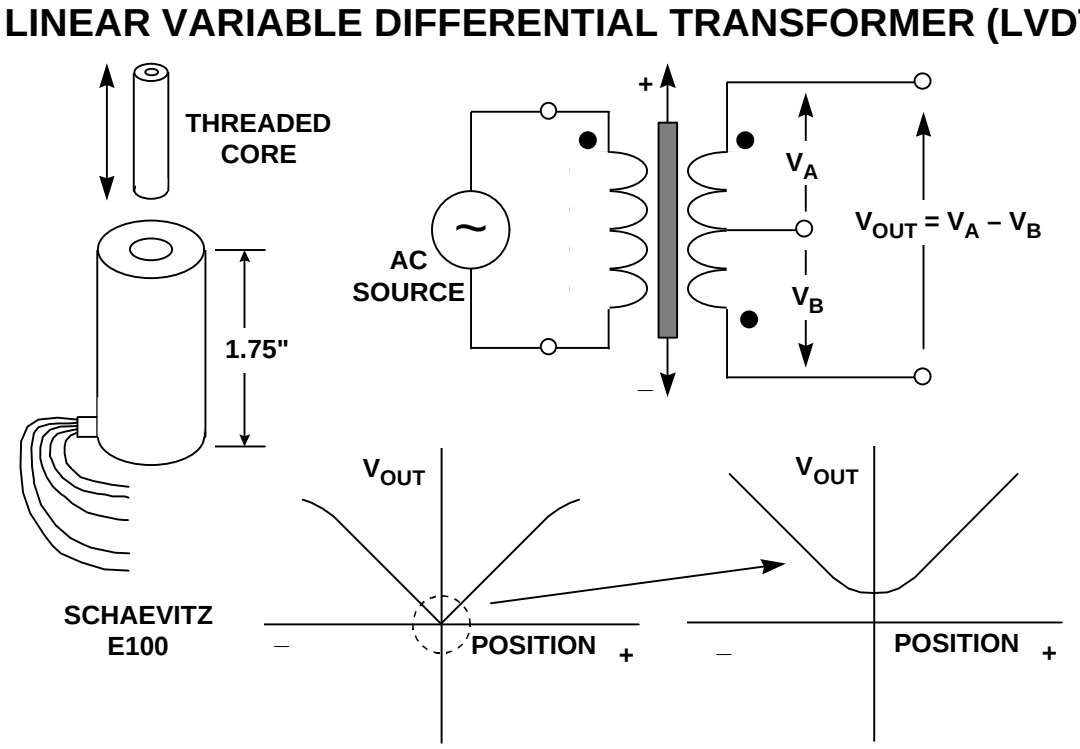


Figure 6.2

The secondary windings are wound out of phase with each other, and when the core is centered the voltages in the two secondary windings oppose each other, and the net output voltage is zero. When the core is moved off center, the voltage in the secondary toward which the core is moved increases, while the opposite voltage decreases. The result is a differential voltage output which varies linearly with the core's position. Linearity is excellent over the design range of movement, typically 0.5% or better. The LVDT offers good accuracy, linearity, sensitivity, infinite resolution, as well as frictionless operation and ruggedness.

A wide variety of measurement ranges are available in different LVDTs, typically from ±100µm to ±25cm. Typical excitation voltages range from 1V to 24V RMS, with frequencies from 50Hz to 20kHz. Key specifications for the Schaevitz E100 LVDT are given in Figure 6.3.

SCHAEVITZ E100 LVDT SPECIFICATIONS

- **Nominal Linear Range: ±0.1 inches (± 2.54mm)**
- **Input Voltage: 3V RMS**
- **Operating Frequency: 50Hz to 10kHz (2.5kHz nominal)**
- **Linearity: 0.5% Fullscale**
- **Sensitivity: 2.4mV Output / 0.001in / Volt Excitation**
- **Primary Impedance: 660Ω**
- **Secondary Impedance: 960Ω**

Figure 6.3

Note that a true null does not occur when the core is in center position because of mismatches between the two secondary windings and leakage inductance. Also, simply measuring the output voltage V_{OUT} will not tell on which side of the null position the core resides.

A signal conditioning circuit which removes these difficulties is shown in Figure 6.4 where the absolute values of the two output voltages are subtracted. Using this technique, both positive and negative variations about the center position can be measured. While a diode/capacitor-type rectifier could be used as the absolute value circuit, the precision rectifier shown in Figure 6.5 is more accurate and linear. The input is applied to a V/I converter which in turn drives an analog multiplier. The sign of the differential input is detected by the comparator whose output switches the sign of the V/I output via the analog multiplier. The final output is a precision replica of the absolute value of the input. These circuits are well understood by IC designers and are easy to implement on modern bipolar processes.

The industry-standard AD598 LVDT signal conditioner shown in Figure 6.6 (simplified form) performs all required LVDT signal processing. The on-chip excitation frequency oscillator can be set from 20Hz to 20kHz with a single external capacitor. Two absolute value circuits followed by two filters are used to detect the amplitude of the A and B channel inputs. Analog circuits are then used to generate the ratiometric function [A–B]/[A+B]. Note that this function is independent of the amplitude of the primary winding excitation voltage, assuming the sum of the LVDT output voltage amplitudes remains constant over the operating range. This is usually the case for most LVDTs, but the user should always check with the manufacturer if it is not specified on the LVDT data sheet. Note also that this approach requires the use of a 5-wire LVDT.

IMPROVED LVDT OUTPUT SIGNAL PROCESSING

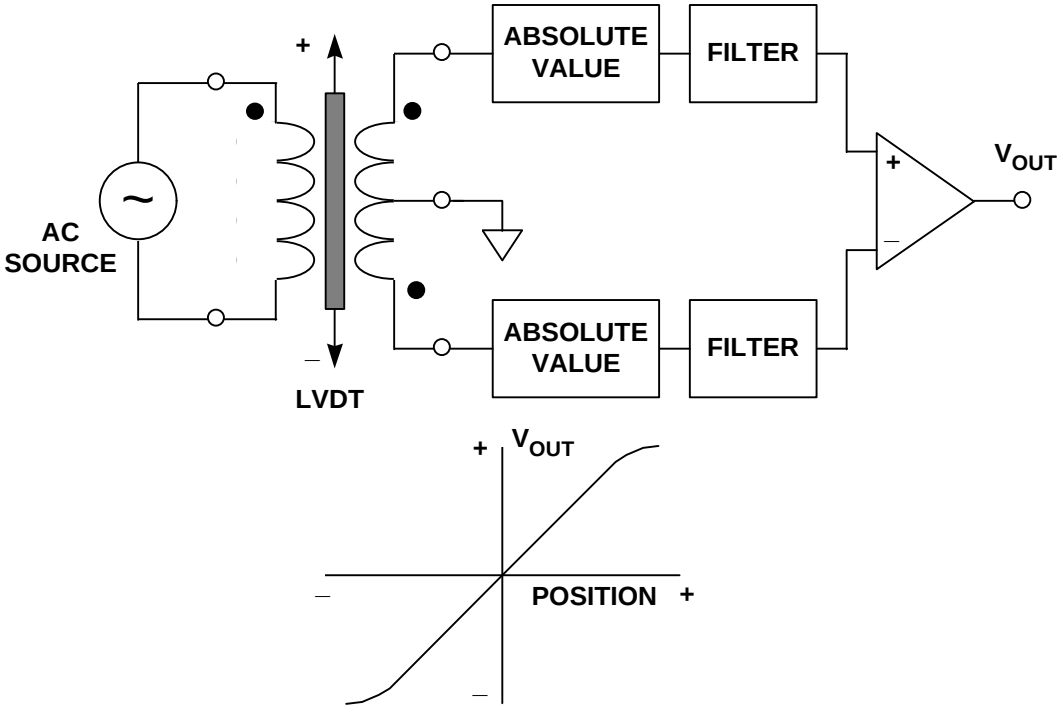


Figure 6.4

PRECISION ABSOLUTE VALUE CIRCUIT (FULL-WAVE RECTIFIER)

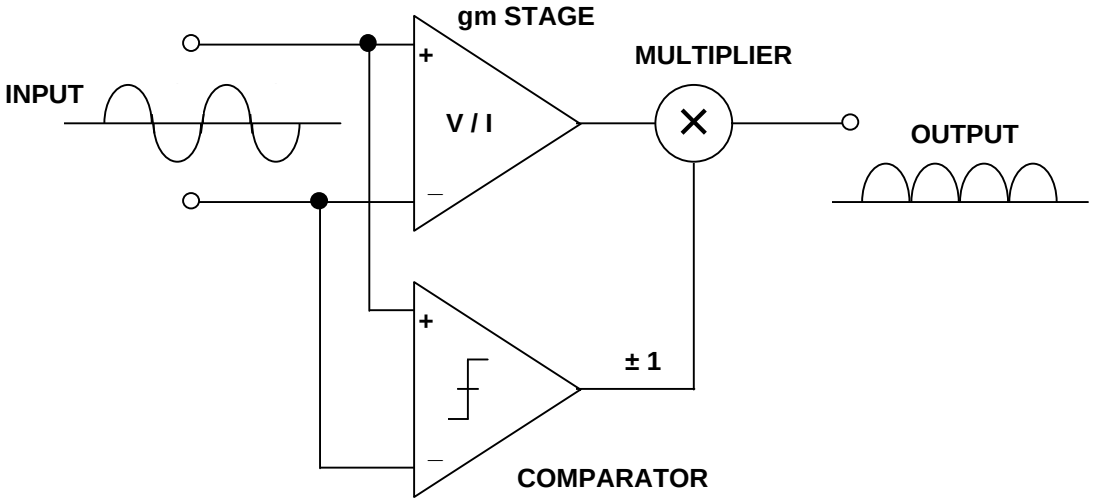


Figure 6.5

AD598 LVDT SIGNAL CONDITIONER (SIMPLIFIED)

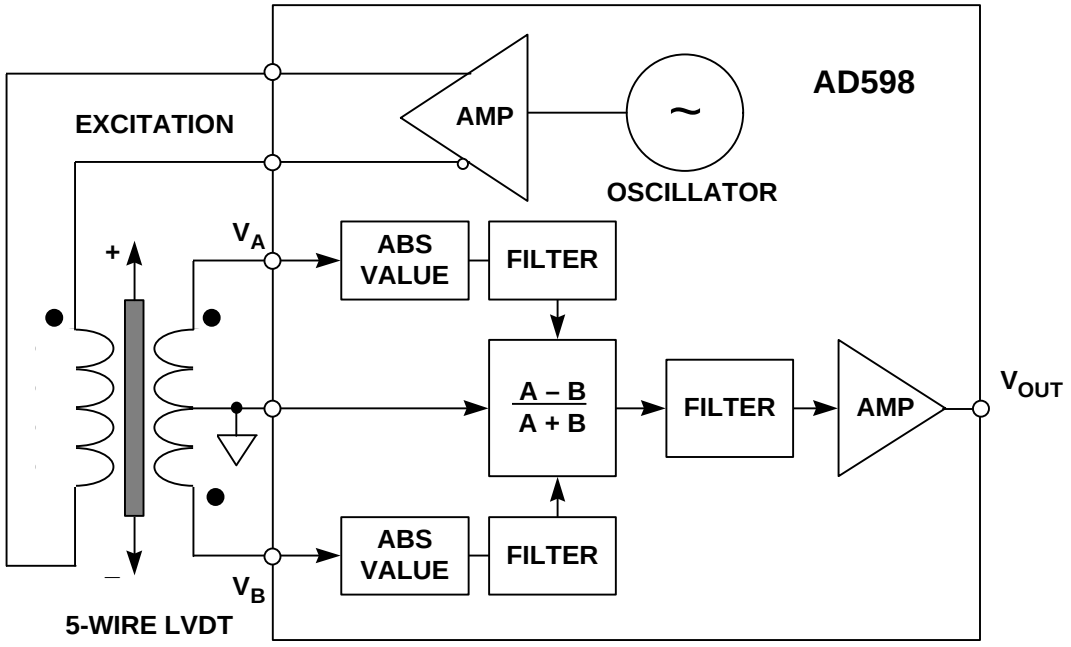


Figure 6.6

A single external resistor sets the AD598 excitation voltage from approximately 1V RMS to 24V RMS. Drive capability is 30mA RMS. The AD598 can drive an LVDT at the end of 300 feet of cable, since the circuit is not affected by phase shifts or absolute signal magnitudes. The position output range of V_{OUT} is ±11V for a 6mA load and it can drive up to 1000 feet of cable. The V_A and V_B inputs can be as low as 100mV RMS.

The AD698 LVDT signal conditioner (see Figure 6.7) has similar specifications as the AD598 but processes the signals slightly differently. Note that the AD698 operates from a 4-wire LVDT and uses synchronous demodulation. The A and B signal processors each consist of an absolute value function and a filter. The A output is then divided by the B output to produce a final output which is ratiometric and independent of the excitation voltage amplitude. Note that the sum of the LVDT secondary voltages does not have to remain constant in the AD698.

The AD698 can also be used with a half-bridge (similar to an auto-transformer) LVDT as shown in Figure 6.8. In this arrangement, the entire secondary voltage is applied to the B processor, while the center-tap voltage is applied to the A processor. The half-bridge LVDT does not produce a null voltage, and the A/B ratio represents the range-of-travel of the core.

AD698 LVDT SIGNAL CONDITIONER (SIMPLIFIED)

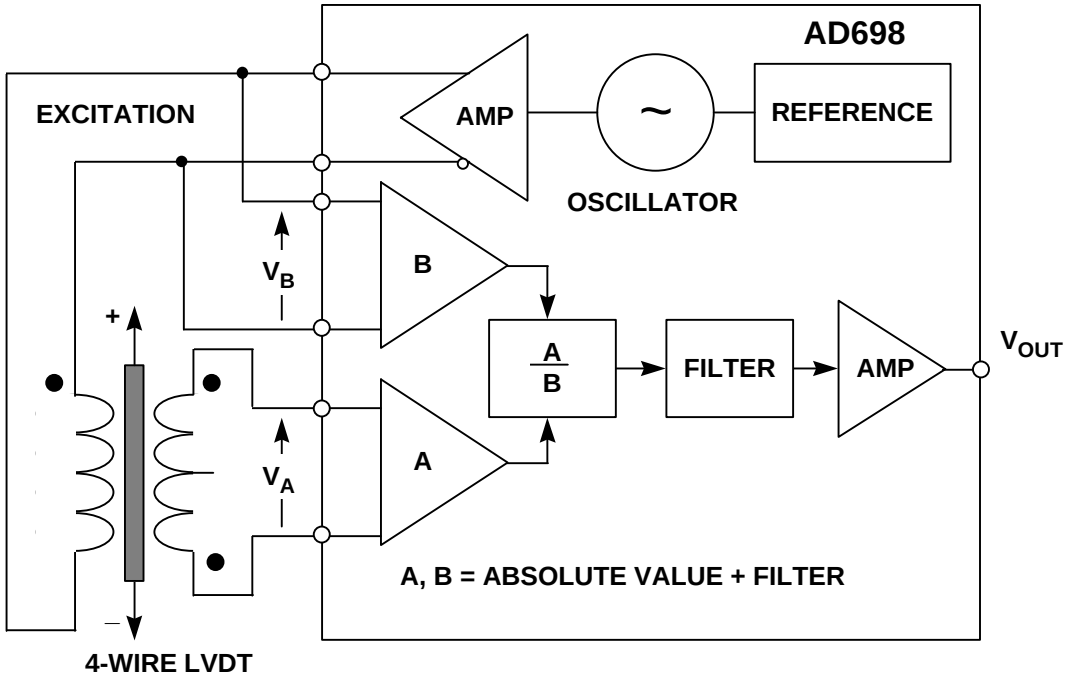


Figure 6.7

HALF-BRIDGE LVDT CONFIGURATION

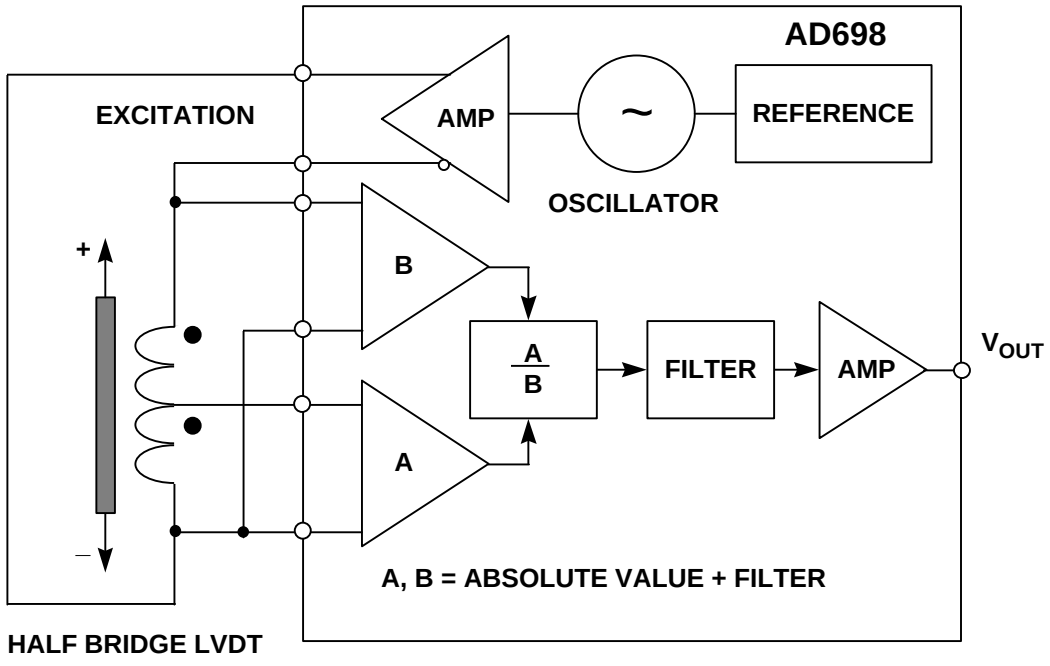


Figure 6.8

It should be noted that the LVDT concept can be implemented in rotary form, in which case the device is called a *rotary variable differential transformer* (RVDT). The shaft is equivalent to the core in an LVDT, and the transformer windings are wound on the stationary part of the assembly. However, the RVDT is linear over a relatively narrow range of rotation and is not capable of measuring a full 360º rotation. Although capable of continuous rotation, typical RVDTs are linear over a range of about ±40º about the null position (0º). Typical sensitivity is 2 to 3mV per volt per degree of rotation, with input voltages in the range of 3V RMS at frequencies between 400Hz and 20kHz. The 0º position is marked on the shaft and the body.

HALL EFFECT MAGNETIC SENSORS

If a current flows in a conductor (or semiconductor) and there is a magnetic field present which is perpendicular to the current flow, then the combination of current and magnetic field will generate a voltage perpendicular to both (see Figure 6.9). This phenomenon is called the *Hall Effect*, was discovered by E. H. Hall in 1879. The voltage, V_H, is known as the *Hall Voltage*. V_H is a function of the current density, the magnetic field, and the charge density and carrier mobility of the conductor.

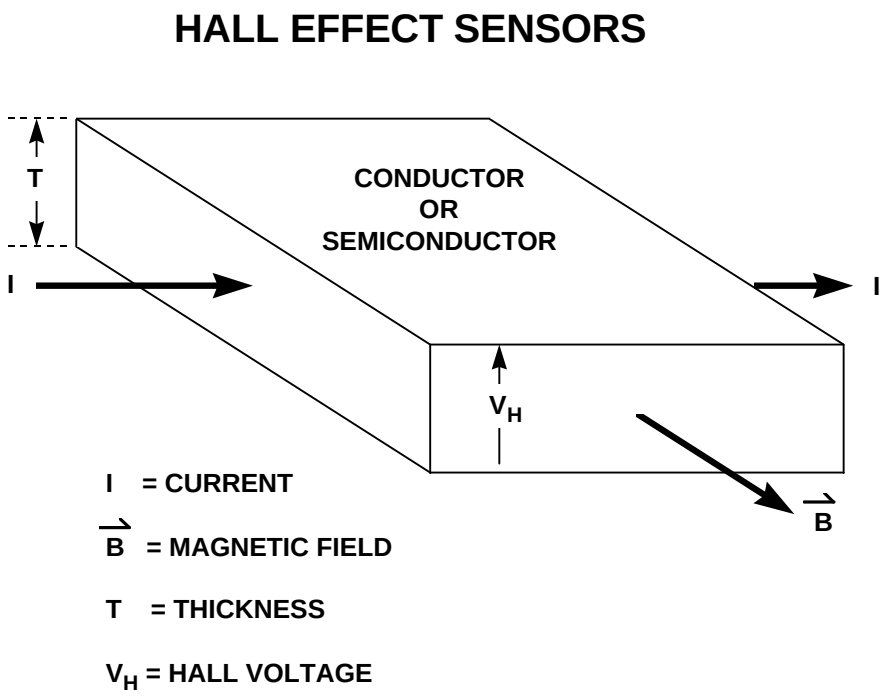


Figure 6.9

The Hall effect may be used to measure magnetic fields (and hence in contact-free current measurement), but its commonest application is in motion sensors where a fixed Hall sensor and a small magnet attached to a moving part can replace a cam and contacts with a great improvement in reliability. (Cams wear and contacts arc or become fouled, but magnets and Hall sensors are contact free and do neither.) Since V_H is proportional to magnetic field and not to rate of change of magnetic field

like an inductive sensor, the Hall Effect provides a more reliable low speed sensor than an inductive pickup.

Although several materials can be used for Hall effect sensors, silicon has the advantage that signal conditioning circuits can be integrated on the same chip as the sensor. CMOS processes are common for this application. A simple rotational speed detector can be made with a Hall sensor, a gain stage, and a comparator as shown in Figure 6.10. The circuit is designed to detect rotation speed as in automotive applications. It responds to small changes in field, and the comparator has built-in hysteresis to prevent oscillation. Several companies manufacture such Hall switches, and their usage is widespread.

HALL EFFECT SENSOR USED AS A ROTATION SENSOR

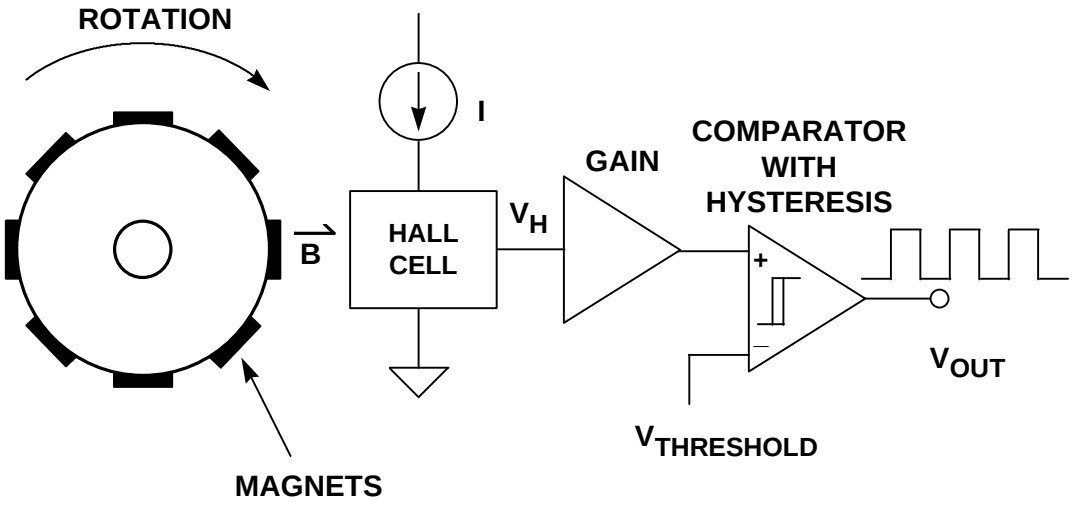


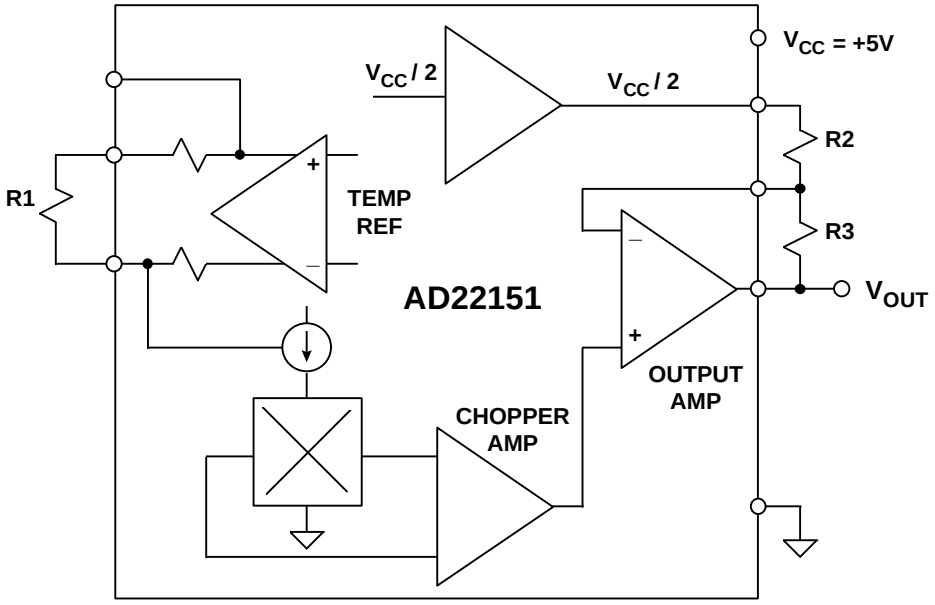
Figure 6.10

There are many other applications, particularly in automotive throttle, pedal, suspension, and valve position sensing, where a linear representation of the magnetic field is desired. The AD22151 is a linear magnetic field sensor whose output voltage is proportional to a magnetic field applied perpendicularly to the package top surface (see Figure 6.11). The AD22151 combines integrated bulk Hall cell technology and conditioning circuitry to minimize temperature related drifts associated with silicon Hall cell characteristics.

The architecture maximizes the advantages of a monolithic implementation while allowing sufficient versatility to meet varied application requirements with a minimum number of external components. Principal features include dynamic offset drift cancellation using a chopper-type op amp and a built-in temperature sensor. Designed for single +5V supply operation, low offset and gain drift allows operation over a –40ºC to +150ºC range. Temperature compensation (set externally with a resistor R1) can accommodate a number of magnetic materials commonly utilized in position sensors. Output voltage range and gain can be easily set with external resistors. Typical gain range is usually set from 2mV/Gauss to 6mV/Gauss. Output voltage can be adjusted from fully bipolar (reversible) field operation to fully

unipolar field sensing. The voltage output achieves near rail-to-rail dynamic range (+0.5V to +4.5V), capable of supplying 1mA into large capacitive loads. The output signal is ratiometric to the positive supply rail in all configurations.

AD22151 LINEAR OUTPUT MAGNETIC FIELD SENSOR



$$V_{OUT} = \left[1 + \frac{R3}{R2}\right]\left[0.4mV\right] / Gauss \qquad NONLINEARITY = 0.1\% FS$$

Figure 6.11

OPTICAL ENCODERS

Among the most popular position measuring sensors, optical encoders find use in relatively low reliability and low resolution applications. An *incremental* optical encoder (left-hand diagram in Figure 6.12) is a disc divided into sectors that are alternately transparent and opaque. A light source is positioned on one side of the disc, and a light sensor on the other side. As the disc rotates, the output from the detector switches alternately on and off, depending on whether the sector appearing between the light source and the detector is transparent or opaque. Thus, the encoder produces a stream of square wave pulses which, when counted, indicate the angular position of the shaft. Available encoder resolutions (the number of opaque and transparent sectors per disc) range from 100 to 65,000, with absolute accuracies approaching 30 arc-seconds (1/43,200 per rotation). Most incremental encoders feature a second light source and sensor at an angle to the main source and sensor, to indicate the direction of rotation. Many encoders also have a third light source and detector to sense a once-per-revolution marker. Without some form of revolution marker, absolute angles are difficult to determine. A potentially serious disadvantage is that incremental encoders require external counters to determine absolute angles within a given rotation. If the power is momentarily shut off, or if the encoder misses a pulse due to noise or a dirty disc, the resulting angular information will be in error.

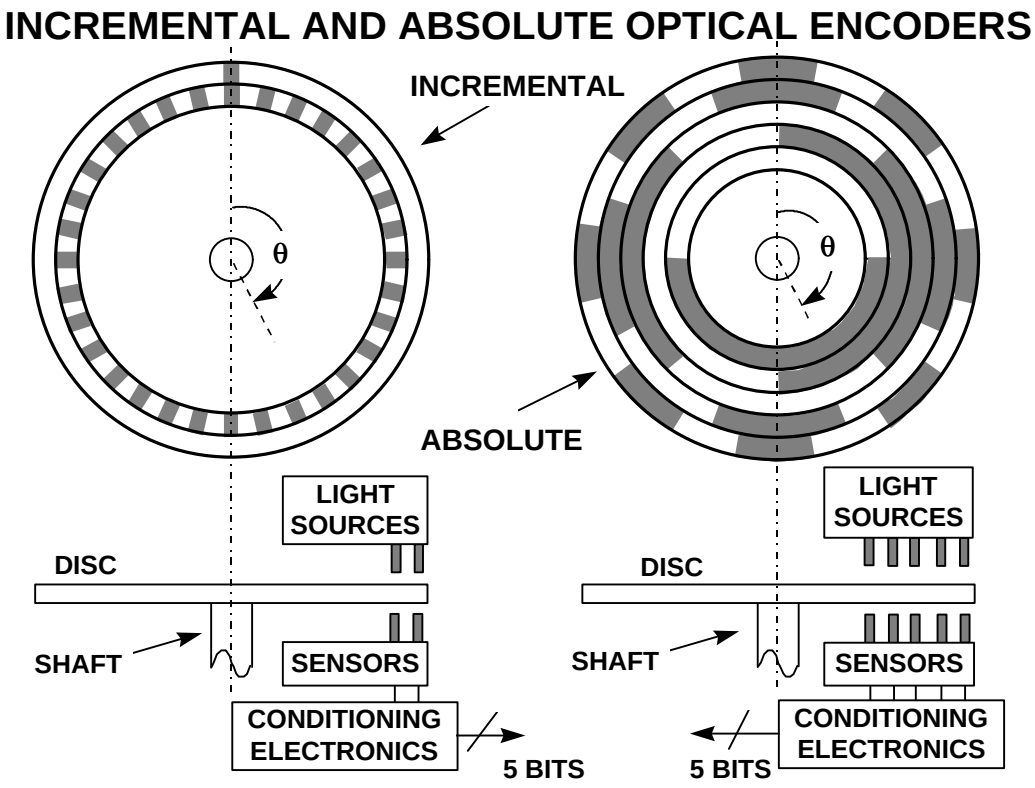


Figure 6.12

The *absolute* optical encoder (right-hand diagram in Figure 6.12) overcomes these disadvantages but is more expensive. An absolute optical encoder's disc is divided up into N sectors (N = 5 for example shown), and each sector is further divided radially along its length into opaque and transparent sections, forming a unique N-bit digital word with a maximum count of $2^N - 1$. The digital word formed radially by each sector increments in value from one sector to the next, usually employing Gray code. Binary coding could be used, but can produce large errors if a single bit is incorrectly interpreted by the sensors. Gray code overcomes this defect: the maximum error produced by an error in any single bit of the Gray code is only 1 LSB after the Gray code is converted into binary code. A set of N light sensors responds to the N-bit digital word which corresponds to the disc's absolute angular position. Industrial optical encoders achieve up to 16-bit resolution, with absolute accuracies that approach the resolution (20 arc seconds). Both absolute and incremental optical encoders, however, may suffer damage in harsh industrial environments.

RESOLVERS AND SYNCHROS

Machine-tool and robotics manufacturers have increasingly turned to resolvers and synchros to provide accurate angular and rotational information. These devices excel in demanding factory applications requiring small size, long-term reliability, absolute position measurement, high accuracy, and low-noise operation.

A diagram of a typical synchro and resolver is shown in Figure 6.13. Both sycnchros and resolvers employ single-winding rotors that revolve inside fixed stators. In the

case of a simple synchro, the stator has three windings oriented 120º apart and electrically connected in a Y-connection. Resolvers differ from synchros in that their stators have only two windings oriented at 90º.

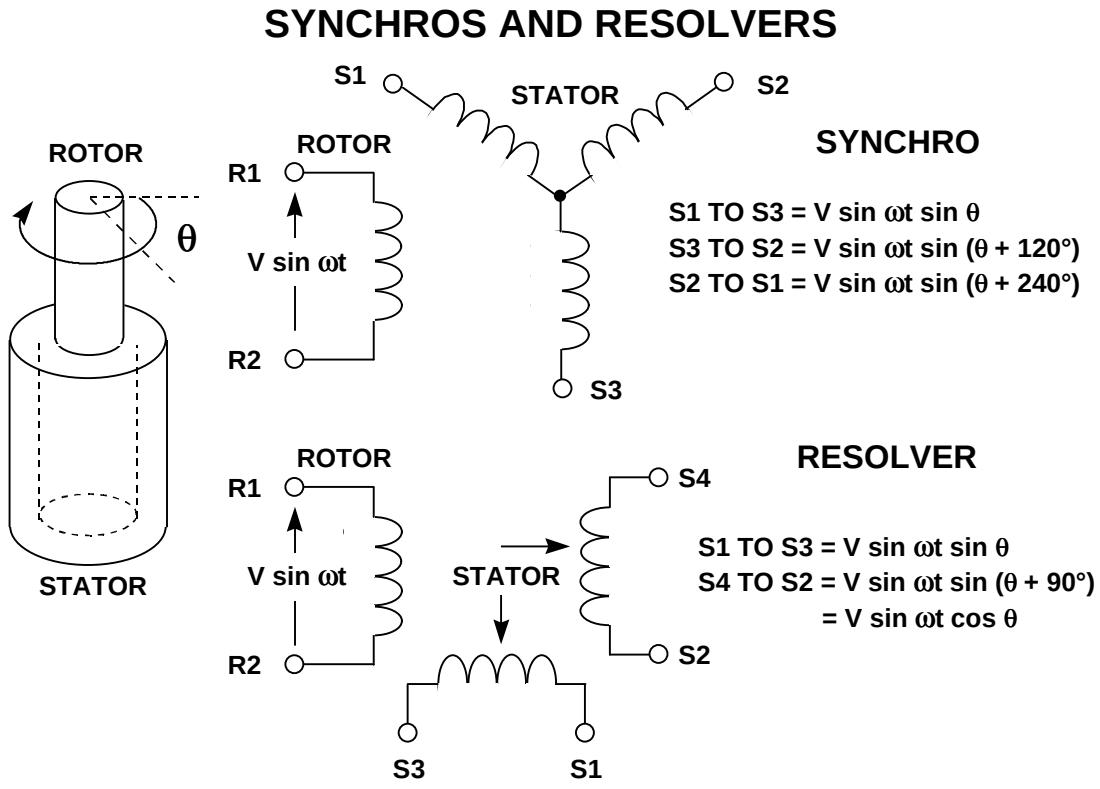


Figure 6.13

Because synchros have three stator coils in a 120º orientation, they are more difficult than resolvers to manufacture and are therefore more costly. Today, synchros find decreasing use, except in certain military and avionic retrofit applications.

Modern resolvers, in contrast, are available in a brushless form that employ a transformer to couple the rotor signals from the stator to the rotor. The primary winding of this transformer resides on the stator, and the secondary on the rotor. Other resolvers use more traditional brushes or slip rings to couple the signal into the rotor winding. Brushless resolvers are more rugged than synchros because there are no brushes to break or dislodge, and the life of a brushless resolver is limited only by its bearings. Most resolvers are specified to work over 2V to 40V RMS and at frequencies from 400Hz to 10kHz. Angular accuracies range from 5 arc-minutes to 0.5 arc-minutes. (There are 60 arc-minutes in one degree, and 60 arc-seconds in one arc-minute. Hence, one arc-minute is equal to 0.0167 degrees).

In operation, synchros and resolvers resemble rotating transformers. The rotor winding is excited by an AC reference voltage, at frequencies up to a few kHz. The magnitude of the voltage induced in any stator winding is proportional to the sine of the angle, θ, between the rotor coil axis and the stator coil axis. In the case of a synchro, the voltage induced across any pair of stator terminals will be the vector sum of the voltages across the two connected coils.

For example, if the rotor of a synchro is excited with a reference voltage, $V\sin\omega t$, across its terminals R1 and R2, then the stator's terminal will see voltages in the form:

$$S1 \text{ to } S3 = V \sin\omega t \sin\theta$$
$$S3 \text{ to } S2 = V \sin\omega t \sin(\theta + 120^o)$$
$$S2 \text{ to } S1 = V \sin\omega t \sin(\theta + 240^o),$$

where θ is the shaft angle.

In the case of a resolver, with a rotor AC reference voltage of $V\sin\omega t$, the stator's terminal voltages will be:

$$S1 \text{ to } S3 = V \sin\omega t \sin\theta$$
$$S4 \text{ to } S2 = V \sin\omega t \sin(\theta + 90^o) = V \sin\omega t \cos\theta.$$

It should be noted that the 3-wire synchro output can be easily converted into the resolver-equivalent format using a Scott-T transformer. Therefore, the following signal processing example describes only the resolver configuration.

A typical resolver-to-digital converter (RDC) is shown functionally in Figure 6.14. The two outputs of the resolver are applied to cosine and sine multipliers. These multipliers incorporate sine and cosine lookup tables and function as multiplying digital-to-analog converters. Begin by assuming that the current state of the up/down counter is a digital number representing a trial angle, φ. The converter seeks to adjust the digital angle, φ, continuously to become equal to, and to track θ, the analog angle being measured. The resolver's stator output voltages are written as:

$$V_1 = V \sin\omega t \sin\theta$$
$$V_2 = V \sin\omega t \cos\theta$$

where θ is the angle of the resolver's rotor. The digital angle φ is applied to the cosine multiplier, and its cosine is multiplied by V_1 to produce the term:

$$V \sin\omega t \sin\theta \cos\varphi.$$

The digital angle φ is also applied to the sine multiplier and multiplied by V_2 to product the term:

$$V \sin\omega t \cos\theta \sin\varphi.$$

These two signals are subtracted from each other by the error amplifier to yield an AC error signal of the form:

$$V \sin\omega t [\sin\theta \cos\varphi - \cos\theta \sin\varphi].$$

Using a simple trigonometric identity, this reduces to:

$$V \sin\omega t [\sin(\theta - \varphi)].$$

The detector synchronously demodulates this AC error signal, using the resolver's rotor voltage as a reference. This results in a DC error signal proportional to $\sin(\theta-\varphi)$.

The DC error signal feeds an integrator, the output of which drives a voltage-controlled-oscillator (VCO). The VCO, in turn, causes the up/down counter to count in the proper direction to cause:

$$\sin(\theta - \varphi) \rightarrow 0.$$

When this is achieved,

$$\theta - \varphi \rightarrow 0,$$

and therefore

$$\varphi = \theta$$

to within one count. Hence, the counter's digital output, φ, represents the angle θ. The latches enable this data to be transferred externally without interrupting the loop's tracking.

RESOLVER-TO-DIGITAL CONVERTER (RTD)

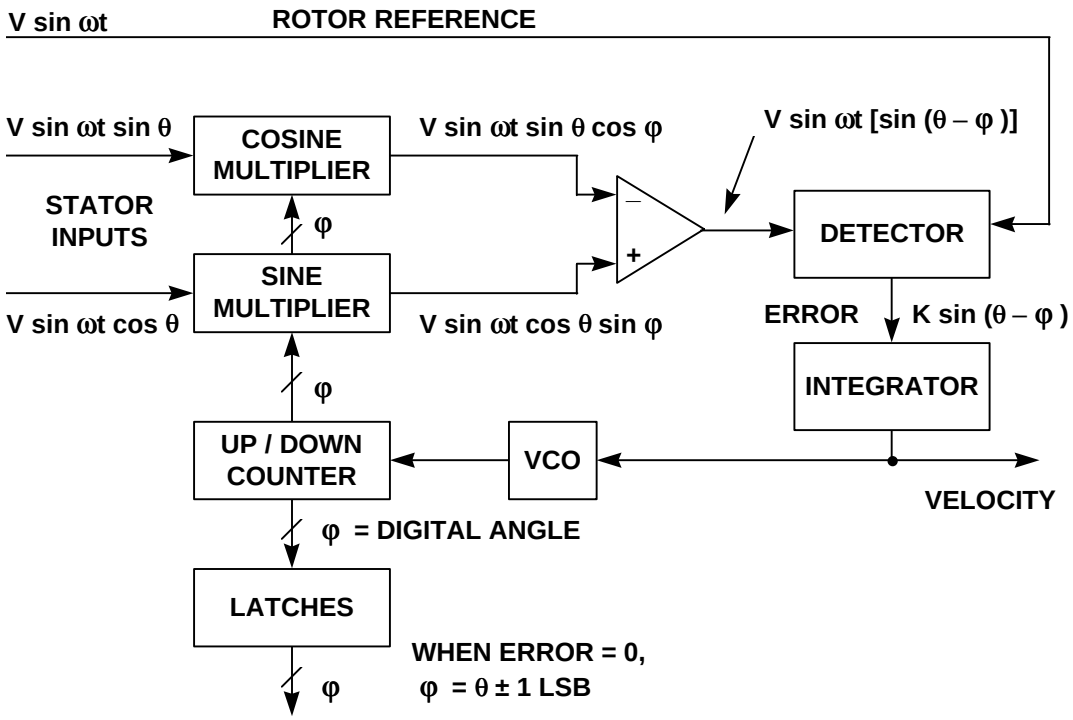


Figure 6.14

This circuit is equivalent to a so-called type-2 servo loop, because it has, in effect, two integrators. One is the counter, which accumulates pulses; the other is the integrator at the output of the detector. In a type-2 servo loop with a constant rotational velocity input, the output digital word continuously follows, or tracks the input, without needing externally derived convert commands, and with no steady state phase lag between the digital output word and actual shaft angle. An error signal appears only during periods of acceleration or deceleration.

As an added bonus, the tracking RDC provides an analog DC output voltage directly proportional to the shaft's rotational velocity. This is a useful feature if velocity is to be measured or used as a stabilization term in a servo system, and it makes tachometers unnecessary.

Since the operation of an RDC depends only on the ratio between input signal amplitudes, attenuation in the lines connecting them to resolvers doesn't substantially affect performance. For similar reasons, these converters are not greatly susceptible to waveform distortion. In fact, they can operate with as much as 10% harmonic distortion on the input signals; some applications actually use square-wave references with little additional error.

Tracking ADCs are therefore ideally suited to RDCs. While other ADC architectures, such as successive approximation, could be used, the tracking converter is the most accurate and efficient for this application.

Because the tracking converter doubly integrates its error signal, the device offers a high degree of noise immunity (12 dB-per-octave rolloff). The net area under any given noise spike produces an error. However, typical inductively coupled noise spikes have equal positive and negative going waveforms. When integrated, this results in a zero net error signal. The resulting noise immunity, combined with the converter's insensitivity to voltage drops, lets the user locate the converter at a considerable distance from the resolver. Noise rejection is further enhanced by the detector's rejection of any signal not at the reference frequency, such as wideband noise.

The AD2S90 is one of a number of integrated RDCs offered by Analog Devices. Key specifications are shown in Figure 6.15. The general architecture is similar to that of Figure 6.14. The input signal level should be 2V RMS ± 10% in the frequency range from 3kHz to 20kHz.

PERFORMANCE CHARACTERISTICS FOR AD2S90 RESOLVER-TO-DIGITAL CONVERTER

- **12-Bit Resolution (1 LSB = 0.08° = 5.3 arc min)**
- **Inputs: 2V RMS ± 10%, 3kHz to 20kHz**
- **Angular Accuracy: 10.6 arc min ± 1 LSB**
- **Maximum Tracking Rate: 375 revolutions per second**
- **Maximum VCO Clock Rate: 1.536MHz**
- **Settling Time:**
  - **1° Step: 7ms**
  - **179° Step: 20ms**
- **Differential Inputs**
- **Serial Output Interface**
- **± 5V Supplies, 50mW Power Dissipation**
- **20 Pin PLCC**

Figure 6.15

INDUCTOSYNS

Synchros and resolvers inherently measure rotary position, but they can make linear position measurements when used with lead screws. An alternative, the Inductosyn™ (registered trademark of Farrand Controls, Inc.) measures linear position directly. In addition, Inductosyns are accurate and rugged, well-suited to severe industrial environments, and do not require ohmic contact.

The linear Inductosyn consists of two magnetically coupled parts; it resembles a multipole resolver in its operation (see Figure 6.16). One part, the scale, is fixed (e.g. with epoxy) to one axis, such as a machine tool bed. The other part, the slider, moves along the scale in conjunction with the device to be positioned (for example, the machine tool carrier).

The scale is constructed of a base material such as steel, stainless steel, aluminum, or a tape of spring steel, covered by an insulating layer. Bonded to this is a printed-circuit trace, in the form of a continuous rectangular waveform pattern. The pattern typically has a cyclic pitch of 0.1 inch, 0.2 inch, or 2 millimeters. The slider, about 4 inches long, has two separate but identical printed circuit traces bonded to the surface that faces the scale. These two traces have a waveform pattern with exactly the same cyclic pitch as the waveform on the scale, but one trace is shifted one-quarter of a cycle relative to the other. The slider and the scale remain separated by a small air gap of about 0.007 inch.

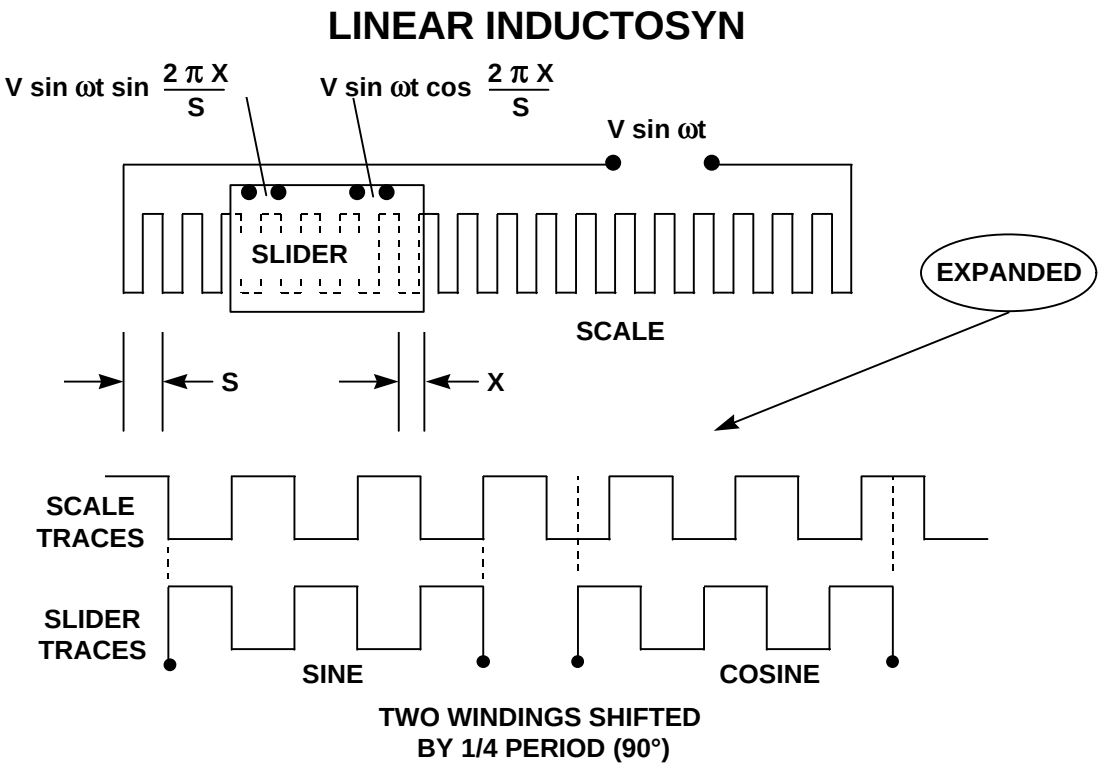


Figure 6.16

Inductosyn operation resembles that of a resolver. When the scale is energized with a sine wave, this voltage couples to the two slider windings, inducing voltages proportional to the sine and cosine of the slider's spacing within the cyclic pitch of the scale. If S is the distance between pitches, and X is the slider displacement within a pitch, and the scale is energized with a voltage V sinωt, then the slider windings will see terminal voltages of:

$$V \text{ (sine output)} = V \sin\omega t \sin[2\pi X/S]$$

$$V \text{ (cosine output)} = V \sin\omega t \cos[2\pi X/S].$$

As the slider moves the distance of the scale pitch, the voltages produced by the two slider windings are similar to those produced by a resolver rotating through 360º. The absolute orientation of the Inductosyn is determined by counting successive pitches in either direction from an established starting point. Because the Inductosyn consists of a large number of cycles, some form of coarse control is necessary in order to avoid ambiguity. The usual method of providing this is to use a resolver or synchro operated through a rack and pinion or a lead screw.

In contrast to a resolver's highly efficient transformation of 1:1 or 2:1, typical Inductosyns operate with transformation ratios of 100:1. This results in a pair of sinusoidal output signals in the millivolt range which generally require amplification.

Since the slider output signals are derived from an average of several spatial cycles, small errors in conductor spacing have minimal effects. This is an important reason for the Inductosyn's very high accuracy. In combination with 12-bit RDCs, linear Inductosyns readily achieve 25 microinch resolutions.

Rotary inductosyns can be created by printing the scale on a circular rotor and the slider's track pattern on a circular stator. Such rotary devices can achieve very high resolutions. For instance, a typical rotary Inductosyn may have 360 cyclic pitches per rotation, and might use a 12-bit RDC. The converter effectively divides each pitch into 4096 sectors. Multiplying by 360 pitches, the rotary Inductosyn divides the circle into a total of 1,474,560 sectors. This corresponds to an angular resolution of less than 0.9 arc seconds. As in the case of the linear Inductosyn, a means must be provided for counting the individual pitches as the shaft rotates. This may be done with an additional resolver acting as the coarse measurement.

VECTOR AC INDUCTION MOTOR CONTROL

Long known for its simplicity of construction, low-cost, high efficiency and long-term dependability, the AC induction motor has been limited by the inability to control its dynamic performance in all but the crudest fashion. This has severely restricted the application of AC induction motors where dynamic control of speed, torque and response to changing load is required. However, recent advances in digital signal processing (DSP) and mixed-signal integrated circuit technology are providing the AC induction motor with performance never before thought possible. Manufacturers anxious to harness the power and economy of Vector Control can reduce R&D costs and time to market for applications ranging from industrial drives to electric automobiles and locomotives with a standard chipset/development system.

It is unlikely that Nikola Tesla (1856-1943), the inventor of the induction motor, could have envisaged that this workhorse of industry could be rejuvenated into a new class of motor that is competitive in most industrial applications.

Before discussing the advantages of Vector Control it is necessary to have a basic understanding of the fundamental operation of the different types of electric motors in common use.

Until recently, motor applications requiring servo-control tasks such as tuned response to dynamic loads, constant torque and speed control over a wide range were almost exclusively the domain of DC brush and DC permanent magnet synchronous motors. The fundamental reason for this preference was the availability of well understood and proven control schemes. Although easily

controlled, DC brush motors suffer from several disadvantages; brushes wear and must be replaced at regular intervals, commutators wear and can be permanently damaged by inadequate brush maintenance, brush/commutator assemblies are a source of particulate contaminants, and the arcing of mechanical commutation can be a serious fire hazard is some environments.

The availability of power inverters capable of controlling high-horsepower motors allowed practical implementation of alternate motor architectures such as the DC permanent magnet synchronous motor (PMSM) in servo control applications. Although eliminating many of the mechanical problems associated with DC brush motors, these motors required more complex control schemes and suffered from several drawbacks of their own. Aside from being costly, DC PMSMs in larger, high-horsepower configurations suffer from high rotor moment-of-inertia as well as limited use in high speed applications due to mechanical constraints of rotor construction and the need to implement field weakening to exceed baseplate speed.

In the 1960's, advances in control theory, in particular the development of *indirect field-oriented control*, provided the theoretical basis for dynamic control of AC induction motors. Because of the intensive mathematical computations required by indirect field-oriented control, now commonly referred to as *vector control*, practical implementation was not possible for many years. Available hardware could not perform the high-speed precision sensing of rotor position and near real-time computation of dynamic flux vectors. The current availability of precision optical encoders, isolated gate bipolar transistors (IGBTs), high-speed resolver-to-digital converters and high-speed digital signal processors (DSPs) has pushed vector control to the forefront of motor development due to the advantages inherent in the AC induction motor.

A simplified block diagram of an AC induction motor control system is shown in Figure 6.17. In this example, a single-chip IC (ADMC300, ADMC330, or ADMC331) performs the control functions. The inputs to the controller chip are the motor currents (normally three-phase) and the motor rotor position and velocity. Hall-effect sensors are often used to monitor the currents, and a resolver and an RDC monitor the rotor position and velocity. The DSP is used to perform the real time vector-type calculations necessary to generate the control outputs to the inverter processors. The transformations required for vector control are also accomplished with the DSP.

The ADMC300 comprises a high performance, 5 channel 16-bit ADC system, a 12-bit 3-phase PWM generation unit, and a flexible encoder interface for position sensor feedback. The ADMC330 includes a 7 channel 12-bit ADC system and a 12-bit 3-phase PWM generator. The ADMC331 includes a 7 channel 12-bit ADC system, and a programmable 16-bit 3-phase PWM generator. It also has additional power factor correction control capabilities. All devices have on-chip DSPs (approximately 20MHz) based on Analog Device's Modified Harvard Architechure 16-bit DSP core. Third-party DSP software and reference designs are available to facilitate motor control system development using these chips.

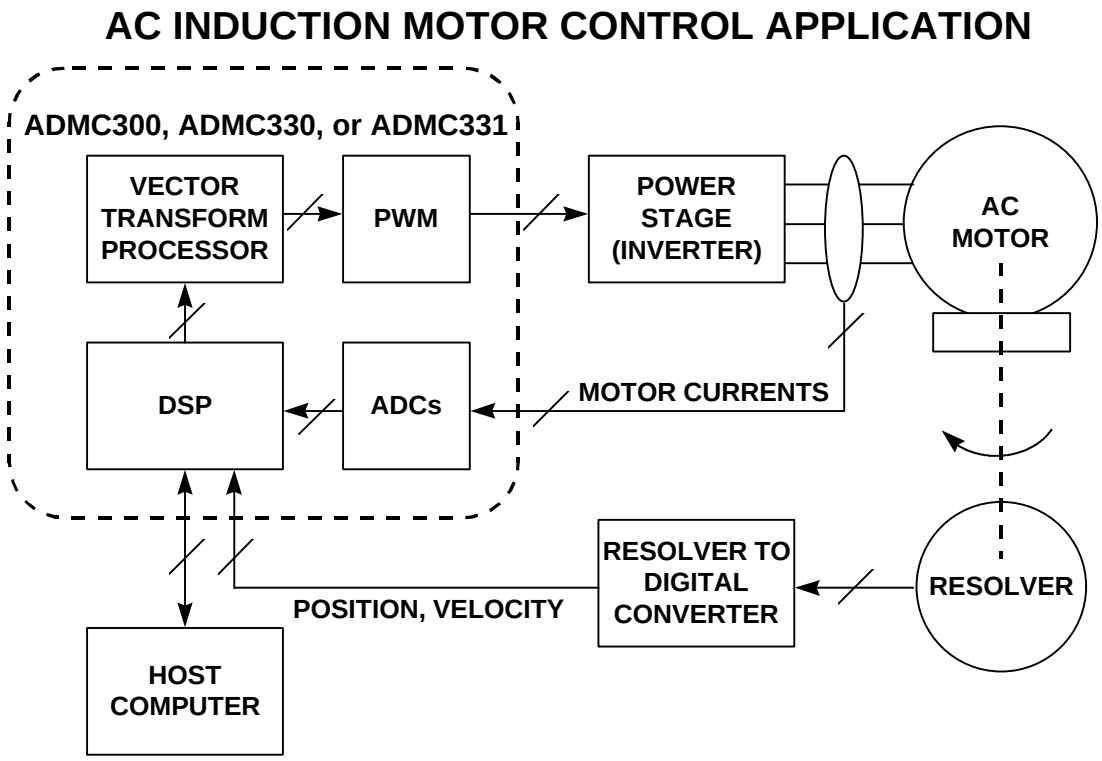


Figure 6.17

ACCELEROMETERS

Accelerometers are widely used to measure tilt, inertial forces, shock, and vibration. They find wide usage in automotive, medical, industrial control, and other applications. Modern micromachining techniques allow these accelerometers to be manufactured on CMOS processes at low cost with high reliability. Analog Devices iMEMS® (Integrated Micro Electro Mechanical Systems) accelerometers represent a breakthrough in this technology. A significant advantage of this type of accelerometer over piezoelectric-type charge-output accelerometers is that DC acceleration can be measured (e.g. they can be used in tilt measurements where the acceleration is a constant 1g).

The basic unit cell sensor building block for these accelerometers is shown in Figure 6.19. The surface micromachined sensor element is made by depositing polysilicon on a sacrificial oxide layer that is then etched away leaving the suspended sensor element. The actual sensor has tens of unit cells for sensing acceleration, but the diagram shows only one cell for clarity. The electrical basis of the sensor is the differential capacitor (CS1 and CS2) which is formed by a center plate which is part of the moving beam and two fixed outer plates. The two capacitors are equal at rest (no applied acceleration). When acceleration is applied, the mass of the beam causes it to move closer to one of the fixed plates while moving further from the other. This change in differential capacitance forms the electrical basis for the conditioning electronics shown in Figure 6.20.

ACCELEROMETER APPLICATIONS

- Tilt or Inclination
  - Car Alarms
  - Patient Monitors
- Inertial Forces
  - Laptop Computer Disc Drive Protection
  - Airbag Crash Sensors
  - Car Navigation systems
  - Elevator Controls
- Shock or Vibration
  - Machine Monitoring
  - Control of Shaker Tables
- ADI Accelerometer Fullscale g-Range: ± 2g to ± 100g
- ADI Accelerometer Frequency Range: DC to 1kHz

Figure 6.18

ADXL-FAMILY MICROMACHINED ACCELEROMETERS (TOP VIEW OF IC)

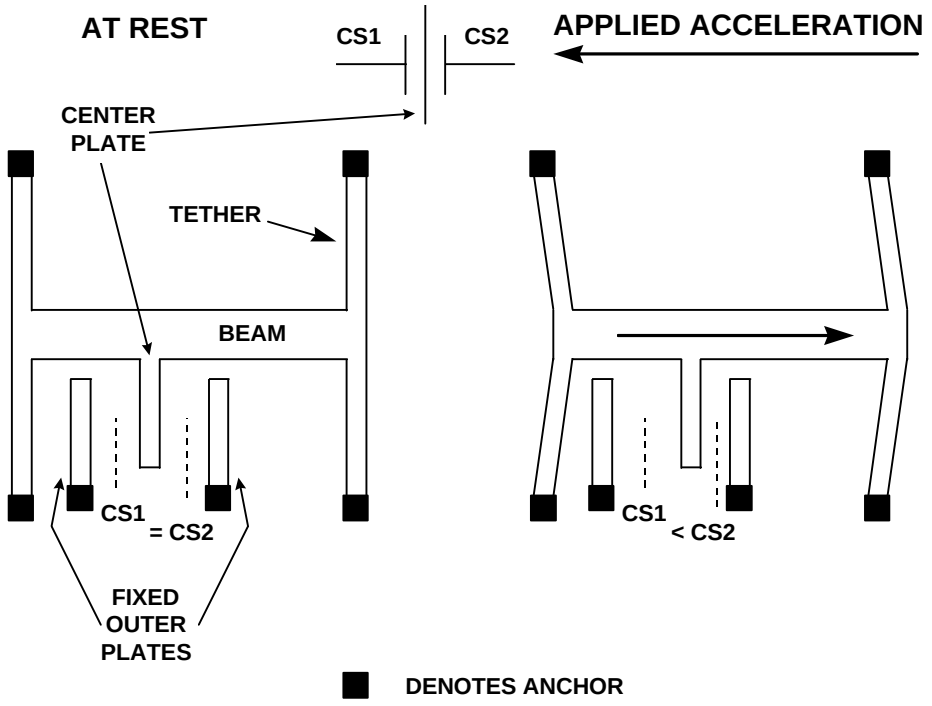


Figure 6.19

ADXL-FAMILY ACCELEROMETERS
INTERNAL SIGNAL CONDITIONING

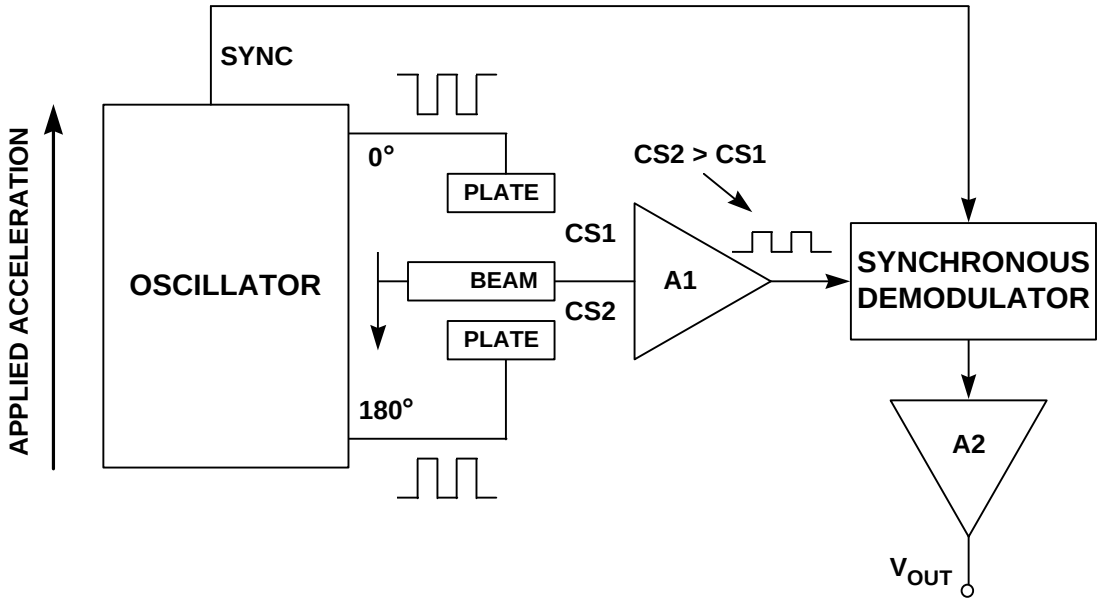


Figure 6.20

The sensor's fixed capacitor plates are driven differentially by a 1MHz square wave: the two square wave amplitudes are equal but are 180º out of phase. When at rest, the values of the two capacitors are the same, and therefore the voltage output at their electrical center (i.e., at the center plate attached to the movable beam) is zero. When the beam begins to move, a mismatch in the capacitance produces an output signal at the center plate. The output amplitude will increase with the acceleration experienced by the sensor. The center plate is buffered by A1 and applied to a synchronous demodulator. The direction of beam motion affects the phase of the signal, and synchronous demodulation is therefore used to extract the amplitude information. The synchronous demodulator output is amplified by A2 which supplies the acceleration output voltage, V_{OUT}.

An interesting application of low-g accelerometers is measuring tilt. Figure 6.21 shows the response of an accelerometer to tilt. The accelerometer output on the diagram has been normalized to 1g fullscale. The accelerometer output is proportional to the sine of the tilt angle with respect to the horizon. Note that maximum sensitivity occurs when the accelerometer axis is perpendicular to the acceleration. This scheme allows tilt angles from –90º to +90º (180º of rotation) to be measured. However, in order to measure a full 360º rotation, a dual-axis accelerometer must be used.

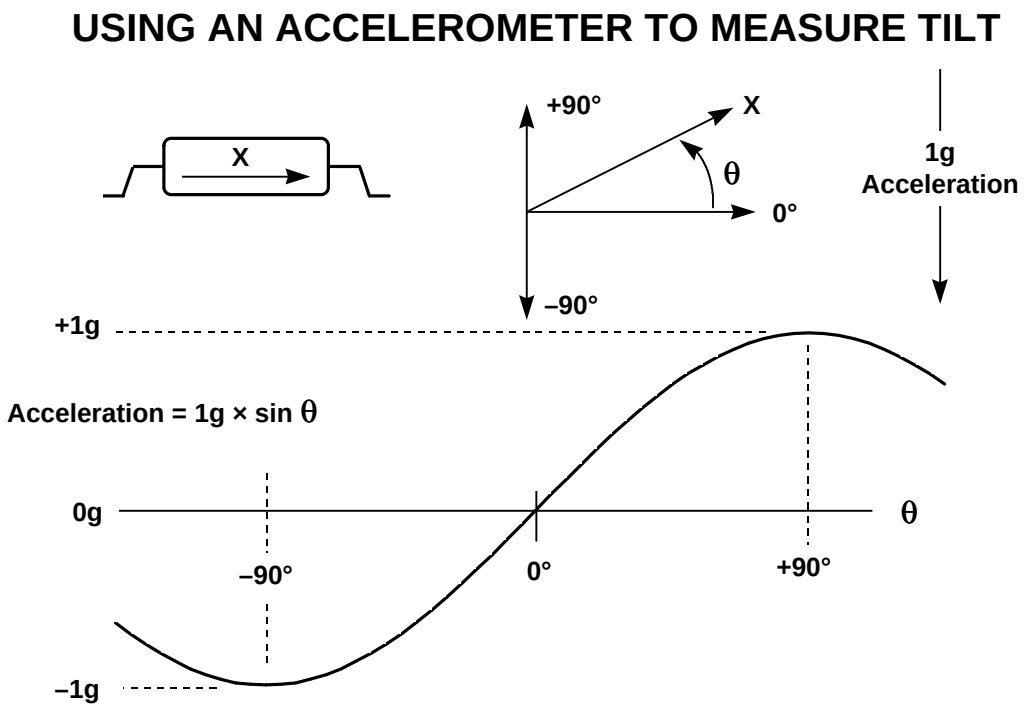


Figure 6.21

Figure 6.22 shows a simplified block diagram of the ADXL202 dual axis ±2g accelerometer. The output is a pulse whose duty cycle contains the acceleration information. This type of output is extremely useful because of its high noise immunity, and the data is transmitted over a single wire. Standard low cost microcontrollers have timers which can be easily used to measure the T1 and T2 intervals. The acceleration in g is then calculated using the formula:

$$A(g) = 8\,[T1/T2 - 0.5]\,.$$

Note that a duty cycle of 50% (T1 = T2) yields a 0g output. T2 does not have to be measured for every measurement cycle. It need only be updated to account for changes due to temperature. Since the T2 time period is shared by both X and Y channels, it is necessary to only measure it on one channel. The T2 period can be set from 0.5ms to 10ms with an external resistor.

Analog voltages representing acceleration can be obtained by buffering the signal from the X_{FILT} and Y_{FILT} outputs or by passing the duty cycle signal through an RC filter to reconstruct its DC value.

A single accelerometer cannot work in all applications. Specifically, there is a need for both low-g and high-g accelerometers. Low-g devices are useful in such applications as tilt measurements, but higher-g accelerometers are needed in applications such as airbag crash sensors. Figure 6.23 summarizes Analog Devices family of ADXL accelerometers to date. Note that dual-axis versions as well as duty-cycle output versions are also available for some of the devices.

ADXL202 ±2g DUAL AXIS ACCELEROMETER

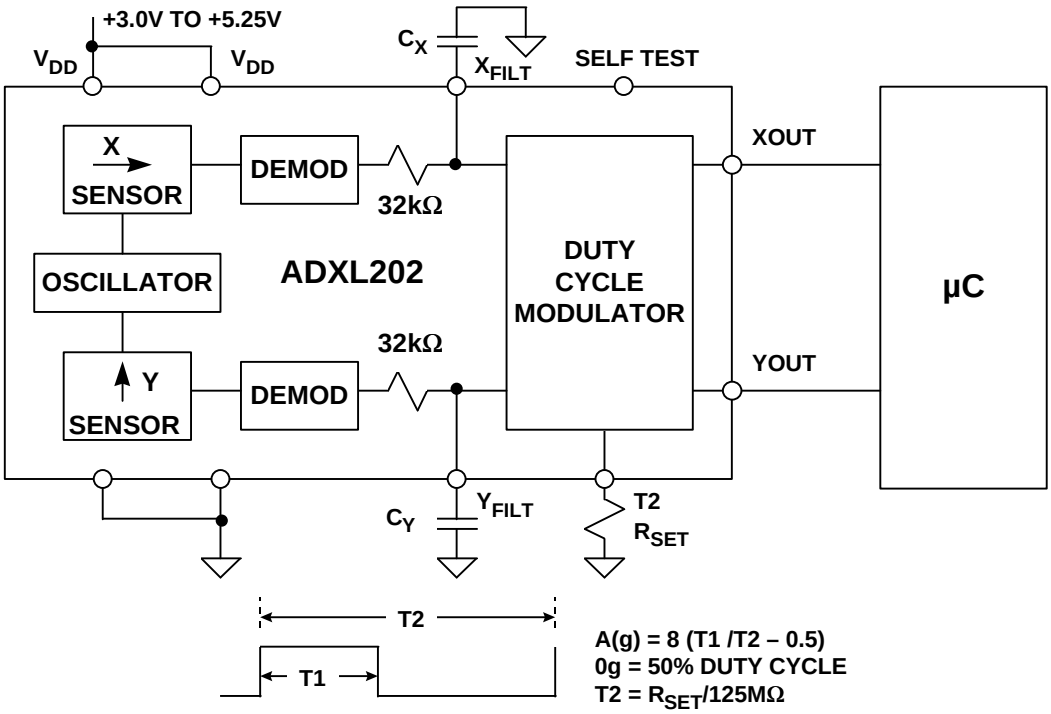


Figure 6.22

ADXL FAMILY OF ACCELEROMETERS

	g RANGE	NOISE DENSITY	SINGLE/ DUAL AXIS	VOLTAGE/ DUTY CYCLE OUTPUT
ADXL202	±2g	0.5mg/√Hz	Dual	Duty Cycle
ADXL05	±5g	0.5mg/√Hz	Single	Voltage
ADXL105	±5g	0.175mg/√Hz	Single	Voltage
ADXL210	±10g	0.5mg/√Hz	Dual	Duty Cycle
ADXL150	±50g	1mg/√Hz	Single	Voltage
ADXL250	±50g	1mg/√Hz	Dual	Voltage
ADXL190	±100g	4mg/√Hz	Single	Voltage

Figure 6.23

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SECTION 7
TEMPERATURE SENSORS

Walt Kester, James Bryant, Walt Jung

INTRODUCTION

Measurement of temperature is critical in modern electronic devices, especially expensive laptop computers and other portable devices with densely packed circuits which dissipate considerable power in the form of heat. Knowledge of system temperature can also be used to control battery charging as well as prevent damage to expensive microprocessors.

Compact high power portable equipment often has fan cooling to maintain junction temperatures at proper levels. In order to conserve battery life, the fan should only operate when necessary. Accurate control of the fan requires a knowledge of critical temperatures from the appropriate temperature sensor.

APPLICATIONS OF TEMPERATURE SENSORS

- **Monitoring**
  - **Portable Equipment**
  - **CPU Temperature**
  - **Battery Temperature**
  - **Ambient Temperature**
- **Compensation**
  - **Oscillator Drift in Cellular Phones**
  - **Thermocouple Cold-Junction Compensation**
- **Control**
  - **Battery Charging**
  - **Process Control**

Figure 7.1

Accurate temperature measurements are required in many other measurement systems such as process control and instrumentation applications. In most cases, because of low-level nonlinear outputs, the sensor output must be properly conditioned and amplified before further processing can occur.

Except for IC sensors, all temperature sensors have nonlinear transfer functions. In the past, complex analog conditioning circuits were designed to correct for the sensor nonlinearity. These circuits often required manual calibration and precision resistors to achieve the desired accuracy. Today, however, sensor outputs may be

digitized directly by high resolution ADCs. Linearization and calibration is then performed digitally, thereby reducing cost and complexity.

Resistance Temperature Devices (RTDs) are accurate, but require excitation current and are generally used in bridge circuits. Thermistors have the most sensitivity but are the most non-linear. However, they are popular in portable applications such as measurement of battery temperature and other critical temperatures in a system.

Modern semiconductor temperature sensors offer high accuracy and high linearity over an operating range of about –55ºC to +150ºC. Internal amplifiers can scale the output to convenient values, such as 10mV/ºC. They are also useful in cold-junction-compensation circuits for wide temperature range thermocouples. Semiconductor temperature sensors can be integrated into multi-function ICs which perform a number of other hardware monitoring functions.

Figure 7.2 lists the most popular types of temperature transducers and their characteristics.

TYPES OF TEMPERATURE SENSORS

THERMOCOUPLE	RTD	THERMISTOR	SEMICONDUCTOR
Widest Range: –184ºC to +2300ºC	Range: –200ºC to +850ºC	Range: 0ºC to +100ºC	Range: –55ºC to +150ºC
High Accuracy and Repeatability	Fair Linearity	Poor Linearity	Linearity: 1ºC Accuracy: 1ºC
Needs Cold Junction Compensation	Requires Excitation	Requires Excitation	Requires Excitation
Low-Voltage Output	Low Cost	High Sensitivity	10mV/K, 20mV/K, or 1µA/K Typical Output

Figure 7.2

THERMOCOUPLE PRINCIPLES AND COLD-JUNCTION COMPENSATION

Thermocouples are small, rugged, relatively inexpensive, and operate over the widest range of all temperature sensors. They are especially useful for making measurements at extremely high temperatures (up to +2300°C) in hostile environments. They produce only millivolts of output, however, and require precision amplification for further processing. They also require cold-junction-compensation (CJC) techniques which will be discussed shortly. They are more linear than many other sensors, and their non-linearity has been well characterized. Some common thermocouples are shown in Figure 7.3. The most common metals used are Iron, Platinum, Rhodium, Rhenium, Tungsten, Copper, Alumel (composed

of Nickel and Aluminum), Chromel (composed of Nickel and Chromium) and Constantan (composed of Copper and Nickel).

COMMON THERMOCOUPLES

JUNCTION MATERIALS	TYPICAL USEFUL RANGE (ºC)	NOMINAL SENSITIVITY (µV/ºC)	ANSI DESIGNATION
Platinum (6%)/ Rhodium-Platinum (30%)/Rhodium	38 to 1800	7.7	B
Tungsten (5%)/Rhenium - Tungsten (26%)/Rhenium	0 to 2300	16	C
Chromel - Constantan	0 to 982	76	E
Iron - Constantan	0 to 760	55	J
Chromel - Alumel	–184 to 1260	39	K
Platinum (13%)/Rhodium-Platinum	0 to 1593	11.7	R
Platinum (10%)/Rhodium-Platinum	0 to 1538	10.4	S
Copper-Constantan	–184 to 400	45	T

Figure 7.3

Figure 7.4 shows the voltage-temperature curves of three commonly used thermocouples, referred to a 0°C fixed-temperature reference junction. Of the thermocouples shown, Type J thermocouples are the most sensitive, producing the largest output voltage for a given temperature change. On the other hand, Type S thermocouples are the least sensitive. These characteristics are very important to consider when designing signal conditioning circuitry in that the thermocouples' relatively low output signals require low-noise, low-drift, high-gain amplifiers.

To understand thermocouple behavior, it is necessary to consider the non-linearities in their response to temperature differences. Figure 7.4 shows the relationships between sensing junction temperature and voltage output for a number of thermocouple types (in all cases, the reference *cold* junction is maintained at 0°C). It is evident that the responses are not quite linear, but the nature of the non-linearity is not so obvious.

Figure 7.5 shows how the Seebeck coefficient (the *change* of output voltage with *change* of sensor junction temperature - i.e., the first derivative of output with respect to temperature) varies with sensor junction temperature (we are still considering the case where the reference junction is maintained at 0°C).

When selecting a thermocouple for making measurements over a particular range of temperature, we should choose a thermocouple whose Seebeck coefficient varies as little as possible over that range.

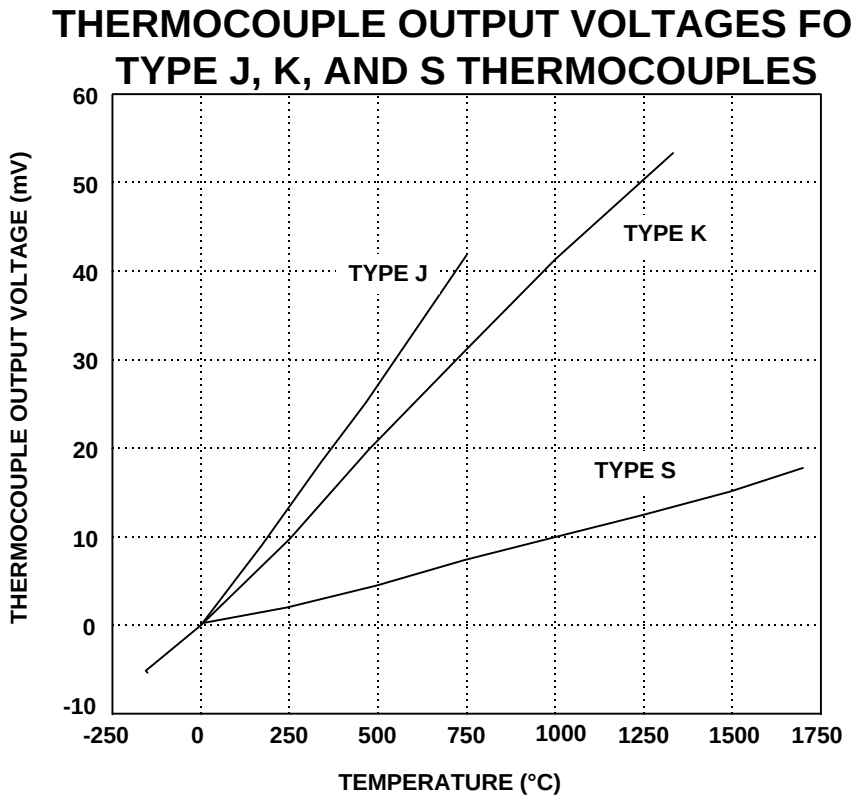


Figure 7.4

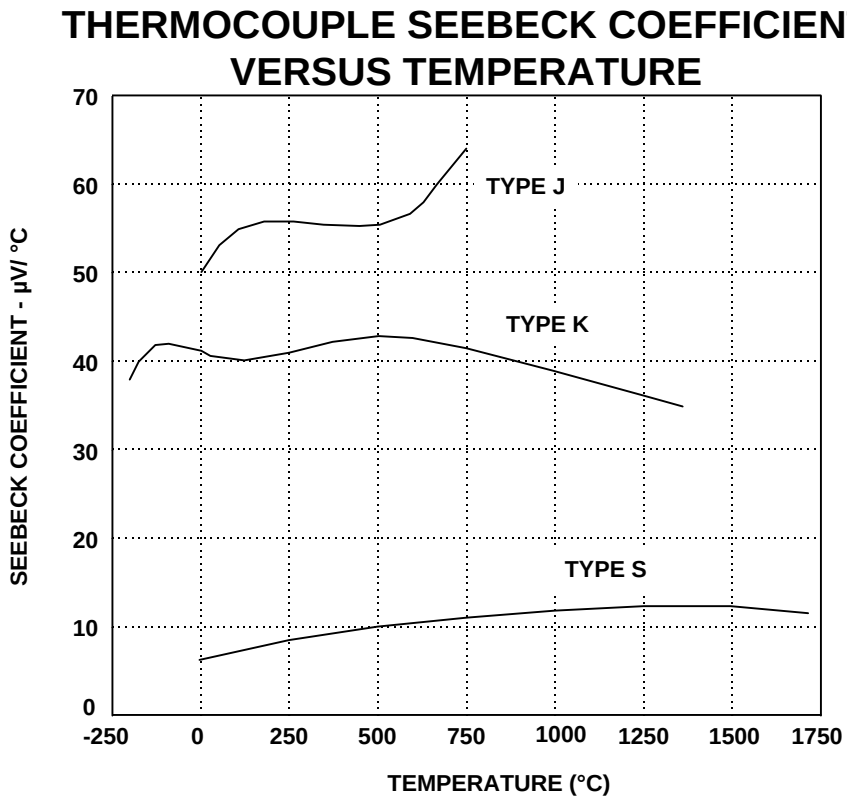


Figure 7.5

For example, a Type J thermocouple has a Seebeck coefficient which varies by less than 1µV/°C between 200 and 500°C, which makes it ideal for measurements in this range.

Presenting these data on thermocouples serves two purposes: First, Figure 7.4 illustrates the range and sensitivity of the three thermocouple types so that the system designer can, at a glance, determine that a Type S thermocouple has the widest useful temperature range, but a Type J thermocouple is more sensitive. Second, the Seebeck coefficients provide a quick guide to a thermocouple's linearity. Using Figure 7.5, the system designer can choose a Type K thermocouple for its linear Seebeck coefficient over the range of 400°C to 800°C or a Type S over the range of 900°C to 1700°C. The behavior of a thermocouple's Seebeck coefficient is important in applications where variations of temperature rather than absolute magnitude are important. These data also indicate what performance is required of the associated signal conditioning circuitry.

To use thermocouples successfully we must understand their basic principles. Consider the diagrams in Figure 7.6.

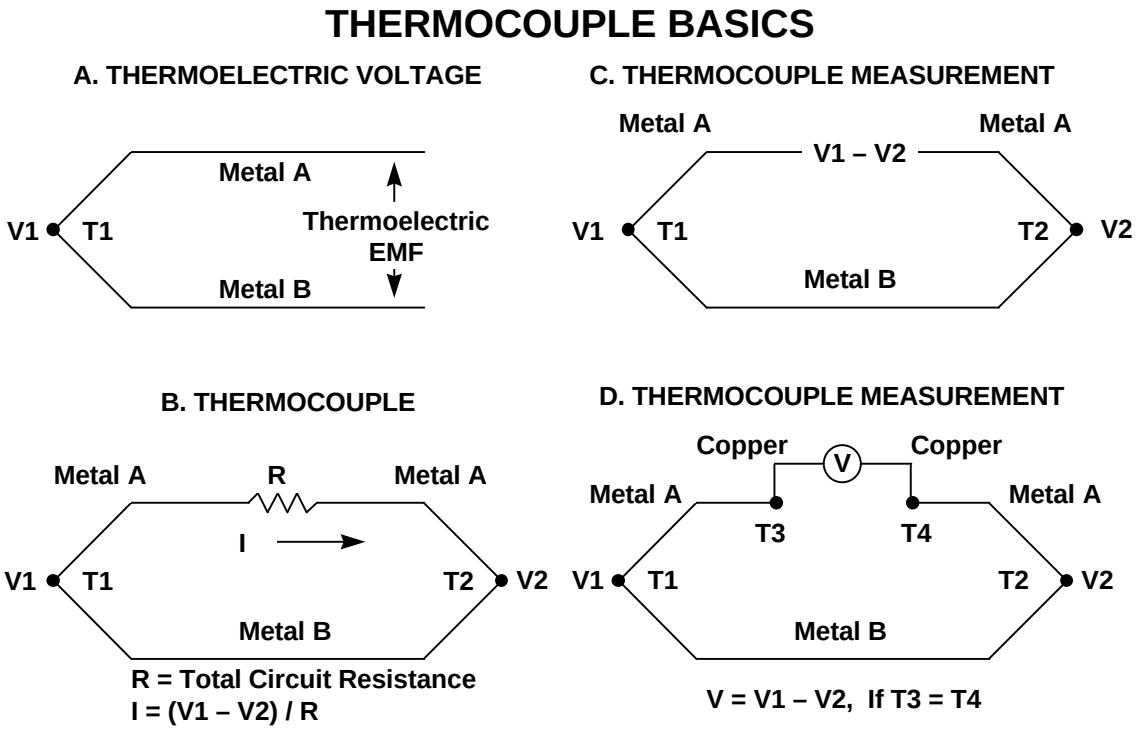


Figure 7.6

If we join two dissimilar metals at any temperature above absolute zero, there will be a potential difference between them (their "thermoelectric e.m.f." or "contact potential") which is a function of the temperature of the junction (Figure 7.6A). If we join the two wires at two places, two junctions are formed (Figure 7.6B). If the two junctions are at different temperatures, there will be a net e.m.f. in the circuit, and a current will flow determined by the e.m.f. and the total resistance in the circuit (Figure 7.6B). If we break one of the wires, the voltage across the break will be

equal to the net thermoelectric e.m.f. of the circuit, and if we measure this voltage, we can use it to calculate the temperature difference between the two junctions (Figure 7.6C). *We must always remember that a thermocouple measures the temperature difference between two junctions, not the absolute temperature at one junction*. We can only measure the temperature at the measuring junction if we know the temperature of the other junction (often called the "reference" junction or the "cold" junction).

But it is not so easy to measure the voltage generated by a thermocouple. Suppose that we attach a voltmeter to the circuit in Figure 7.6C (Figure 7.6D). The wires attached to the voltmeter will form further thermojunctions where they are attached. If both these additional junctions are at the same temperature (it does not matter what temperature), then the "Law of Intermediate Metals" states that they will make no net contribution to the total e.m.f. of the system. If they are at different temperatures, they will introduce errors. Since *every pair of dissimilar metals in contact generates a thermoelectric e.m.f.* (including copper/solder, kovar/copper [kovar is the alloy used for IC leadframes] and aluminum/kovar [at the bond inside the IC]), it is obvious that in practical circuits the problem is even more complex, and it is necessary to take extreme care to ensure that all the junction pairs in the circuitry around a thermocouple, except the measurement and reference junctions themselves, are at the same temperature.

Thermocouples generate a voltage, albeit a very small one, and do not require excitation. As shown in Figure 7.6D, however, two junctions (T1, the measurement junction and T2, the reference junction) are involved. If T2 = T1, then V2 = V1, and the output voltage V = 0. Thermocouple output voltages are often defined with a reference junction temperature of 0ºC (hence the term *cold* or *ice point* junction), so the thermocouple provides an output voltage of 0V at 0ºC. To maintain system accuracy, the reference junction must therefore be at a well-defined temperature (but not necessarily 0ºC). A conceptually simple approach to this need is shown in Figure 7.7. Although an ice/water bath is relatively easy to define, it is quite inconvenient to maintain.

Today an ice-point reference, and its inconvenient ice/water bath, is generally replaced by electronics. A temperature sensor of another sort (often a semiconductor sensor, sometimes a thermistor) measures the temperature of the cold junction and is used to inject a voltage into the thermocouple circuit which compensates for the difference between the actual cold junction temperature and its ideal value (usually 0°C) as shown in Figure 7.8. Ideally, the compensation voltage should be an exact match for the difference voltage required, which is why the diagram gives the voltage as f(T2) (a *function* of T2) rather than KT2, where K is a simple constant. In practice, since the cold junction is rarely more than a few tens of degrees from 0°C, and generally varies by little more than ±10°C, a linear approximation (V=KT2) to the more complex reality is sufficiently accurate and is what is often used. (The expression for the output voltage of a thermocouple with its measuring junction at T°C and its reference at 0°C is a polynomial of the form $V = K_1T + K_2T^2 + K_3T^3 + ...$, but the values of the coefficients K_2, K_3, etc. are very small for most common types of thermocouple. References 8 and 9 give the values of these coefficients for a wide range of thermocouples.)

CLASSICAL COLD-JUNCTION COMPENSATION USING AN ICE-POINT (0°C) REFERENCE JUNCTION

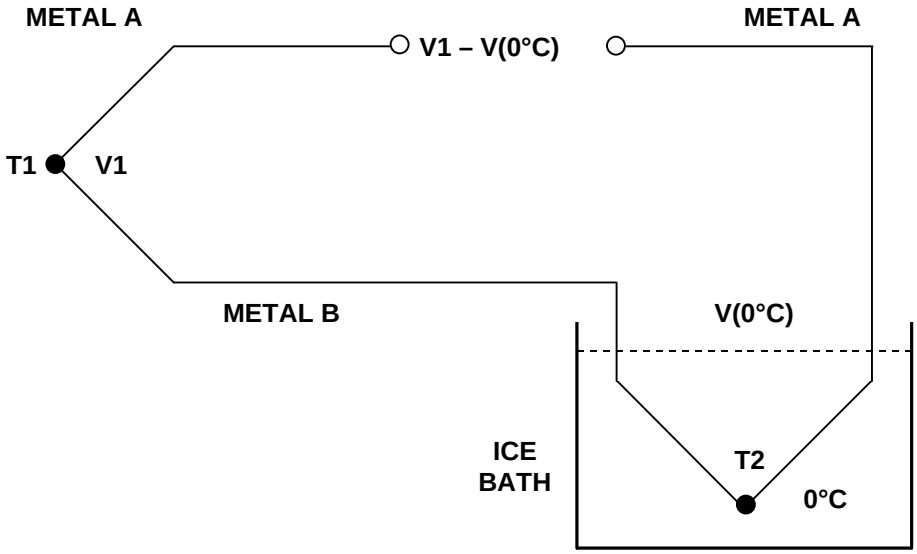
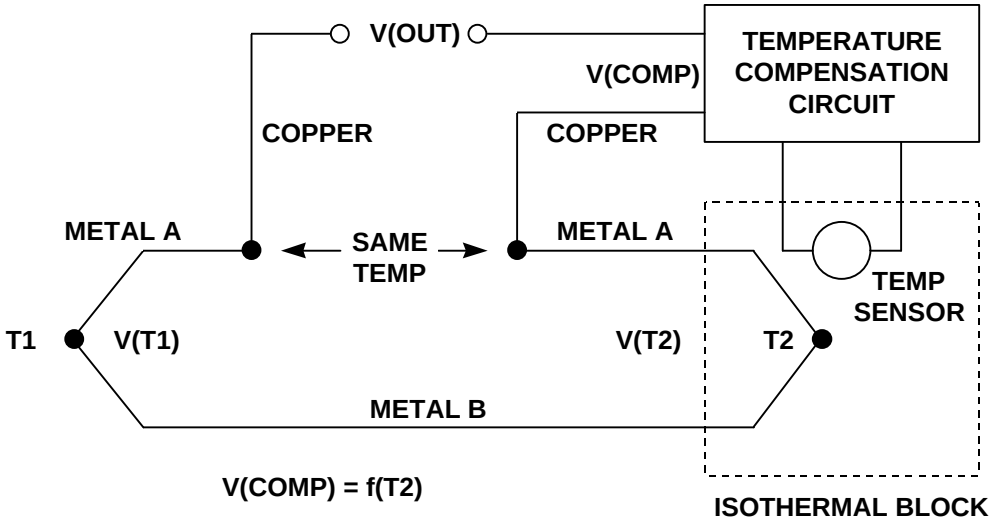


Figure 7.7

USING A TEMPERATURE SENSOR FOR COLD-JUNCTION COMPENSATION



V(COMP) = f(T2)

V(OUT) = V(T1) – V(T2) + V(COMP)

IF V(COMP) = V(T2) – V(0°C), THEN

V(OUT) = V(T1) – V(0°C)

Figure 7.8

When electronic cold-junction compensation is used, it is common practice to eliminate the additional thermocouple wire and terminate the thermocouple leads in the isothermal block in the arrangement shown in Figure 7.9. The Metal A-Copper and the Metal B-Copper junctions, if at the same temperature, are equivalent to the Metal A-Metal B thermocouple junction in Figure 7.8.

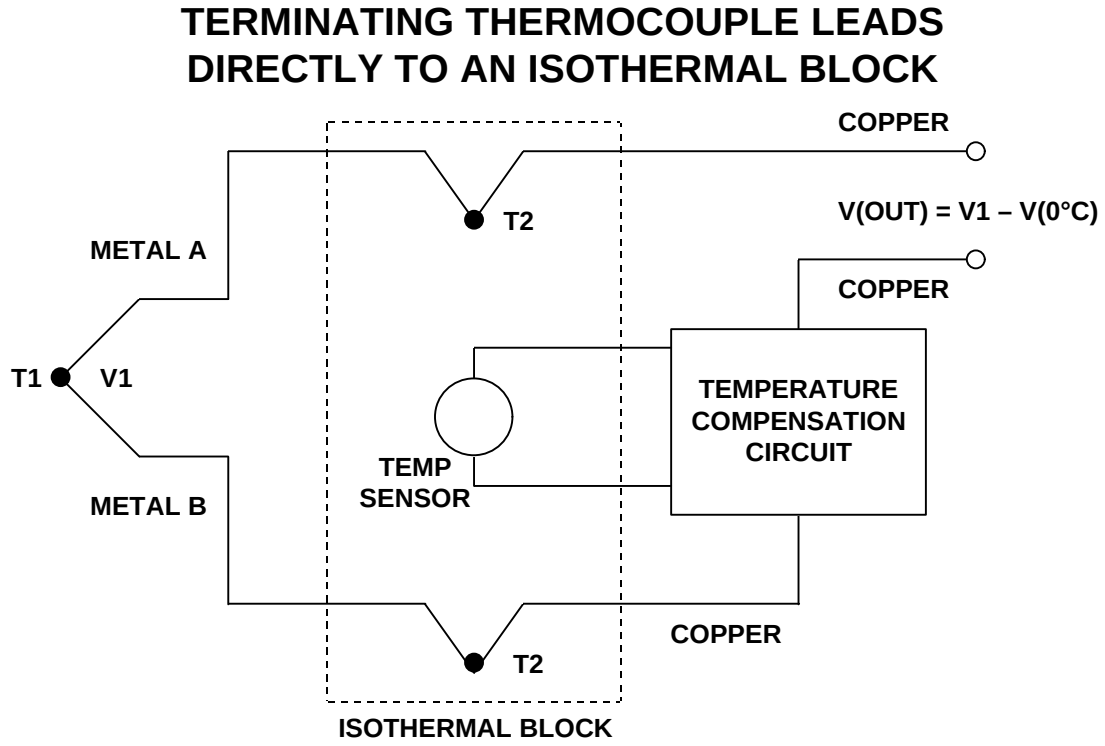


Figure 7.9

The circuit in Figure 7.10 conditions the output of a Type K thermocouple, while providing cold-junction compensation, for temperatures between 0ºC and 250ºC. The circuit operates from single +3.3V to +12V supplies and has been designed to produce an output voltage transfer characteristic of 10mV/ºC.

A Type K thermocouple exhibits a Seebeck coefficient of approximately 41µV/ºC; therefore, at the cold junction, the TMP35 voltage output sensor with a temperature coefficient of 10mV/ºC is used with R1 and R2 to introduce an opposing cold-junction temperature coefficient of –41µV/ºC. This prevents the isothermal, cold-junction connection between the circuit's printed circuit board traces and the thermocouple's wires from introducing an error in the measured temperature. This compensation works extremely well for circuit ambient temperatures in the range of 20ºC to 50ºC. Over a 250ºC measurement temperature range, the thermocouple produces an output voltage change of 10.151mV. Since the required circuit's output full-scale voltage change is 2.5V, the gain of the circuit is set to 246.3. Choosing R4 equal to 4.99kΩ sets R5 equal to 1.22MΩ. Since the closest 1% value for R5 is 1.21MΩ, a 50kΩ potentiometer is used with R5 for fine trim of the full-scale output voltage. Although the OP193 is a single-supply op amp, its output stage is not rail-to-rail, and will only go down to about 0.1V above ground. For this reason, R3 is added to the circuit to supply an output offset voltage of about 0.1V for a nominal supply voltage of 5V. This offset (10°C) must be subtracted when making measurements

referenced to the OP193 output. R3 also provides an open thermocouple detection, forcing the output voltage to greater than 3V should the thermocouple open. Resistor R7 balances the DC input impedance of the OP193, and the 0.1µF film capacitor reduces noise coupling into its non-inverting input.

USING A TEMPERATURE SENSOR FOR COLD-JUNCTION COMPENSATION (TMP35)

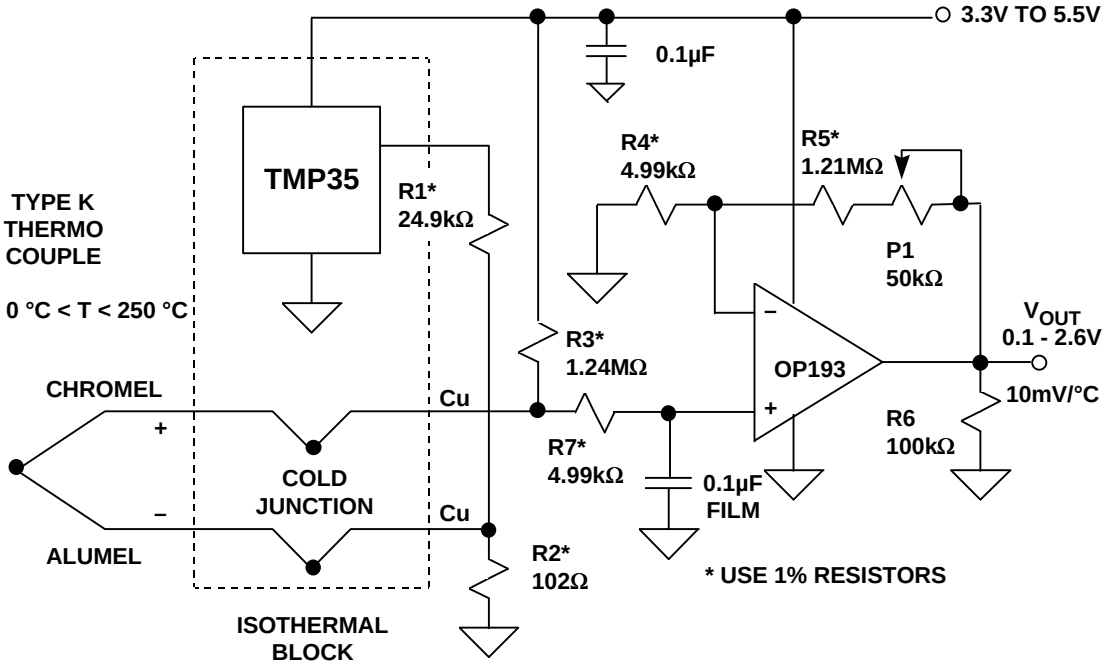


Figure 7.10

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip (see Figure 7.11). It combines an ice point reference with a precalibrated amplifier to provide a high level (10mV/°C) output directly from the thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby becoming a stand-alone Celsius transducer with 10mV/°C output. In such applications it is very important that the IC chip is at the same temperature as the cold junction of the thermocouple, which is usually achieved by keeping the two in close proximity and isolated from any heat sources.

The AD594/AD595 includes a thermocouple failure alarm that indicates if one or both thermocouple leads open. The alarm output has a flexible format which includes TTL drive capability. The device can be powered from a single-ended supply (which may be as low as +5V), but by including a negative supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will operate with a supply current of 160µA, but is also capable of delivering ±5mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristics of type J (iron/constantan) thermocouples, and the AD595 is laser trimmed for type K

(chromel/alumel). The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications. The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used with cold junctions between 0 to +50°C. The circuit shown in Figure 7.11 will provide a direct output from a type J thermocouple (AD594) or a type K thermocouple (AD595) capable of measuring 0 to +300°C.

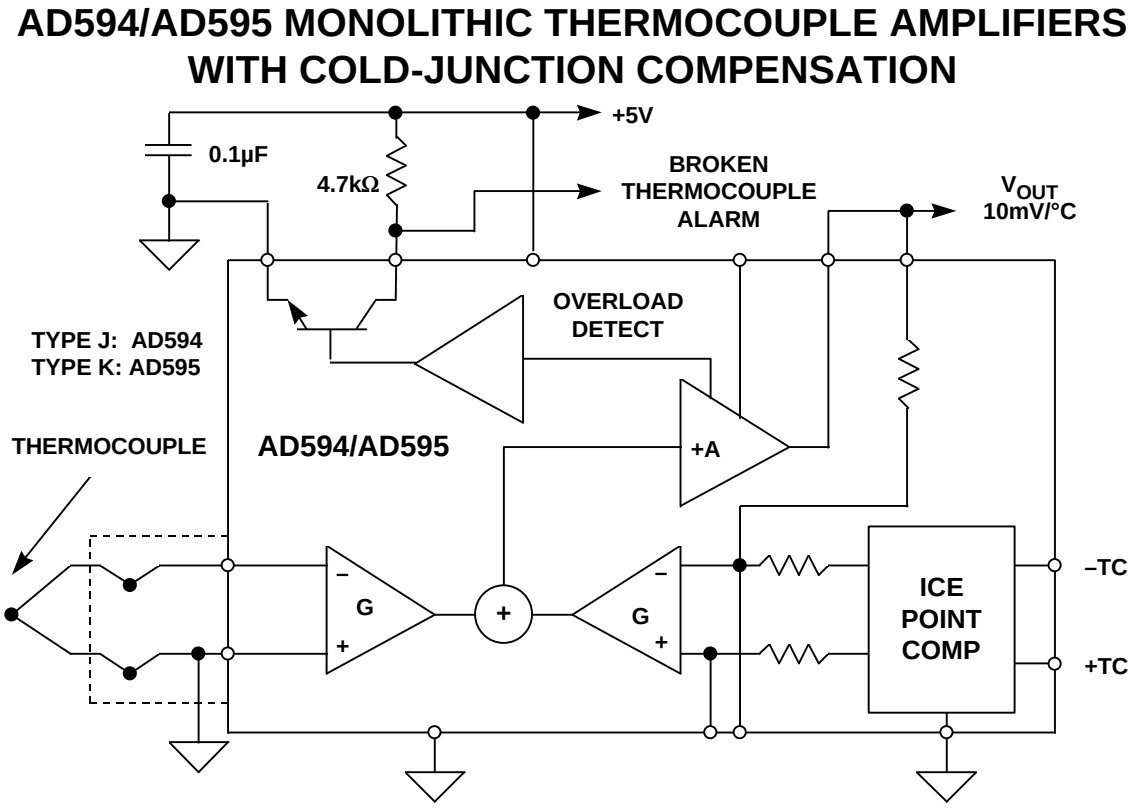


Figure 7.11

The AD596/AD597 are monolithic set-point controllers which have been optimized for use at elevated temperatures as are found in oven control applications. The device cold-junction compensates and amplifies a type J/K thermocouple to derive an internal signal proportional to temperature. They can be configured to provide a voltage output (10mV/°C) directly from type J/K thermocouple signals. The device is packaged in a 10-pin metal can and is trimmed to operate over an ambient range from +25°C to +100°C. The AD596 will amplify thermocouple signals covering the entire –200°C to +760°C temperature range recommended for type J thermocouples while the AD597 can accommodate –200°C to +1250°C type K inputs. They have a calibration accuracy of ±4°C at an ambient temperature of 60°C and an ambient temperature stability specification of 0.05°C/°C from +25°C to +100°C.

None of the thermocouple amplifiers previously described compensate for thermocouple non-linearity, they only provide conditioning and voltage gain. High

resolution ADCs such as the AD77XX family can be used to digitize the thermocouple output directly, allowing a microcontroller to perform the transfer function linearization as shown in Figure 7.12. The two multiplexed inputs to the ADC are used to digitize the thermocouple voltage and the cold-junction temperature sensor outputs directly. The input PGA gain is programmable from 1 to 128, and the ADC resolution is between 16 and 22 bits (depending upon the particular ADC selected). The microcontroller performs both the cold-junction compensation and the linearization arithmetic.

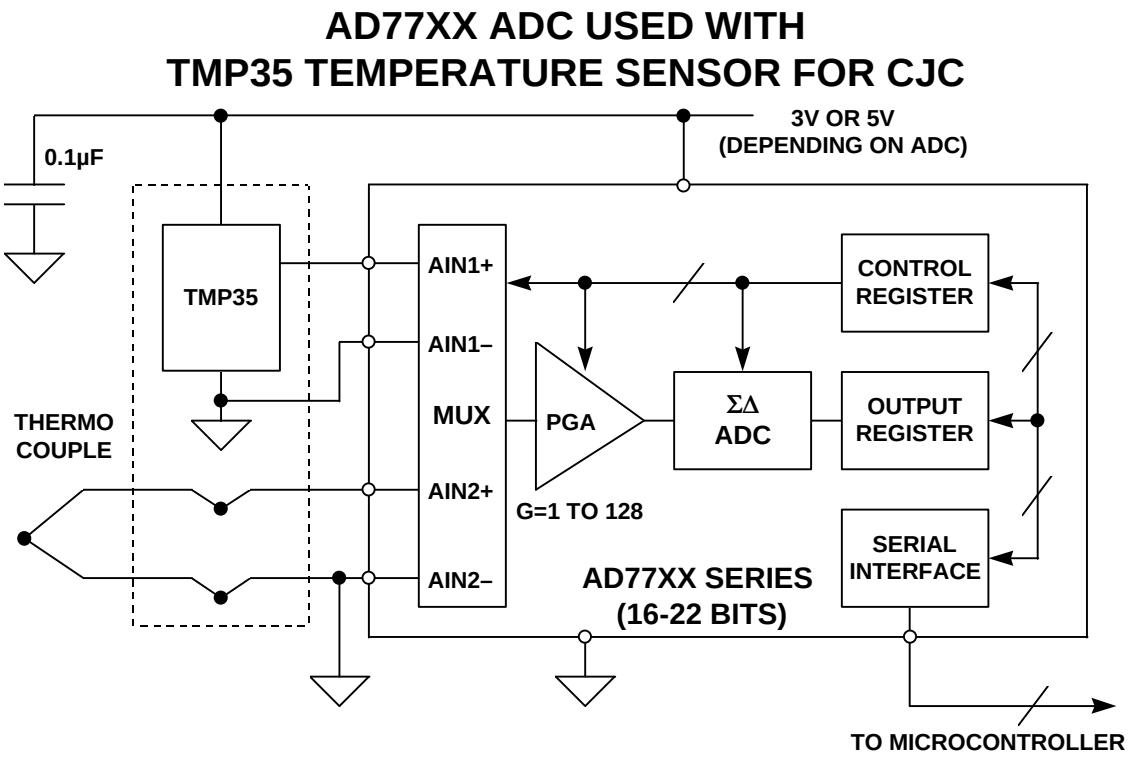


Figure 7.12

RESISTANCE TEMPERATURE DETECTORS (RTDS)

The Resistance Temperature Detector, or the RTD, is a sensor whose resistance changes with temperature. Typically built of a platinum (Pt) wire wrapped around a ceramic bobbin, the RTD exhibits behavior which is more accurate and more linear over wide temperature ranges than a thermocouple. Figure 7.13 illustrates the temperature coefficient of a 100Ω RTD and the Seebeck coefficient of a Type S thermocouple. Over the entire range (approximately –200°C to +850°C), the RTD is a more linear device. Hence, linearizing an RTD is less complex.

RESISTANCE TEMPERATURE DETECTORs (RTD)

- **Platinum (Pt) the Most Common**
- **100Ω, 1000Ω Standard Values**
- **Typical TC = 0.385% / °C,**
  0.385Ω / °C for 100Ω Pt RTD
- **Good Linearity - Better than Thermocouple, Easily Compensated**

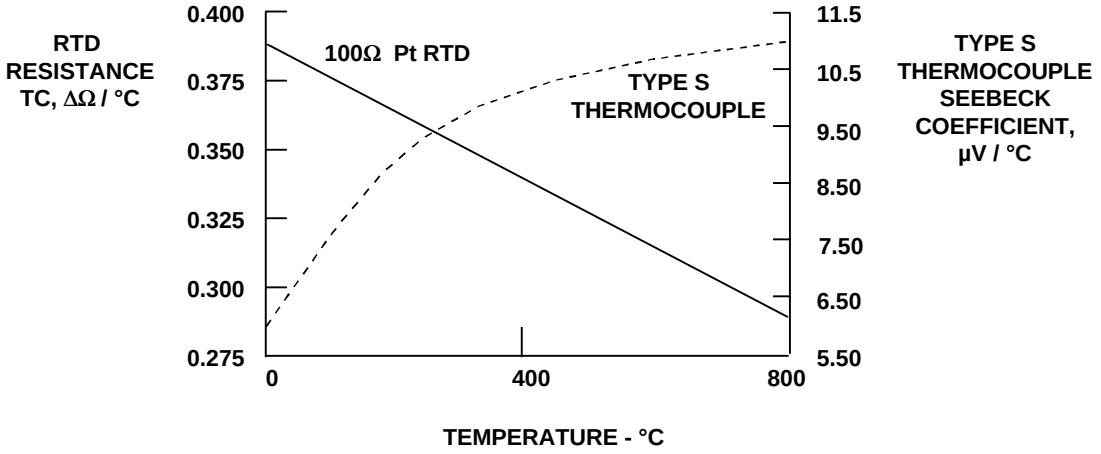


Figure 7.13

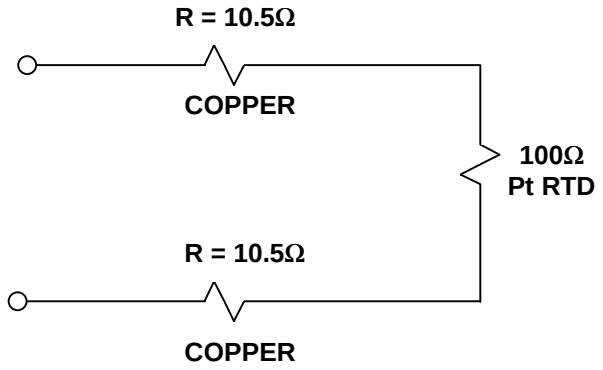
Unlike a thermocouple, however, an RTD is a passive sensor and requires current excitation to produce an output voltage. The RTD's low temperature coefficient of 0.385%/°C requires similar high-performance signal conditioning circuitry to that used by a thermocouple; however, the voltage drop across an RTD is much larger than a thermocouple output voltage. A system designer may opt for large value RTDs with higher output, but large-valued RTDs exhibit slow response times. Furthermore, although the cost of RTDs is higher than that of thermocouples, they use copper leads, and thermoelectric effects from terminating junctions do not affect their accuracy. And finally, because their resistance is a function of the absolute temperature, RTDs require no cold-junction compensation.

Caution must be exercised using current excitation because the current through the RTD causes heating. This self-heating changes the temperature of the RTD and appears as a measurement error. Hence, careful attention must be paid to the design of the signal conditioning circuitry so that self-heating is kept below 0.5°C. Manufacturers specify self-heating errors for various RTD values and sizes in still and in moving air. To reduce the error due to self-heating, the minimum current should be used for the required system resolution, and the largest RTD value chosen that results in acceptable response time.

Another effect that can produce measurement error is voltage drop in RTD lead wires. This is especially critical with low-value 2-wire RTDs because the temperature coefficient and the absolute value of the RTD resistance are both small. If the RTD is located a long distance from the signal conditioning circuitry, then the lead resistance can be ohms or tens of ohms, and a small amount of lead resistance can contribute a significant error to the temperature measurement. To illustrate

this point, let us assume that a 100Ω platinum RTD with 30-gauge copper leads is located about 100 feet from a controller's display console. The resistance of 30-gauge copper wire is 0.105Ω/ft, and the two leads of the RTD will contribute a total 21Ω to the network which is shown in Figure 7.14. This additional resistance will produce a 55°C error in the measurement! The leads' temperature coefficient can contribute an additional, and possibly significant, error to the measurement. To eliminate the effect of the lead resistance, a 4-wire technique is used.

A 100Ω Pt RTD WITH 100 FEET OF 30-GAUGE LEAD WIRES



RESISTANCE TC OF COPPER = 0.40%/°C @ 20°C

RESISTANCE TC OF Pt RTD = 0.385%/ °C @ 20°C

Figure 7.14

In Figure 7.15, a 4-wire, or Kelvin, connection is made to the RTD. A constant current is applied though the FORCE leads of the RTD, and the voltage across the RTD itself is measured remotely via the SENSE leads. The measuring device can be a DVM or an instrumentation amplifier, and high accuracy can be achieved provided that the measuring device exhibits high input impedance and/or low input bias current. Since the SENSE leads do not carry appreciable current, this technique is insensitive to lead wire length. Sources of errors are the stability of the constant current source and the input impedance and/or bias currents in the amplifier or DVM.

RTDs are generally configured in a four-resistor bridge circuit. The bridge output is amplified by an instrumentation amplifier for further processing. However, high resolution measurement ADCs such as the AD77XX series allow the RTD output to be digitized directly. In this manner, linearization can be performed digitally, thereby easing the analog circuit requirements.

FOUR-WIRE OR KELVIN CONNECTION TO Pt RTD FOR ACCURATE MEASUREMENTS

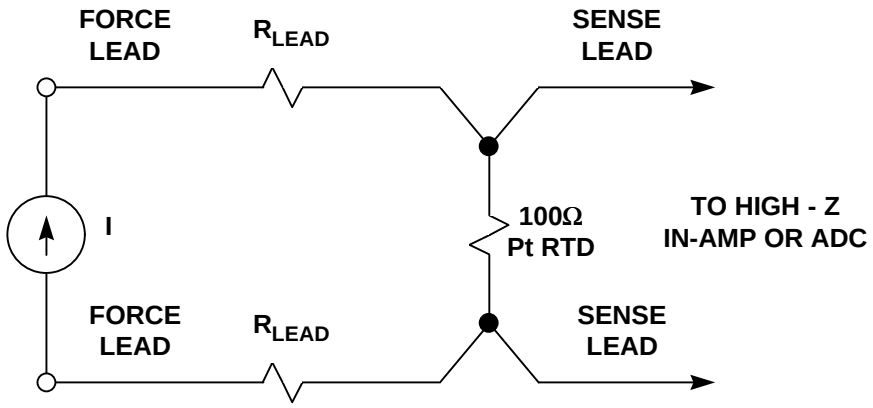


Figure 7.15

Figure 7.16 shows a 100Ω Pt RTD driven with a 400µA excitation current source. The output is digitized by one of the AD77XX series ADCs. Note that the RTD excitation current source also generates the 2.5V reference voltage for the ADC via the 6.25kΩ resistor. Variations in the excitation current do not affect the circuit accuracy, since both the input voltage and the reference voltage vary ratiometrically with the excitation current. However, the 6.25kΩ resistor must have a low temperature coefficient to avoid errors in the measurement. The high resolution of the ADC and the input PGA (gain of 1 to 128) eliminates the need for additional conditioning circuits.

The ADT70 is a complete Pt RTD signal conditioner which provides an output voltage of 5mV/°C when using a 1kΩ RTD (see Figure 7.17). The Pt RTD and the 1kΩ reference resistor are both excited with 1mA matched current sources. This allows temperature measurements to be made over a range of approximately –50°C to +800°C.

The ADT70 contains the two matched current sources, a precision rail-to-rail output instrumentation amplifier, a 2.5V reference, and an uncommitted rail-to-rail output op amp. The ADT71 is the same as the ADT70 except the internal voltage reference is omitted. A shutdown function is included for battery powered equipment that reduces the quiescent current from 3mA to 10µA. The gain or full-scale range for the Pt RTD and ADT701 system is set by a precision external resistor connected to the instrumentation amplifier. The uncommitted op amp may be used for scaling the internal voltage reference, providing a "Pt RTD open" signal or "over temperature" warning, providing a heater switching signal, or other external conditioning determined by the user. The ADT70 is specified for operation from –40°C to +125°C and is available in 20-pin DIP and SOIC packages.

INTERFACING A Pt RTD TO A HIGH RESOLUTION ADC

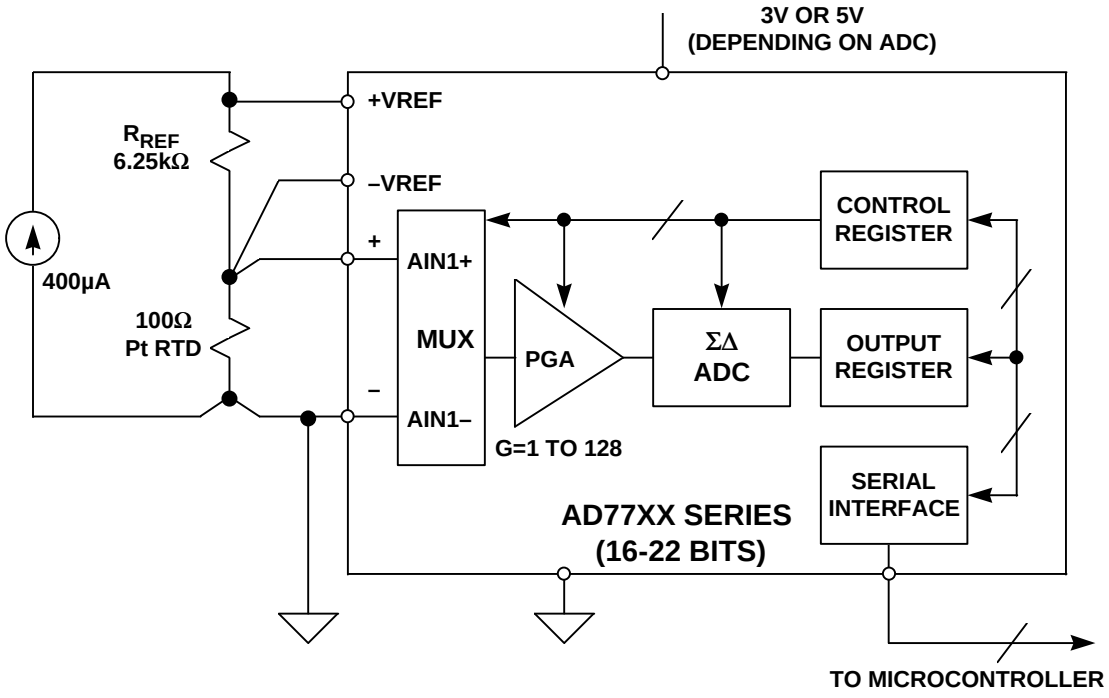


Figure 7.16

CONDITIONING THE PLATINUM RTD USING THE ADT70

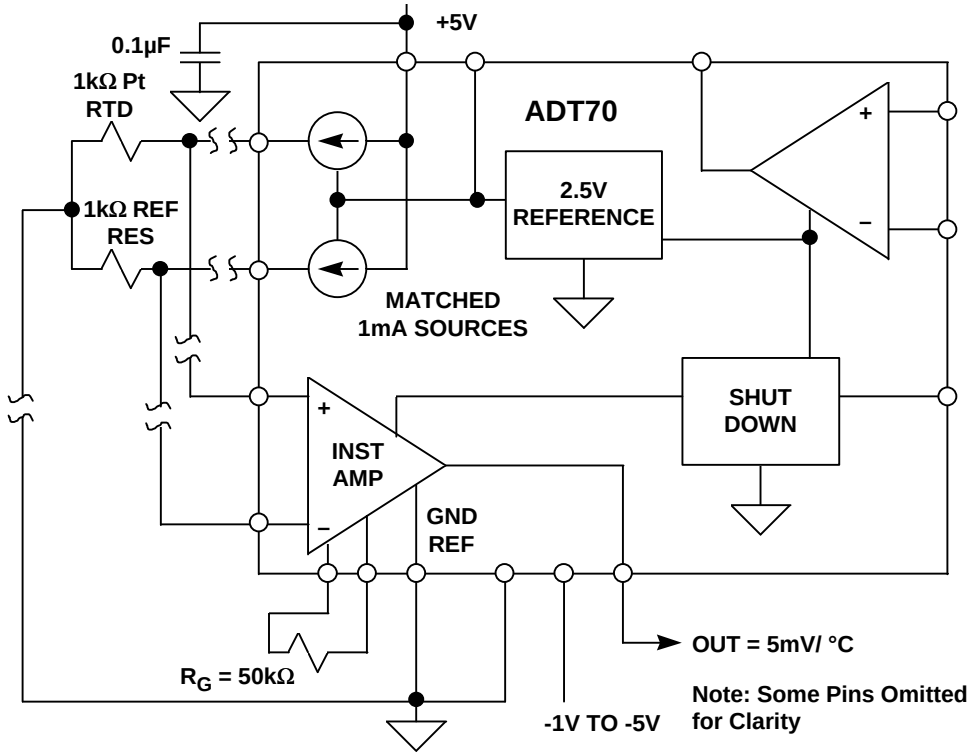


Figure 7.17

THERMISTORS

Similar in function to the RTD, thermistors are low-cost temperature-sensitive resistors and are constructed of solid semiconductor materials which exhibit a positive or negative temperature coefficient. Although positive temperature coefficient devices are available, the most commonly used thermistors are those with a negative temperature coefficient. Figure 7.18 shows the resistance-temperature characteristic of a commonly used NTC (Negative Temperature Coefficient) thermistor. The thermistor is highly non-linear and, of the three temperature sensors discussed, is the most sensitive.

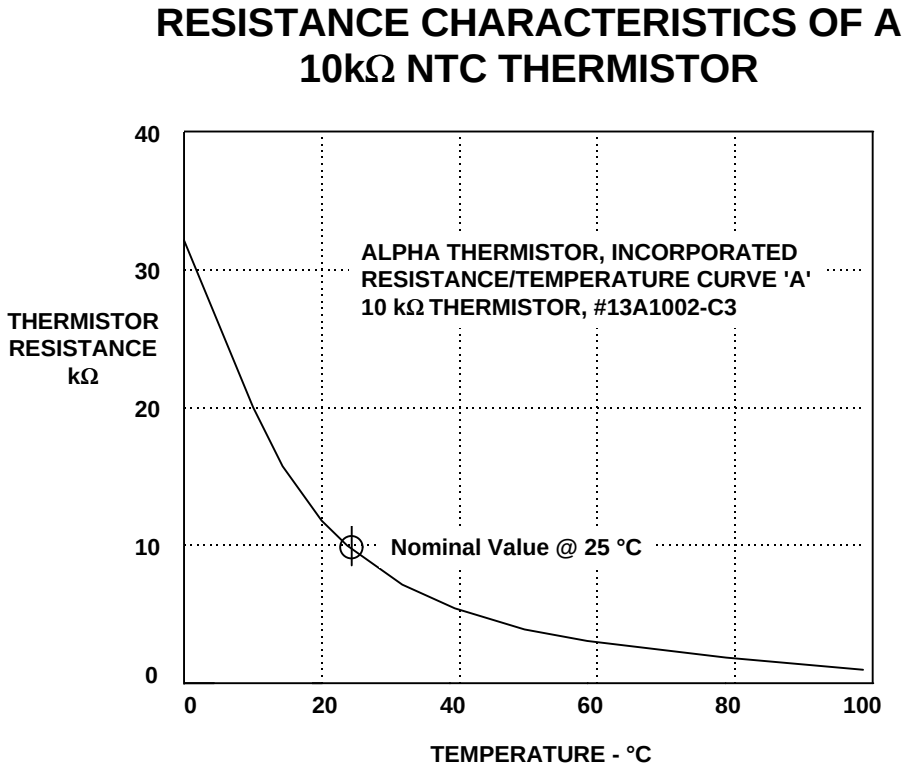


Figure 7.18

The thermistor's high sensitivity (typically, – 44,000ppm/°C at 25°C, as shown in Figure 7.19), allows it to detect minute variations in temperature which could not be observed with an RTD or thermocouple. This high sensitivity is a distinct advantage over the RTD in that 4-wire Kelvin connections to the thermistor are not needed to compensate for lead wire errors. To illustrate this point, suppose a 10kΩ NTC thermistor, with a typical 25°C temperature coefficient of –44,000ppm/°C, were substituted for the 100Ω Pt RTD in the example given earlier, then a total lead wire resistance of 21Ω would generate less than 0.05°C error in the measurement. This is roughly a factor of 500 improvement in error over an RTD.

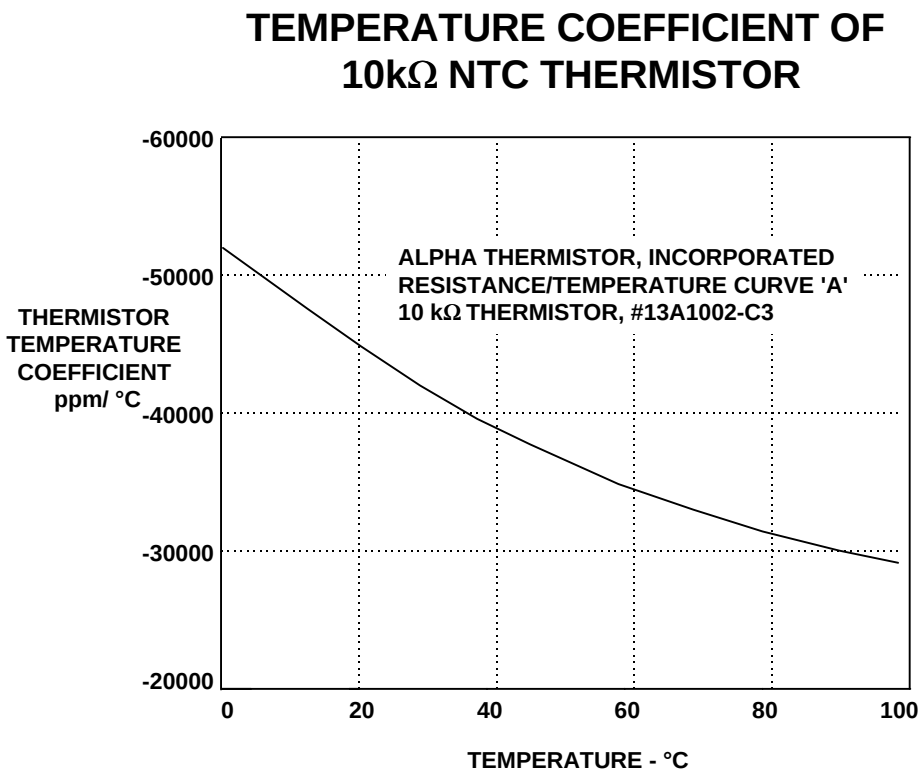


Figure 7.19

However, the thermistor's high sensitivity to temperature does not come without a price. As was shown in Figure 7.18, the temperature coefficient of thermistors does not decrease linearly with increasing temperature as it does with RTDs; therefore, linearization is required for all but the narrowest of temperature ranges. Thermistor applications are limited to a few hundred degrees at best because they are more susceptible to damage at high temperatures. Compared to thermocouples and RTDs, thermistors are fragile in construction and require careful mounting procedures to prevent crushing or bond separation. Although a thermistor's response time is short due to its small size, its small thermal mass makes it very sensitive to self-heating errors.

Thermistors are very inexpensive, highly sensitive temperature sensors. However, we have shown that a thermistor's temperature coefficient varies from –44,000 ppm/°C at 25°C to –29,000ppm/°C at 100°C. Not only is this non-linearity the largest source of error in a temperature measurement, it also limits useful applications to very narrow temperature ranges if linearization techniques are not used.

It is possible to use a thermistor over a wide temperature range only if the system designer can tolerate a lower sensitivity to achieve improved linearity. One approach to linearizing a thermistor is simply shunting it with a fixed resistor. Paralleling the thermistor with a fixed resistor increases the linearity significantly. As shown in Figure 7.20, the parallel combination exhibits a more linear variation with temperature compared to the thermistor itself. Also, the sensitivity of the combination still is high compared to a thermocouple or RTD. The primary

disadvantage to this technique is that linearization can only be achieved within a narrow range.

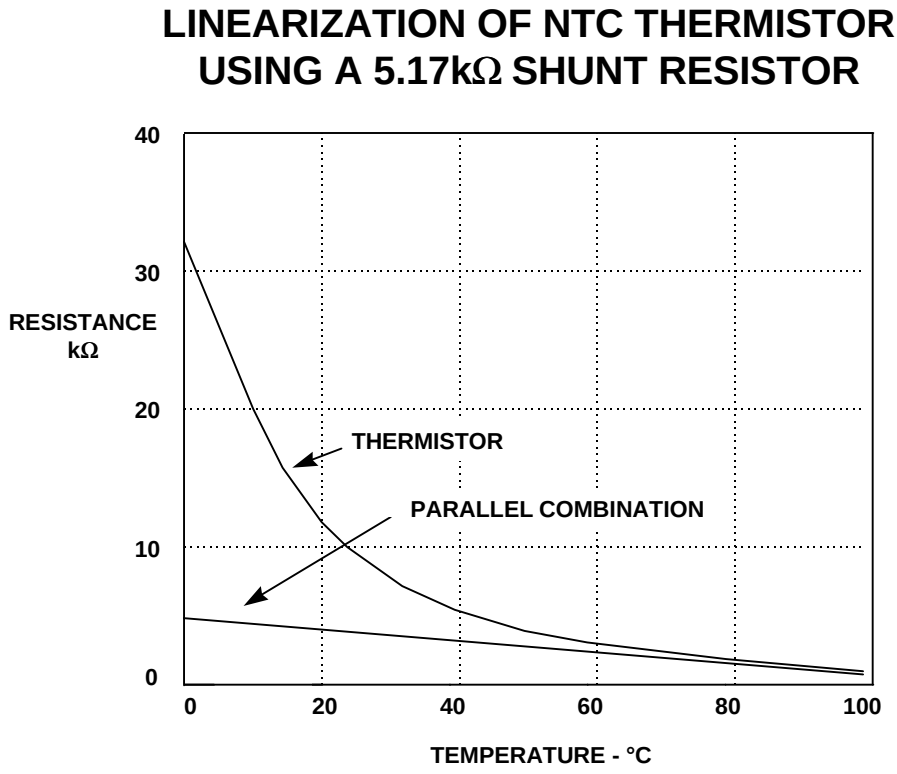


Figure 7.20

The value of the fixed resistor can be calculated from the following equation:

$$R = \frac{RT2 \cdot (RT1 + RT3) - 2 \cdot RT1 \cdot RT3}{RT1 + RT3 - 2 \cdot RT2},$$

where RT1 is the thermistor resistance at T1, the lowest temperature in the measurement range, RT3 is the thermistor resistance at T3, the highest temperature in the range, and RT2 is the thermistor resistance at T2, the midpoint, T2 = (T1 +T3)/2.

For a typical 10kΩ NTC thermistor, RT1 = 32,650Ω at 0°C, RT2 = 6,532Ω at 35°C, and RT3 = 1,752Ω at 70°C. This results in a value of 5.17kΩ for R. The accuracy needed in the signal conditioning circuitry depends on the linearity of the network. For the example given above, the network shows a non-linearity of – 2.3°C/ + 2.0 °C.

The output of the network can be applied to an ADC to perform further linearization as shown in Figure 7.21. Note that the output of the thermistor network has a slope of approximately –10mV/°C, which implies a 12-bit ADC has more than sufficient resolution.

LINEARIZED THERMISTOR AMPLIFIER

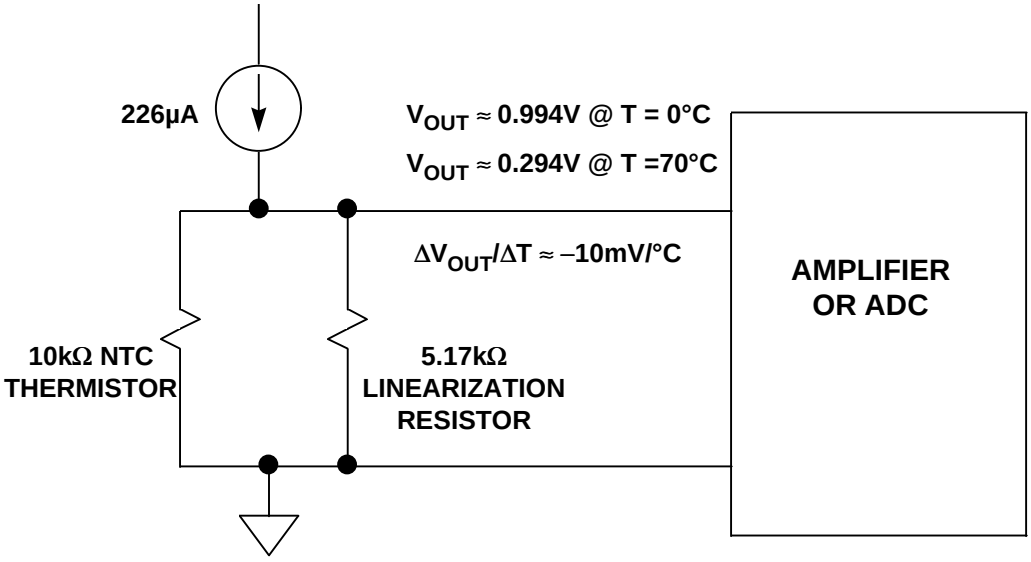


Figure 7.21

SEMICONDUCTOR TEMPERATURE SENSORS

Modern semiconductor temperature sensors offer high accuracy and high linearity over an operating range of about –55°C to +150°C. Internal amplifiers can scale the output to convenient values, such as 10mV/°C. They are also useful in cold-junction-compensation circuits for wide temperature range thermocouples.

All semiconductor temperature sensors make use of the relationship between a bipolar junction transistor's (BJT) base-emitter voltage to its collector current:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$$

where k is Boltzmann's constant, T is the absolute temperature, q is the charge of an electron, and I_S is a current related to the geometry and the temperature of the transistors. (The equation assumes a voltage of at least a few hundred mV on the collector, and ignores Early effects.)

If we take N transistors identical to the first (see Figure 7.22) and allow the total current I_C to be shared equally among them, we find that the new base-emitter voltage is given by the equation

$$V_N = \frac{kT}{q} \ln\left(\frac{I_C}{N \cdot I_S}\right)$$

BASIC RELATIONSHIPS FOR SEMICONDUCTOR TEMPERATURE SENSORS

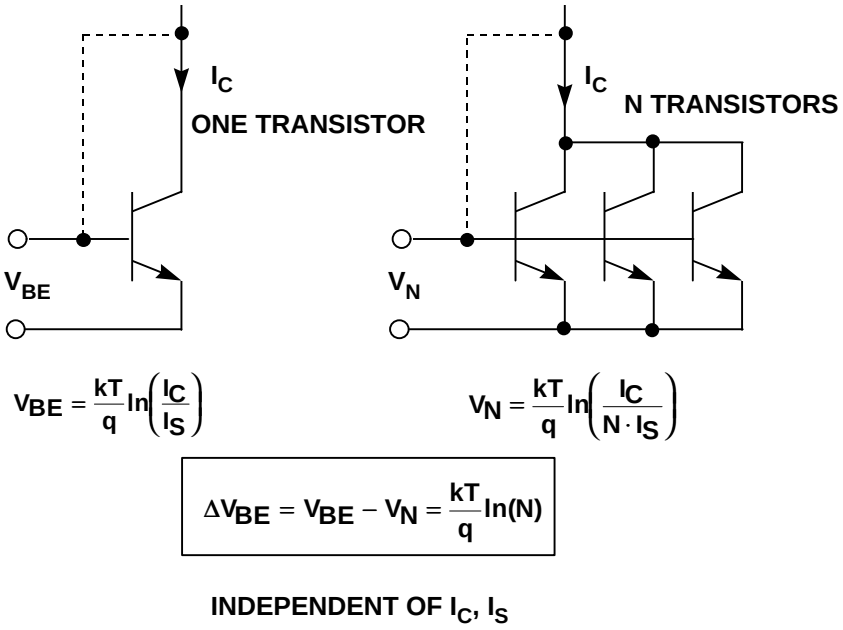


Figure 7.22

Neither of these circuits is of much use by itself because of the strongly temperature dependent current I_S, but if we have equal currents in one BJT and N similar BJTs then the expression for the *difference* between the two base-emitter voltages is proportional to absolute temperature and does not contain I_S.

$$\Delta V_{BE} = V_{BE} - V_N = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) - \frac{kT}{q} \ln\left(\frac{I_C}{N \cdot I_S}\right)$$

$$\Delta V_{BE} = V_{BE} - V_N = \frac{kT}{q} \left[\ln\left(\frac{I_C}{I_S}\right) - \ln\left(\frac{I_C}{N \cdot I_S}\right) \right]$$

$$\Delta V_{BE} = V_{BE} - V_N = \frac{kT}{q} \ln\left[\left(\frac{I_C}{I_S}\right) \Big/ \left(\frac{I_C}{N \cdot I_S}\right) \right] = \frac{kT}{q} \ln(N)$$

The circuit shown in Figure 7.23 implements the above equation and is known as the "Brokaw Cell" (see Reference 10). The voltage $\Delta V_{BE} = V_{BE} - V_N$ appears across resistor R2. The emitter current in Q2 is therefore $\Delta V_{BE}/R2$. The op amp's servo loop and the resistors, R, force the same current to flow through Q1. The Q1 and Q2 currents are equal and are summed and flow into resistor R1. The corresponding voltage developed across R1 is proportional to absolute temperature (PTAT) and given by:

$$V_{PTAT} = \frac{2R1(V_{BE} - V_N)}{R2} = 2\frac{R1}{R2}\frac{kT}{q}\ln(N).$$

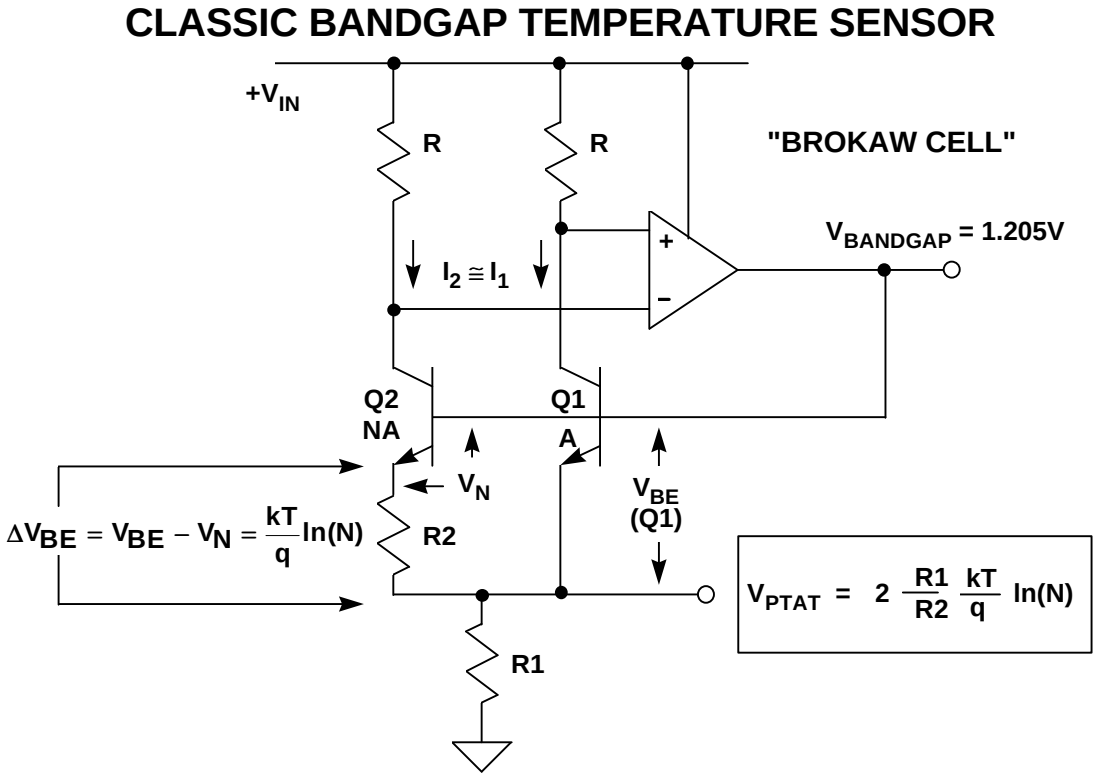


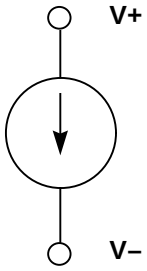
Figure 7.23

The bandgap cell reference voltage, $V_{BANDGAP}$, appears at the base of Q1 and is the sum of $V_{BE}(Q1)$ and V_{PTAT}. $V_{BE(Q1)}$ is complementary to absolute temperature (CTAT), and summing it with V_{PTAT} causes the bandgap voltage to be constant with respect to temperature (assuming proper choice of R1/R2 ratio and N to make the bandgap voltage equal to1.205V). This circuit is the basic *band-gap* temperature sensor, and is widely used in semiconductor temperature sensors.

Current and Voltage Output Temperature Sensors

The concepts used in the bandgap temperature sensor discussion above can be used as the basis for a variety of IC temperature sensors to generate either current or voltage outputs. The AD592 and TMP17 (see Figure 7.24) are current output sensors which have scale factors of 1µA/K. The sensors do not require external calibration and are available in several accuracy grades. The AD592 is available in three accuracy grades. The highest grade version (AD592CN) has a maximum error @ 25ºC of ±0.5ºC and ±1.0ºC error from –25ºC to +105ºC. Linearity error is ±0.35ºC. The TMP17 is available in two accuracy grades. The highest grade version (TMP17F) has a maximum error @ 25ºC of ±2.5ºC and ±3.5ºC error from –40ºC to +105ºC. Typical linearity error is ±0.5ºC. The AD592 is available in a TO-92 package and the TMP17 in an SO-8 package.

CURRENT OUTPUT SENSORS: AD592, TMP17



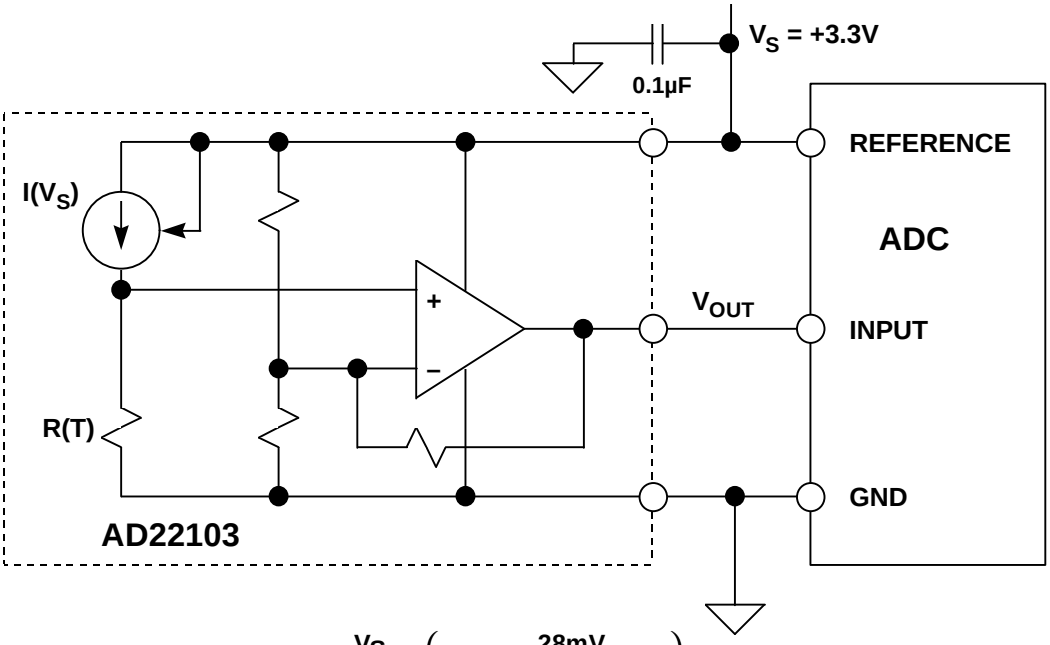
AD592: TO-92 PACKAGE

TMP17: SO-8 PACKAGE

- 1µA/K Scale Factor
- Nominal Output Current @ +25°C: 298.2µA
- Operation from 4V to 30V
- ±0.5°C Max Error @ 25°C, ±1.0°C Error Over Temp, ±0.1°C Typical Nonlinearity (AD592CN)
- ±2.5°C Max Error @ 25°C, ±3.5°C Error Over Temp, ±0.5°C Typical Nonlinearity (TMP17F)
- AD592 Specified from –25°C to +105°C
- TMP17 Specified from –40°C to +105°C

Figure 7.24

RATIOMETRIC VOLTAGE OUTPUT SENSORS



$$V_{OUT} = \frac{V_S}{3.3V} \times \left(0.25V + \frac{28mV}{°C} \times T_A \right)$$

Figure 7.25

In some cases, it is desirable for the output of a temperature sensor to be ratiometric with its supply voltage. The AD22103 (see Figure 7.25) has an output that is ratiometric with its supply voltage (nominally 3.3V) according to the equation:

$$V_{OUT} = \frac{V_S}{3.3V} \times \left(0.25V + \frac{28mV}{°C} \times T_A \right).$$

The circuit shown in Figure 7.25 uses the AD22103 power supply as the reference to the ADC, thereby eliminating the need for a precision voltage reference. The AD22103 is specified over a range of 0°C to +100°C and has an accuracy better than ±2.5°C and a linearity better than ±0.5°C.

The TMP35/TMP36/TMP37 are low voltage (2.7V to 5.5V) SOT-23 (5-pin), SO-8, or TO-92 packaged voltage output temperature sensors with a 10mV/°C (TMP35/36) or 20mV/°C (TMP37) scale factor (see Figure 7.26). Supply current is below 50µA, providing very low self-heating (less than 0.1°C in still air). A shutdown feature is provided which reduces the current to 0.5µA.

The TMP35 provides a 250mV output at +25°C and reads temperature from +10°C to +125°C. The TMP36 is specified from –40°C to +125°C. and provides a 750mV output at 25°C. Both the TMP35 and TMP36 have an output scale factor of +10mV/°C. The TMP37 is intended for applications over the range +5°C to +100°C, and provides an output scale factor of 20mV/°C. The TMP37 provides a 500mV output at +25°C.

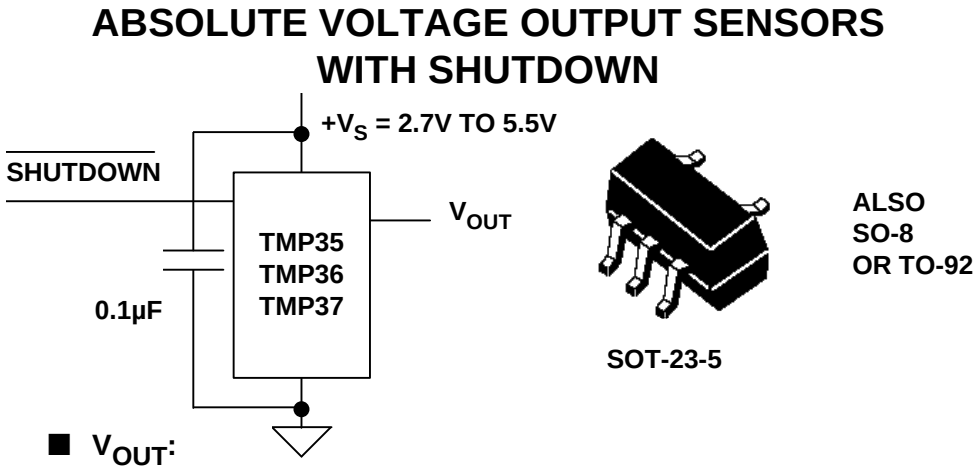
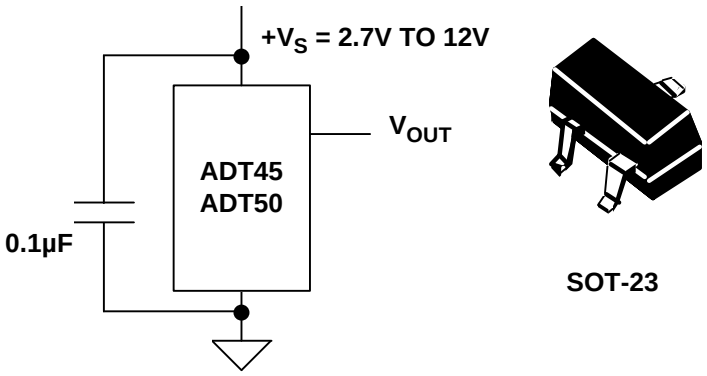


Figure 7.26

The ADT45/ADT50 are voltage output temperature sensors packaged in a SOT-23-3 package designed for an operating voltage of 2.7V to 12V (see Figure 7.27). The devices are specified over the range of –40ºC to +125ºC. The output scale factor for both devices is 10mV/ºC. Typical accuracies are ±1ºC at +25ºC and ±2ºC over the –40ºC to +125ºC range. The ADT45 provides a 250mV output at +25ºC and is specified for temperature from 0ºC to +100ºC. The ADT50 provides a 750mV output at +25ºC and is specified for temperature from –40ºC to +125ºC.

ADT45/ADT50 ABSOLUTE VOLTAGE OUTPUT SENSORS



- V_{OUT}:
  - ADT45, 250mV @ 25°C, 10mV/°C Scale Factor
  - ADT50, 750mV @ 25°C, 10mV/°C Scale Factor
- ±2°C Error Over Temp (Typical), ±0.5°C Non-Linearity (Typical)
- Specified –40°C to +125°C
- 60µA Quiescent Current

Figure 7.27

If the ADT45/ADT50 sensors are thermally attached and protected, they can be used in any temperature measurement application where the maximum temperature range of the medium is between –40°C to +125°C. Properly cemented or glued to the surface of the medium, these sensors will be within 0.01°C of the surface temperature. Caution should be exercised, as any wiring to the device can act as heat pipes, introducing errors if the surrounding air-surface interface is not isothermal. Avoiding this condition is easily achieved by dabbing the leads of the sensor and the hookup wires with a bead of thermally conductive epoxy. This will ensure that the ADT45/ADT50 die temperature is not affected by the surrounding air temperature.

In the SOT-23-3 package, the thermal resistance junction-to-case, θ_{JC}, is 180°C/W. The thermal resistance case-to-ambient, θ_{CA}, is the difference between θ_{JA} and θ_{JC}, and is determined by the characteristics of the thermal connection. With no air flow and the device soldered on a PC board, θ_{JA} is 300°C/W. The temperature sensor's power dissipation, P_D, is the product of the total voltage across the device and its total supply current (including any current delivered to the load). The rise in die temperature above the medium's ambient temperature is given by:

$$T_J = P_D \times (\theta_{JC} + \theta_{CA}) + T_A.$$

Thus, the die temperature rise of an unloaded ADT45/ADT50 (SOT-23-3 package) soldered on a board in still air at 25°C and driven from a +5V supply (quiescent current = 60µA, P_D = 300µW) is less than 0.09°C. In order to prevent further temperature rise, it is important to minimize the load current, always keeping it less than 100µA.

The transient response of the ADT45/ADT50 sensors to a step change in temperature is determined by the thermal resistances and the thermal mass of the die and the case. The thermal mass of the case varies with the measurement medium since it includes anything that is in direct contact with the package. In all practical cases, the thermal mass of the case is the limiting factor in the thermal response time of the sensor and can be represented by a single-pole RC time constant. Thermal mass is often considered the thermal equivalent of electrical capacitance.

The thermal time constant of a temperature sensor is defined to be the time required for the sensor to reach 63.2% of the final value for a step change in the temperature. Figure 7.28 shows the thermal time constant of the ADT45/ADT50 series of sensors with the SOT-23-3 package soldered to 0.338" x 0.307" copper PC board as a function of air flow velocity. Note the rapid drop from 32 seconds to 12 seconds as the air velocity increases from 0 (still air) to 100 LFPM. As a point of reference, the thermal time constant of the ADT45/ADT50 series in a stirred oil bath is less than 1 second, which verifies that the major part of the thermal time constant is determined by the case.

The power supply pin of these sensors should be bypassed to ground with a 0.1µF ceramic capacitor having very short leads (preferably surface mount) and located as close to the power supply pin as possible. Since these temperature sensors operate on very little supply current and could be exposed to very hostile electrical environments, it is important to minimize the effects of EMI/RFI on these devices. The effect of RFI on these temperature sensors is manifested as abnormal DC shifts in the output voltage due to rectification of the high frequency noise by the internal IC junctions. In those cases where the devices are operated in the presence of high frequency radiated or conducted noise, a large value tantalum electrolytic capacitor (>2.2µF) placed across the 0.1µF ceramic may offer additional noise immunity.

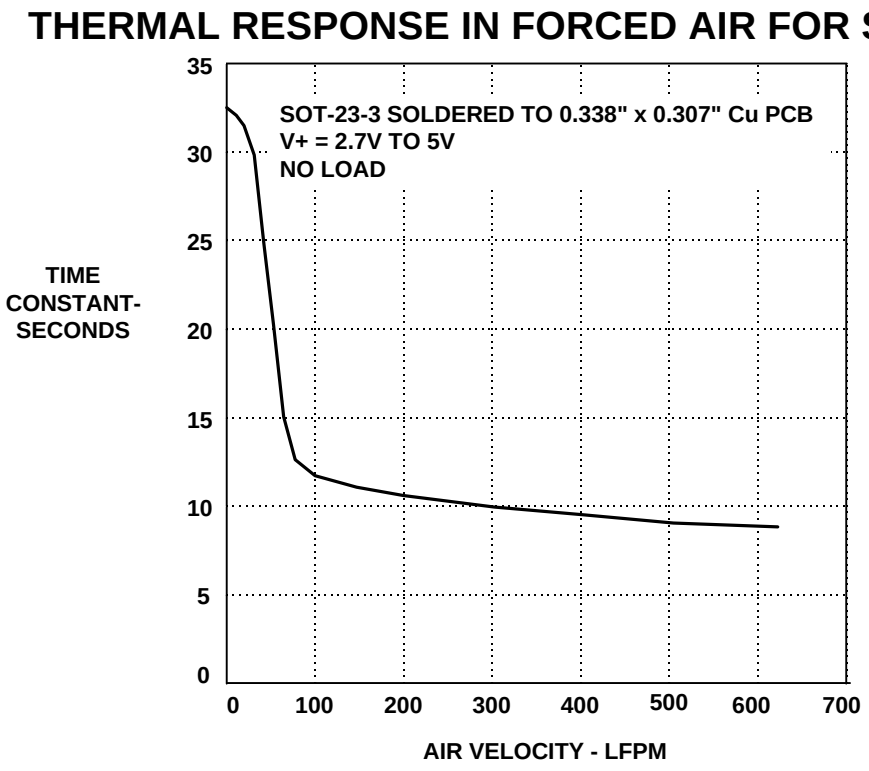


Figure 7.28

Digital Output Temperature Sensors

Temperature sensors which have digital outputs have a number of advantages over those with analog outputs, especially in remote applications. Opto-isolators can also be used to provide galvanic isolation between the remote sensor and the measurement system. A voltage-to-frequency converter driven by a voltage output temperature sensor accomplishes this function, however, more sophisticated ICs are now available which are more efficient and offer several performance advantages.

The TMP03/TMP04 digital output sensor family includes a voltage reference, V_{PTAT} generator, sigma-delta ADC, and a clock source (see Figure 7.29). The sensor output is digitized by a first-order sigma-delta modulator, also known as the "charge balance" type analog-to-digital converter. This converter utilizes time-domain oversampling and a high accuracy comparator to deliver 12 bits of effective accuracy in an extremely compact circuit.

The output of the sigma-delta modulator is encoded using a proprietary technique which results in a serial digital output signal with a mark-space ratio format (see Figure 7.30) that is easily decoded by any microprocessor into either degrees centigrade or degrees Fahrenheit, and readily transmitted over a single wire. Most importantly, this encoding method avoids major error sources common to other modulation techniques, as it is clock-independent. The nominal output frequency is 35Hz at + 25ºC, and the device operates with a fixed high-level pulse width (T1) of 10ms.

DIGITAL OUTPUT SENSORS: TMP03/04

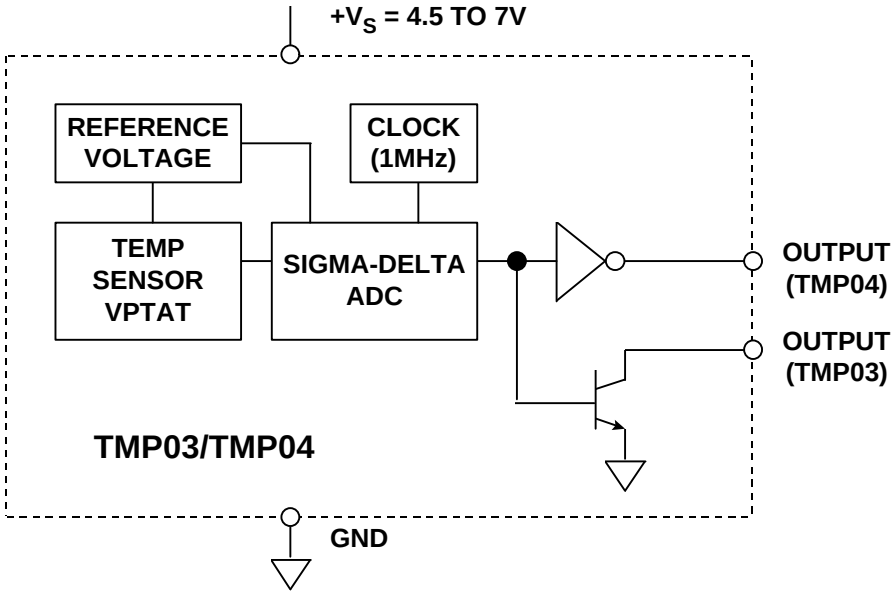
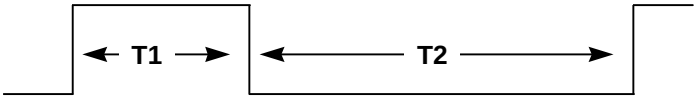


Figure 7.29

TMP03/TMP04 OUTPUT FORMAT



$$\text{TEMPERATURE (°C)} = 235 - \left(\frac{400 \times T1}{T2}\right)$$

$$\text{TEMPERATURE (°F)} = 455 - \left(\frac{720 \times T1}{T2}\right)$$

- T1 Nominal Pulse Width = 10ms
- ±1.5°C Error Over Temp, ±0.5°C Non-Linearity (Typical)
- Specified –40°C to +100°C
- Nominal T1/T2 @ 0°C = 60%
- Nominal Frequency @ +25°C = 35Hz
- 6.5mW Power Consumption @ 5V
- TO-92, SO-8, or TSSOP Packages

Figure 7.30

The TMP03/TMP04 output is a stream of digital pulses, and the temperature information is contained in the mark-space ratio per the equations:

$$\text{Temperature}\,(^\circ\text{C}) = 235 - \left(\frac{400 \times \text{T1}}{\text{T2}}\right)$$

$$\text{Temperature}\,(^\circ\text{F}) = 455 - \left(\frac{720 \times \text{T1}}{\text{T2}}\right).$$

Popular microcontrollers, such as the 80C51 and 68HC11, have on-chip timers which can easily decode the mark-space ratio of the TMP03/TMP04. A typical interface to the 80C51 is shown in Figure 7.31. Two timers, labeled *Timer 0* and *Timer 1* are 16 bits in length. The 80C51's system clock, divided by twelve, provides the source for the timers. The system clock is normally derived from a crystal oscillator, so timing measurements are quite accurate. Since the sensor's output is ratiometric, the actual clock frequency is not important. This feature is important because the microcontroller's clock frequency is often defined by some external timing constraint, such as the serial baud rate.

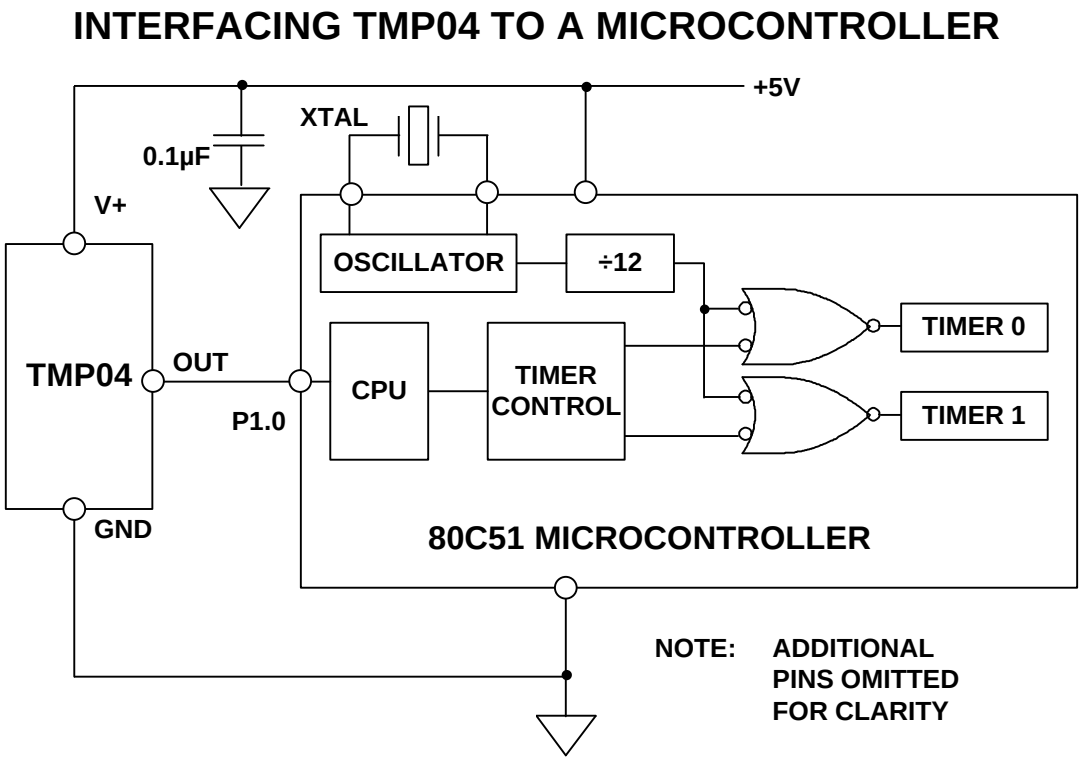


Figure 7.31

Software for the sensor interface is straightforward. The microcontroller simply monitors I/O port P1.0, and starts *Timer 0* on the rising edge of the sensor output. The microcontroller continues to monitor P1.0, stopping *Timer 0* and starting *Timer 1* when the sensor output goes low. When the output returns high, the sensor's T1 and T2 times are contained in registers *Timer 0* and *Timer 1*, respectively. Further software routines can then apply the conversion factor shown in the equations above and calculate the temperature.

The TMP03/TMP04 are ideal for monitoring the thermal environment within electronic equipment. For example, the surface mounted package will accurately reflect the thermal conditions which affect nearby integrated circuits. The TO-92 package, on the other hand, can be mounted above the surface of the board to measure the temperature of the air flowing over the board.

The TMP03 and TMP04 measure and convert the temperature at the surface of their own semiconductor chip. When they are used to measure the temperature of a nearby heat source, the thermal impedance between the heat source and the sensor must be considered. Often, a thermocouple or other temperature sensor is used to measure the temperature of the source, while the TMP03/TMP04 temperature is monitored by measuring T1 and T2. Once the thermal impedance is determined, the temperature of the heat source can be inferred from the TMP03/TMP04 output.

One example of using the TMP04 to monitor a high power dissipation microprocessor or other IC is shown in Figure 7.32. The TMP04, in a surface mount package, is mounted directly beneath the microprocessor's pin grid array (PGA) package. In a typical application, the TMP04's output would be connected to an ASIC where the mark-space ratio would be measured. The TMP04 pulse output provides a significant advantage in this application because it produces a linear temperature output, while needing only one I/O pin and without requiring an ADC.

MONITORING HIGH POWER MICROPROCESSOR OR DSP WITH TMP04

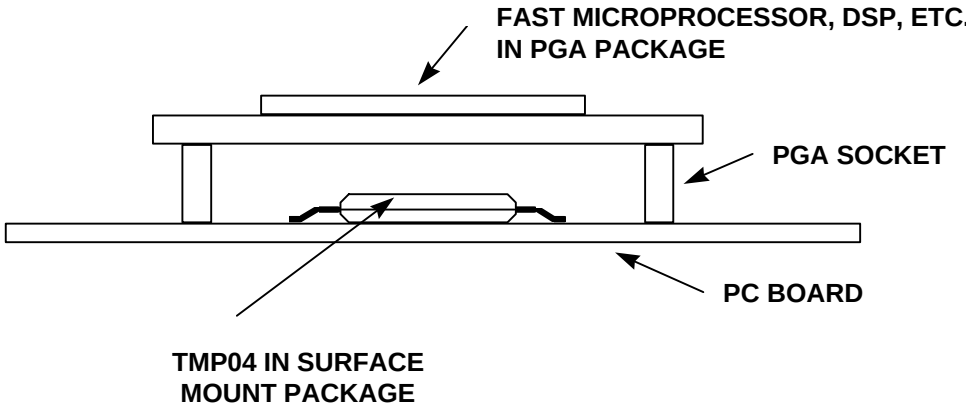


Figure 7.32

Thermostatic Switches and Setpoint Controllers

Temperature sensors used in conjunction with comparators can act as thermostatic switches. ICs such as the ADT05 accomplish this function at low cost and allow a single external resistor to program the setpoint to 2ºC accuracy over a range of –40ºC to +150ºC (see Figure 7.33). The device asserts an open collector output when the ambient temperature exceeds the user-programmed setpoint temperature. The ADT05 has approximately 4ºC of hysteresis which prevents rapid thermal on/off cycling. The ADT05 is designed to operate on a single supply voltage from +2.7V to

+7.0V facilitating operation in battery powered applications as well as industrial control systems. Because of low power dissipation (200µW @ 3.3V), self-heating errors are minimized, and battery life is maximized. An optional internal 200kΩ pull-up resistor is included to facilitate driving light loads such as CMOS inputs.

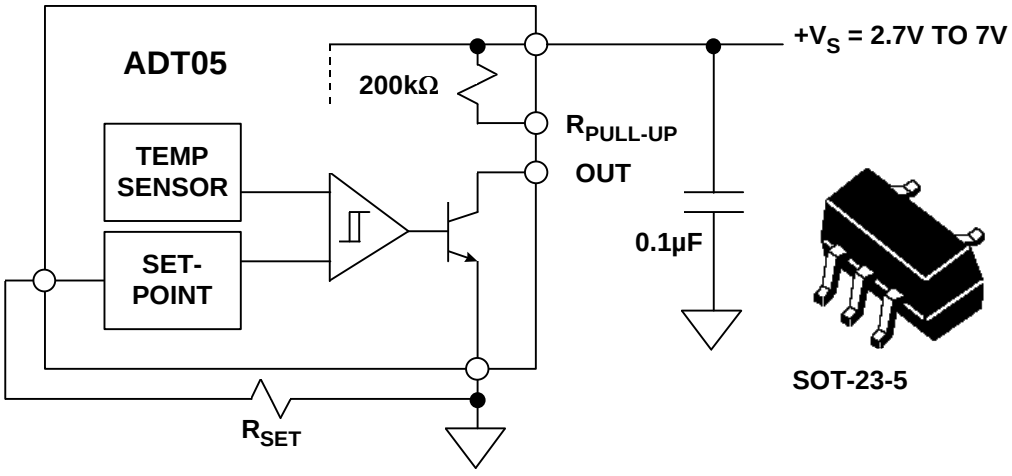
The setpoint resistor is determined by the equation:

$$R_{SET} = \frac{39M\Omega^{\circ}C}{T_{SET}(^{\circ}C) + 281.6^{\circ}C} - 90.3k\Omega.$$

The setpoint resistor should be connected directly between the R_{SET} pin (Pin 4) and the GND pin (Pin 5). If a ground plane is used, the resistor may be connected directly to this plane at the closest available point.

The setpoint resistor can be of nearly any resistor type, but its initial tolerance and thermal drift will affect the accuracy of the programmed switching temperature. For most applications, a 1% metal-film resistor will provide the best tradeoff between cost and accuracy. Once R_{SET} has been calculated, it may be found that the calculated value does not agree with readily available standard resistors of the chosen tolerance. In order to achieve a value as close as possible to the calculated value, a compound resistor can be constructed by connecting two resistors in series or parallel.

ADT05 THERMOSTATIC SWITCH



- ±2°C Setpoint Accuracy
- 4°C Preset Hysteresis
- Specified Operating Range: –40°C to + 150°C
- Power Dissipation: 200µW @ 3.3V

Figure 7.33

The TMP01 is a dual setpoint temperature controller which also generates a PTAT output voltage (see Figure 7.34 and 7.35). It also generates a control signal from one of two outputs when the device is either above or below a specific temperature range. Both the high/low temperature trip points and hysteresis band are determined by user-selected external resistors.

TMP01 PROGRAMMABLE SETPOINT CONTROLLER

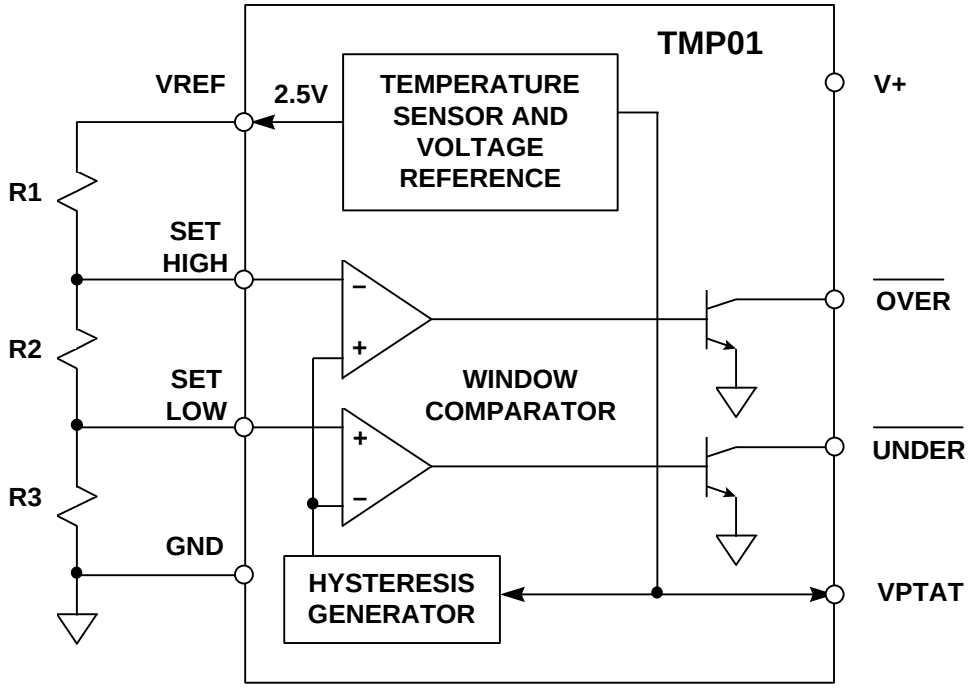


Figure 7.34

The TMP01 consists of a bandgap voltage reference combined with a pair of matched comparators. The reference provides both a constant 2.5V output and a PTAT output voltage which has a precise temperature coefficient of 5mV/K and is 1.49V (nominal) at +25ºC. The comparators compare VPTAT with the externally set temperature trip points and generate an open-collector output signal when one of their respective thresholds has been exceeded.

Hysteresis is also programmed by the external resistor chain and is determined by the total current drawn out of the 2.5V reference. This current is mirrored and used to generate a hysteresis offset voltage of the appropriate polarity after a comparator has been tripped. The comparators are connected in parallel, which guarantees that there is no hysteresis overlap and eliminates erratic transitions between adjacent trip zones.

The TMP01 utilizes laser trimmed thin-film resistors to maintain a typical temperature accuracy of ±1ºC over the rated temperature range. The open-collector outputs are capable of sinking 20mA, enabling the TMP01 to drive control relays directly. Operating from a +5V supply, quiescent current is only 500µA maximum.

TMP01 SETPOINT CONTROLLER KEY FEATURES

- **V_C: 4.5 to 13.2V**
- **Temperature Output: VPTAT, +5mV/K**
- **Nominal 1.49V Output @ 25°C**
- **±1°C Typical Accuracy Over Temperature**
- **Specified Operating Range: –55°C to + 125°C**
- **Resistor-Programmable Hysteresis**
- **Resistor-Programmable Setpoints**
- **Precision 2.5V ±8mV Reference**
- **400µA Quiescent Current, 1µA in Shutdown**
- **Packages: 8-Pin Dip, 8-Pin SOIC, 8-Pin TO-99**
- **Other Setpoint Controllers:**
  - **Dual Setpoint Controllers: ADT22/ADT23 (3V Versions of TMP01 with Internal Hysteresis)**
  - **Quad Setpoint Controller: ADT14**

Figure 7.35

The ADT22/23-series are similar to the TMP01 but have internal hysteresis and are designed to operate on a 3V supply. A quad (ADT14) setpoint controller is also available.

ADCs With On-Chip Temperature Sensors

The AD7816/7817/7818-series digital temperature sensors have on-board temperature sensors whose outputs are digitized by a 10-bit 9µs conversion time switched capacitor SAR ADC. The serial interface is compatible with the Intel 8051, Motorola SPI™ and QSPI™, and National Semiconductor's MICROWIRE™ protocol. The device family offers a variety of input options for further flexibility. The AD7416/7417/7418 are similar but have standard serial interfaces. Functional block diagrams of the AD7816, AD7817, and AD7818 are shown in Figures 7.36, 37, and 38, and key specifications in Figure 7.39

AD7816 10-BIT DIGITAL TEMPERATURE SENSOR WITH SERIAL INTERFACE

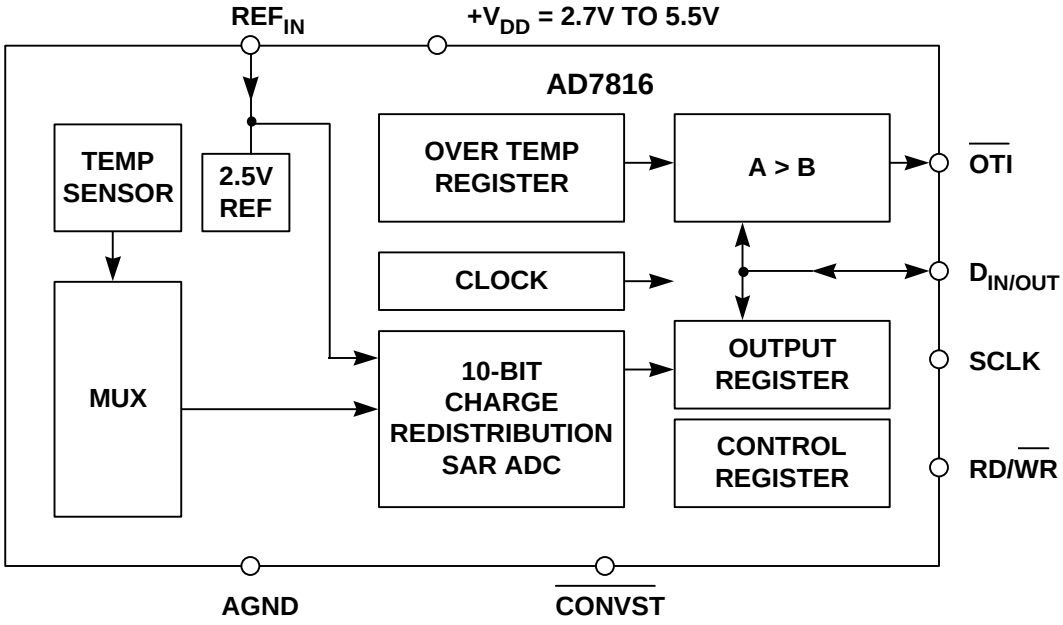


Figure 7.36

AD7817 10-BIT MUXED INPUT ADC WITH TEMP SENSOR

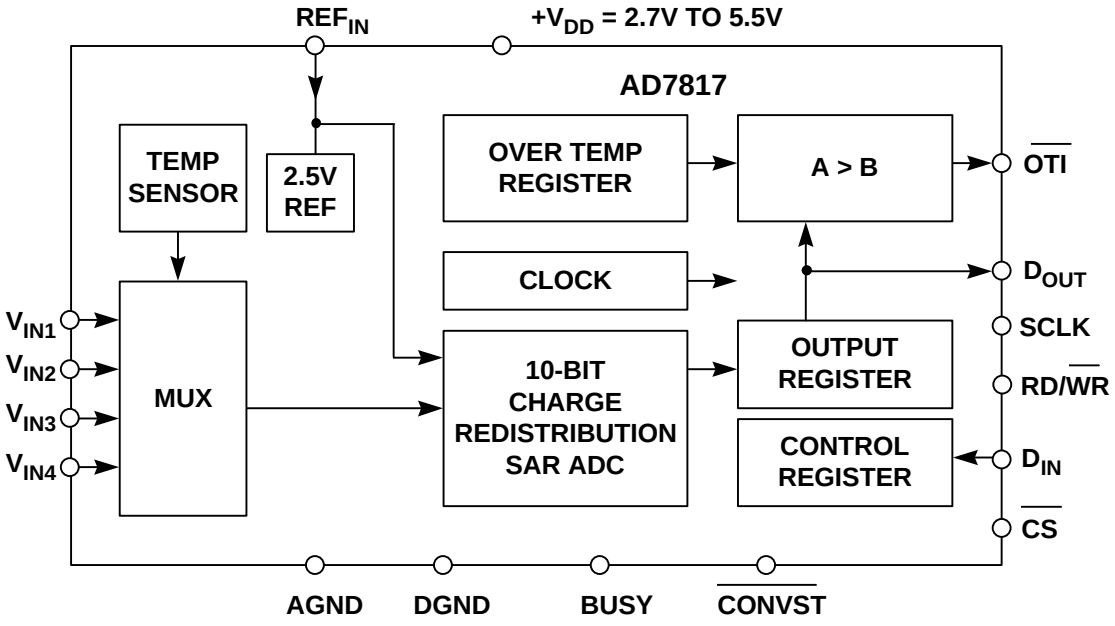


Figure 7.37

AD7818 SINGLE INPUT 10-BIT ADC WITH TEMP SENSOR

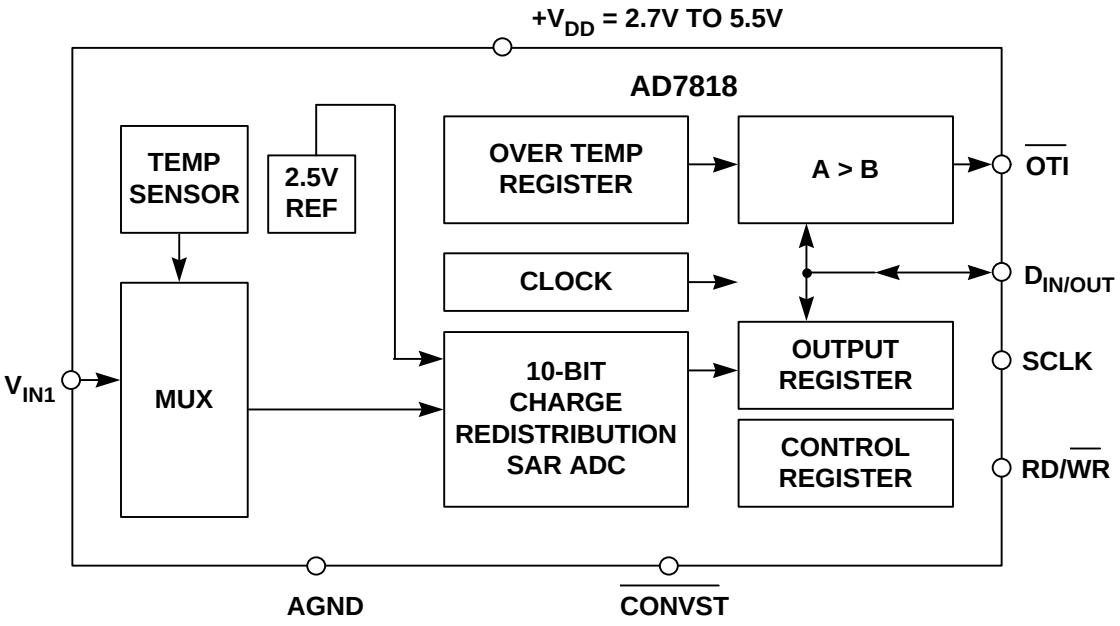


Figure 7.38

AD7816/7817/7818 - SERIES TEMP SENSOR 10-BIT ADCs WITH SERIAL INTERFACE

- 10-Bit ADC with 9µs Conversion Time
- Flexible Serial Interface (Intel 8051, Motorola SPI™ and QSPI™, National MICROWIRE™)
- On-Chip Temperature Sensor: –55°C to +125°C
- Temperature Accuracy: ± 2°C from –40°C to +85°C
- On-Chip Voltage Reference: 2.5V ±1%
- +2.7V to +5.5V Power Supply
- 4µW Power Dissipation at 10Hz Sampling Rate
- Auto Power Down after Conversion
- Over-Temp Interrupt Output
- Four Single-Ended Analog Input Channels: AD7817
- One Single-Ended Analog Input Channel: AD7818
- AD7416/7417/7418: Similar, but have I^2C Compatible Interface

Figure 7.39

MICROPROCESSOR TEMPERATURE MONITORING

Today's computers require that hardware as well as software operate properly, in spite of the many things that can cause a system crash or lockup. The purpose of hardware monitoring is to monitor the critical items in a computing system and take corrective action should problems occur.

Microprocessor supply voltage and temperature are two critical parameters. If the supply voltage drops below a specified minimum level, further operations should be halted until the voltage returns to acceptable levels. In some cases, it is desirable to reset the microprocessor under "brownout" conditions. It is also common practice to reset the microprocessor on power-up or power-down. Switching to a battery backup may be required if the supply voltage is low.

Under low voltage conditions it is mandatory to inhibit the microprocessor from writing to external CMOS memory by inhibiting the Chip Enable signal to the external memory.

Many microprocessors can be programmed to periodically output a "watchdog" signal. Monitoring this signal gives an indication that the processor and its software are functioning properly and that the processor is not stuck in an endless loop.

The need for hardware monitoring has resulted in a number of ICs, traditionally called "microprocessor supervisory products," which perform some or all of the above functions. These devices range from simple manual reset generators (with debouncing) to complete microcontroller-based monitoring sub-systems with on-chip temperature sensors and ADCs. Analog Devices' ADM-family of products is specifically to perform the various microprocessor supervisory functions required in different systems.

CPU temperature is critically important in the Pentium II microprocessors. For this reason, all new Pentium II devices have an on-chip substrate PNP transistor which is designed to monitor the actual chip temperature. The collector of the substrate PNP is connected to the substrate, and the base and emitter are brought out on two separate pins of the Pentium II.

The ADM1021 Microprocessor Temperature Monitor is specifically designed to process these outputs and convert the voltage into a digital word representing the chip temperature. The simplified analog signal processing portion of the ADM1021 is shown in Figure 7.40.

The technique used to measure the temperature is identical to the "ΔV_{BE}" principle previously discussed. Two different currents (I and N·I)are applied to the sensing transistor, and the voltage measured for each. In the ADM1021, the nominal currents are I = 6µA, (N = 17), N·I = 102µA. The change in the base-emitter voltage, ΔV_{BE}, is a PTAT voltage and given by the equation:

$$\Delta V_{BE} = \frac{kT}{q} \ln(N).$$

Figure 7.40 shows the external sensor as a substrate transistor, provided for temperature monitoring in the microprocessor, but it could equally well be a discrete transistor. If a discrete transistor is used, the collector should be connected to the base and not grounded. To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode. If the sensor is operating in a noisy environment, C may be optionally added as a noise filter. Its value is typically 2200pF, but should be no more than 3000pF.

ADM1021 MICROPROCESSOR TEMPERATURE MONITOR INPUT SIGNAL CONDITIONING CIRCUITS

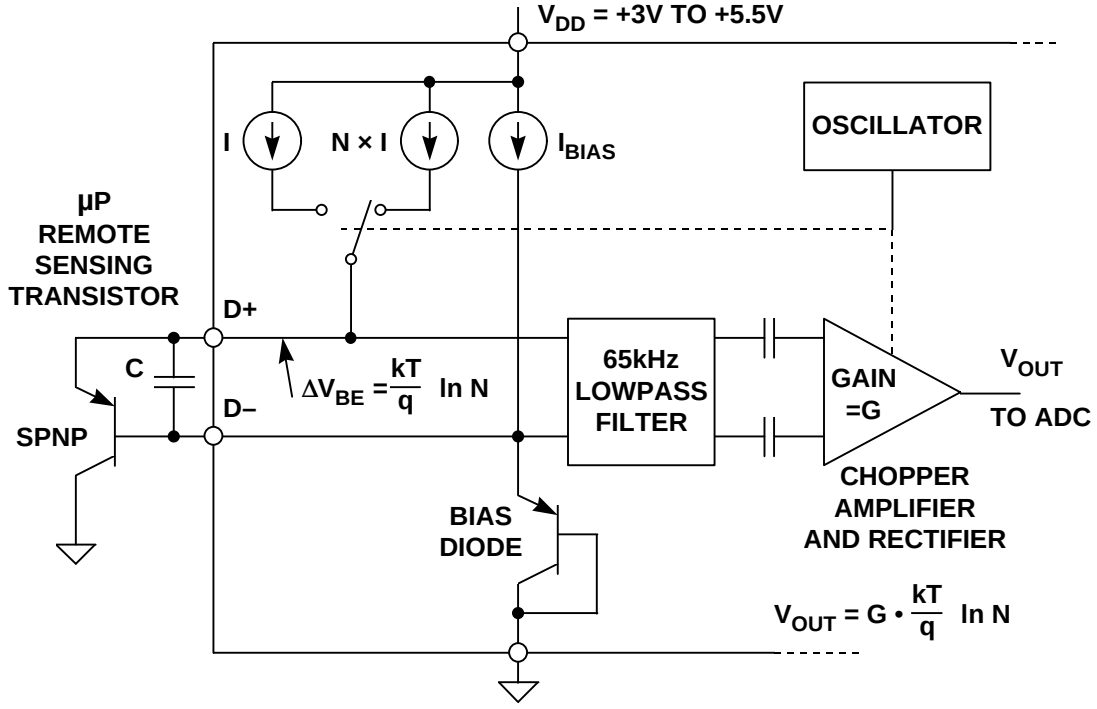


Figure 7.40

To measure ΔV_{BE}, the sensing transistor is switched between operating currents of I and N·I. The resulting waveform is passed through a 65kHz lowpass filter to remove noise, then to a chopper-stabilized amplifier which performs the function of amplification and synchronous rectification. The resulting DC voltage is proportional to ΔV_{BE} and is digitized by an 8-bit ADC. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

In addition, the ADM1021 contains an on-chip temperature sensor, and its signal conditioning and measurement is performed in the same manner.

One LSB of the ADC corresponds to 1ºC, so the ADC can theoretically measure from –128ºC to +127ºC, although the practical lowest value is limited to –65ºC due to device maximum ratings. The results of the local and remote temperature measurements are stored in the local and remote temperature value registers, and are compared with limits programmed into the local and remote high and low limit registers as shown in Figure 7.41. An $\overline{\text{ALERT}}$ output signals when the on-chip or remote temperature is out of range. This output can be used as an interrupt, or as an SMBus alert.

The limit registers can be programmed, and the device controlled and configured, via the serial System Management Bus (SMBus). The contents of any register can also be read back by the SMBus. Control and configuration functions consist of: switching the device between normal operation and standby mode, masking or enabling the $\overline{\text{ALERT}}$ output, and selecting the conversion rate which can be set from 0.0625Hz to 8Hz.

ADM1021 SIMPLIFIED BLOCK DIAGRAM

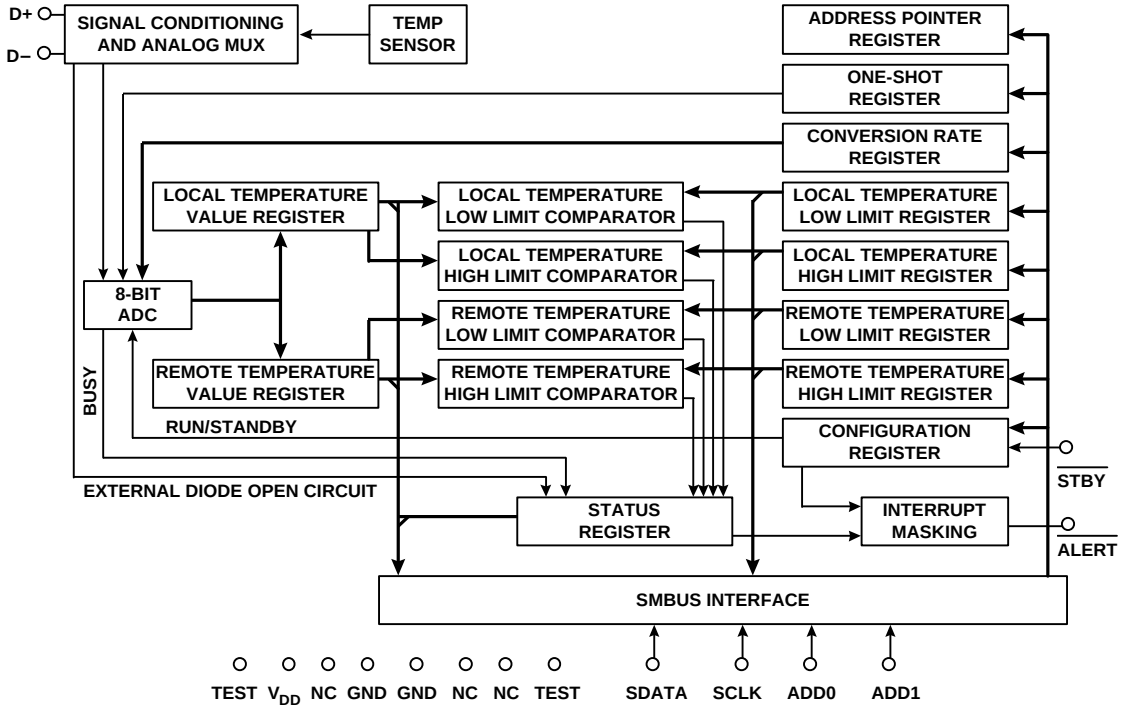


Figure 7.41

ADM1021 KEY SPECIFICATIONS

- On-Chip and Remote Temperature Sensing
- 1°C Accuracy for On-Chip Sensor
- 3°C Accuracy for Remote Sensor
- Programmable Over / Under Temperature Limits
- 2-Wire SMBus Serial Interface
- 70µA Max Operating Current
- 3µA Standby Current
- +3V to +5.5V Supplies
- 16-Pin QSOP Package

Figure 7.42

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SECTION 8

ADCs FOR SIGNAL CONDITIONING

Walt Kester, James Bryant, Joe Buxton

The trend in ADCs and DACs is toward higher speeds and higher resolutions at reduced power levels. Modern data converters generally operate on ±5V (dual supply) or +5V (single supply). In fact, many new converters operate on a single +3V supply. This trend has created a number of design and applications problems which were much less important in earlier data converters, where ±15V supplies and ±10V input ranges were the standard.

Lower supply voltages imply smaller input voltage ranges, and hence more susceptibility to noise from all potential sources: power supplies, references, digital signals, EMI/RFI, and probably most important, improper layout, grounding, and decoupling techniques. Single-supply ADCs often have an input range which is not referenced to ground. Finding compatible single-supply drive amplifiers and dealing with level shifting of the input signal in direct-coupled applications also becomes a challenge.

In spite of these issues, components are now available which allow extremely high resolutions at low supply voltages and low power. This section discusses the applications problems associated with such components and shows techniques for successfully designing them into systems.

The most popular precision signal conditioning ADCs are based on two fundamental architectures: *successive approximation* and *sigma-delta*. We have seen that the *tracking* ADC architecture is particularly suited for resolver-to-digital converters, but it is rarely used in other precision signal conditioning applications. The *flash* converter and the *subranging (or pipelined)* converter architectures are widely used where sampling frequencies extend into the megahertz and hundreds of megahertz region, but are overkill's in both speed and cost for low frequency precision signal conditioning applications.

LOW POWER, LOW VOLTAGE ADC DESIGN ISSUES

- **Typical Supply Voltages: ±5V, +5V, +5/+3V, +3V**
- **Lower Signal Swings Increase Sensitivity to**

  All Types of Noise (Device, Power Supply, Logic, etc.)
- **Device Noise Increases at Low Currents**
- **Common Mode Input Voltage Restrictions**
- **Input Buffer Amplifier Selection Critical**
- **Auto-Calibration Modes Desirable at High Resolutions**

Figure 8.1

ADCs FOR SIGNAL CONDITIONING

- **Successive Approximation**
  - **Resolutions to 16-bits**
  - **Minimal Throughput Delay Time**
  - **Used in Multiplexed Data Acquisition Systems**
- **Sigma-Delta**
  - **Resolutions to 24-bits**
  - **Excellent Differential Linearity**
  - **Internal Digital Filter, Excellent AC Line Rejection**
  - **Long Throughput Delay Time**
  - **Difficult to Multiplex Inputs Due to Digital Filter Settling Time**
- **High Speed Architectures:**
  - **Flash Converter**
  - **Subranging or Pipelined**

Figure 8.2

SUCCESSIVE APPROXIMATION ADCS

The successive approximation ADC has been the mainstay of signal conditioning for many years. Recent design improvements have extended the sampling frequency of these ADCs into the megahertz region. The use of internal switched capacitor techniques along with auto calibration techniques extend the resolution of these ADCs to 16-bits on standard CMOS processes without the need for expensive thin-film laser trimming.

The basic successive approximation ADC is shown in Figure 8.3. It performs conversions on command. On the assertion of the CONVERT START command, the sample-and-hold (SHA) is placed in the *hold* mode, and all the bits of the successive approximation register (SAR) are reset to "0" except the MSB which is set to "1". The SAR output drives the internal DAC. If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The next most significant bit is then set to "1". If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The process is repeated with each bit in turn. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the value of the analog input, and the conversion is complete.

The end of conversion is generally indicated by an end-of-convert (EOC), data-ready (DRDY), or a busy signal (actually, *not*-BUSY indicates end of conversion). The polarities and name of this signal may be different for different SAR ADCs, but the fundamental concept is the same. At the beginning of the conversion interval, the signal goes high (or low) and remains in that state until the conversion is completed,

at which time it goes low (or high). The trailing edge is generally an indication of valid output data.

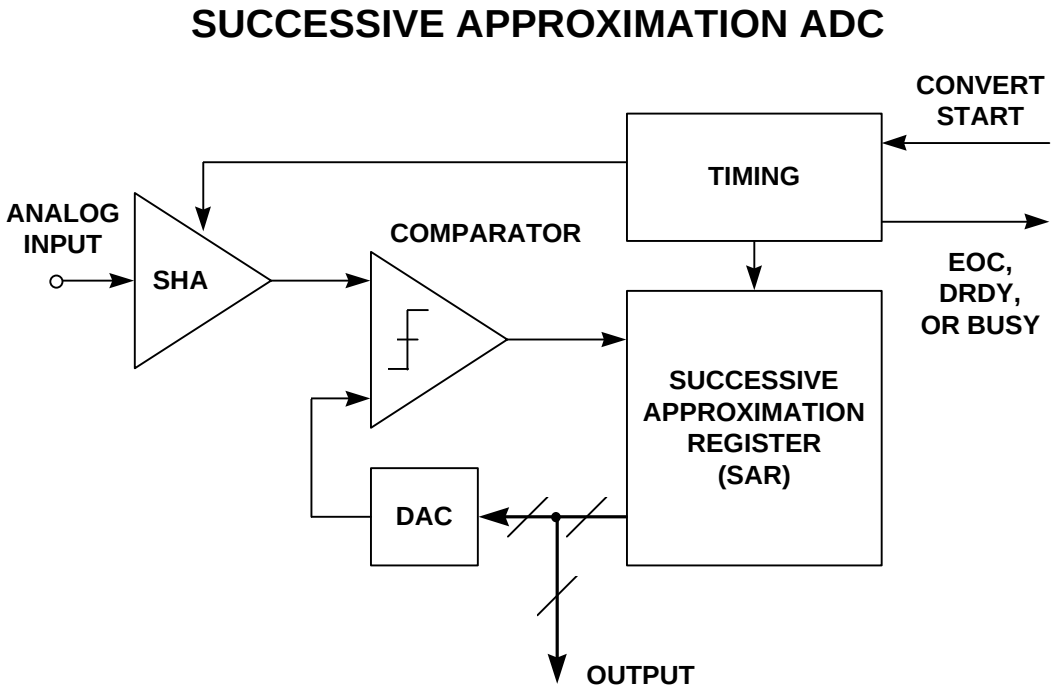


Figure 8.3

An N-bit conversion takes N steps. It would seem on superficial examination that a 16-bit converter would have twice the conversion time of an 8-bit one, but this is not the case. In an 8-bit converter, the DAC must settle to 8-bit accuracy before the bit decision is made, whereas in a 16-bit converter, it must settle to 16-bit accuracy, which takes a lot longer. In practice, 8-bit successive approximation ADCs can convert in a few hundred nanoseconds, while 16-bit ones will generally take several microseconds.

Notice that the overall accuracy and linearity of the SAR ADC is determined primarily by the internal DAC. Until recently, most precision SAR ADCs used laser-trimmed thin-film DACs to achieve the desired accuracy and linearity. The thin-film resistor trimming process adds cost, and the thin-film resistor values may be affected when subjected to the mechanical stresses of packaging.

For these reasons, switched capacitor (or charge-redistribution) DACs have become popular in newer SAR ADCs. The advantage of the switched capacitor DAC is that the accuracy and linearity is primarily determined by photolithography, which in turn controls the capacitor plate area and the capacitance as well as matching. In addition, small capacitors can be placed in parallel with the main capacitors which can be switched in and out under control of autocalibration routines to achieve high accuracy and linearity without the need for thin-film laser trimming. Temperature tracking between the switched capacitors can be better than 1ppm/ºC, thereby offering a high degree of temperature stability.

A simple 3-bit capacitor DAC is shown in Figure 8.4. The switches are shown in the *track*, or *sample* mode where the analog input voltage, A_{IN}, is constantly charging and discharging the parallel combination of all the capacitors. The *hold* mode is initiated by opening S_{IN}, leaving the sampled analog input voltage on the capacitor array. Switch S_C is then opened allowing the voltage at node A to move as the bit switches are manipulated. If S1, S2, S3, and S4 are all connected to ground, a voltage equal to $-A_{IN}$ appears at node A. Connecting S1 to V_{REF} adds a voltage equal to $V_{REF}/2$ to $-A_{IN}$. The comparator then makes the MSB bit decision, and the SAR either leaves S1 connected to V_{REF} or connects it to ground depending on the comparator output (which is high or low depending on whether the voltage at node A is negative or positive, respectively). A similar process is followed for the remaining two bits. At the end of the conversion interval, S1, S2, S3, S4, and S_{IN} are connected to A_{IN}, S_C is connected to ground, and the converter is ready for another cycle.

3-BIT SWITCHED CAPACITOR DAC

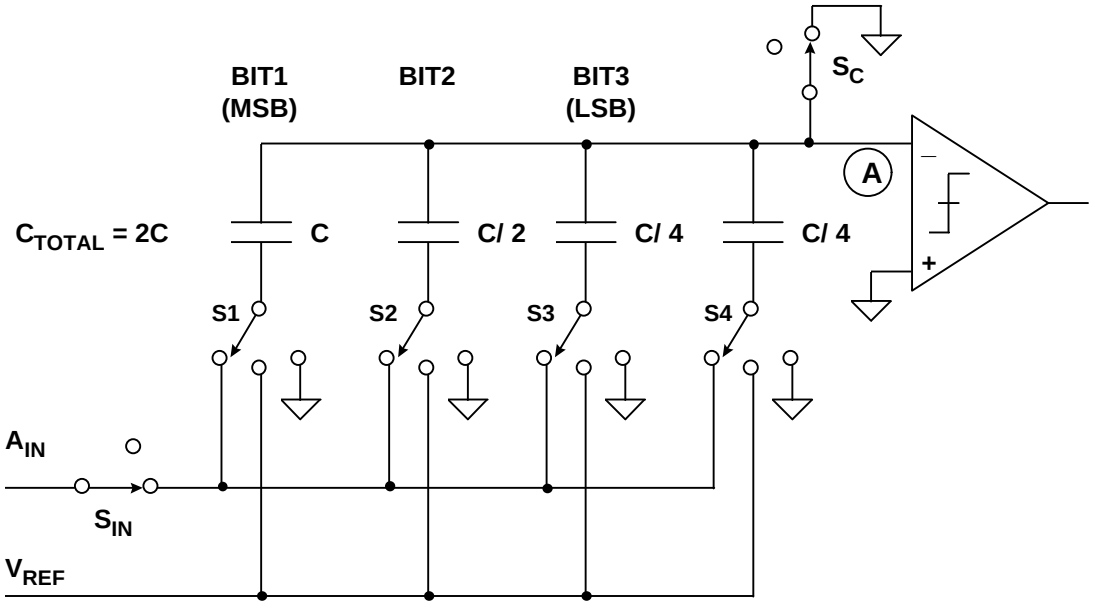


Figure 8.4

Note that the extra LSB capacitor (C/4 in the case of the 3-bit DAC) is required to make the total value of the capacitor array equal to 2C so that binary division is accomplished when the individual bit capacitors are manipulated.

The operation of the capacitor DAC (cap DAC) is similar to an R/2R resistive DAC. When a particular bit capacitor is switched to V_{REF}, the voltage divider created by the bit capacitor and the total array capacitance (2C) adds a voltage to node A equal to the weight of that bit. When the bit capacitor is switched to ground, the same voltage is subtracted from node A.

Because of their popularity, successive approximation ADCs are available in a wide variety of resolutions, sampling rates, input and output options, package styles, and costs. It would be impossible to attempt to list all types, but Figure 8.5 shows a number of recent Analog Devices' SAR ADCs which are representative. Note that many devices are complete data acquisition systems with input multiplexers which allow a single ADC core to process multiple analog channels.

RESOLUTION / CONVERSION TIME COMPARISON FOR REPRESENTATIVE SINGLE-SUPPLY SAR ADCs

	RESOLUTION	SAMPLING RATE	POWER	CHANNELS
AD7472	12-BITS	1.5MSPS	9mW	1
AD7891	12-BITS	500kSPS	85mW	8
AD7858/59	12-BITS	200kSPS	20mW	8
AD7887/88	12-BITS	125kSPS	3.5mW	8
AD7856/57	14-BITS	285kSPS	60mW	8
AD974	16-BITS	200kSPS	120mW	4
AD7670	16-BITS	1MSPS	250mW	1

Figure 8.5

While there are some variations, the fundamental timing of most SAR ADCs is similar and relatively straightforward (see Figure 8.6). The conversion process is initiated by asserting a CONVERT START signal. The $\overline{\text{CONVST}}$ signal is a negative-going pulse whose positive-going edge actually initiates the conversion. The internal sample-and-hold (SHA) amplifier is placed in the hold mode on this edge, and the various bits are determined using the SAR algorithm. The negative-going edge of the $\overline{\text{CONVST}}$ pulse causes the $\overline{\text{EOC}}$ or BUSY line to go high. When the conversion is complete, the BUSY line goes low, indicating the completion of the conversion process. In most cases the trailing edge of the BUSY line can be used as an indication that the output data is valid and can be used to strobe the output data into an external register. However, because of the many variations in terminology and design, the individual data sheet should always be consulted when using with a specific ADC.

It should also be noted that some SAR ADCs require an external high frequency clock in addition to the CONVERT START command. In most cases, there is no need to synchronize the two. The frequency of the external clock, if required, generally falls in the range of 1MHz to 30MHz depending on the conversion time and resolution of the ADC. Other SAR ADCs have an internal oscillator which is used to perform the conversions and only require the CONVERT START command. Because

of their architecture, SAR ADCs allow single-shot conversion at any repetition rate from DC to the converter's maximum conversion rate.

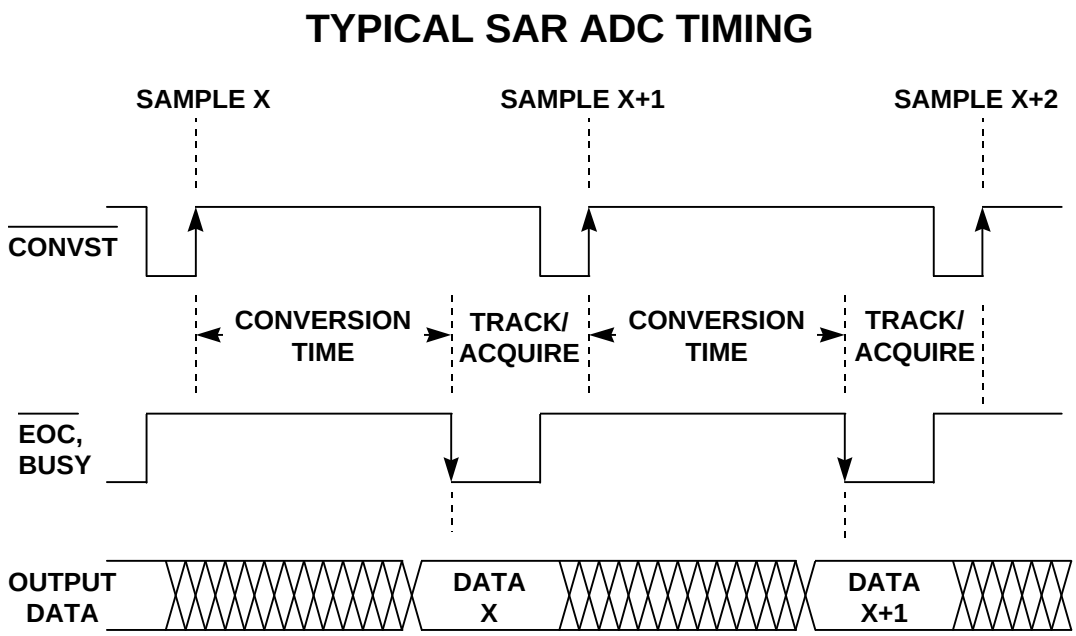


Figure 8.6

In a SAR ADC, the output data for a particular cycle is valid at the end of the conversion interval. In other ADC architectures, such as sigma-delta or the two-stage subranging architecture shown in Figure 8.7, this is not the case. The subranging ADC shown in the figure is a two-stage *pipelined* or subranging 12-bit converter. The first conversion is done by the 6-bit ADC which drives a 6-bit DAC. The output of the 6-bit DAC represents a 6-bit approximation to the analog input. Note that SHA2 delays the analog signal while the 6-bit ADC makes its decision and the 6-bit DAC settles. The DAC approximation is then subtracted from the analog signal from SHA2, amplified, and digitized by a 7-bit ADC. The outputs of the two conversions are combined, and the extra bit used to correct errors made in the first conversion. The typical timing associated with this type of converter is shown in Figure 8.8. Note that the output data presented immediately after sample X actually corresponds to sample X–2, i.e., there is a two clock-cycle "pipeline" delay. The pipelined ADC architecture is generally associated with high speed ADCs, and in most cases the pipeline delay, or *latency*, is not a major system problem in most applications where this type of converter is used.

Pipelined ADCs may have more than two clock-cycles latency depending on the particular architecture. For instance, the conversion could be done in three, or four, or perhaps even more pipelined stages causing additional latency in the output data.

Therefore, if the ADC is to be used in an event-triggered (or single-shot) mode where there must be a one-to-one time correspondence between each sample and the corresponding data, then the pipeline delay can be troublesome, and the SAR architecture is advantageous. Pipeline delay or latency can also be a problem in high speed servo-loop control systems or multiplexed applications. In addition, some

pipelined converters have a *minimum* allowable conversion rate and must be kept running to prevent saturation of internal nodes.

12-BIT TWO-STAGE PIPELINED ADC ARCHITECTURE

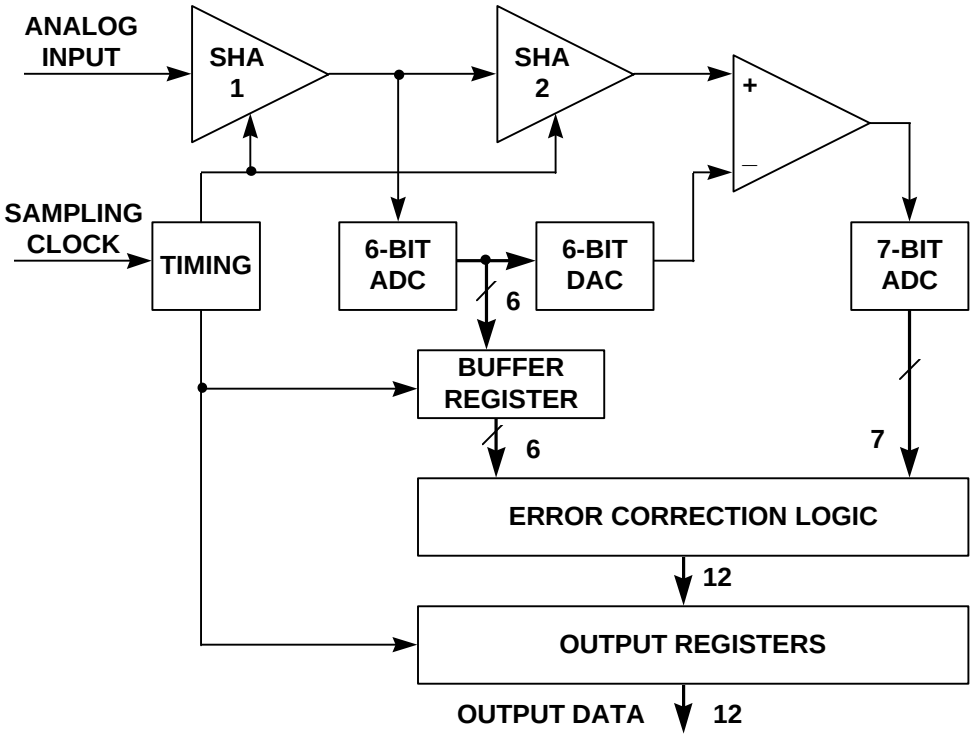
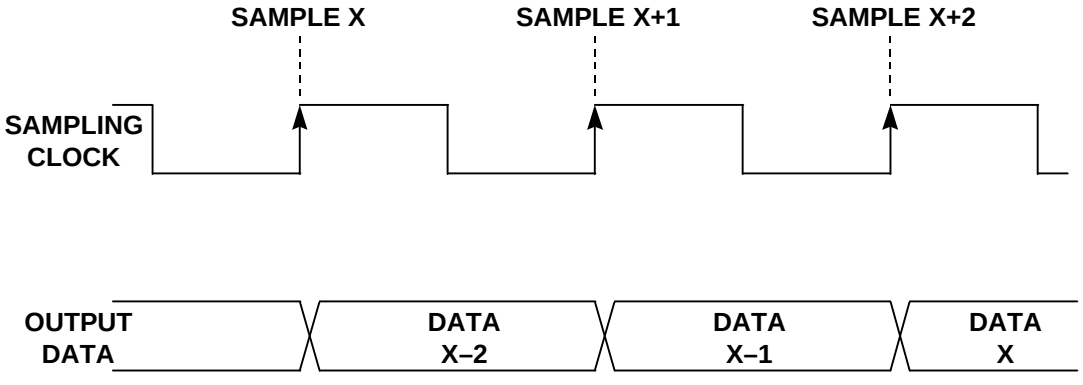


Figure 8.7

TYPICAL PIPELINED ADC TIMING



ABOVE SHOWS TWO CLOCK-CYCLES PIPELINE DELAY

Figure 8.8

Switched capacitor SAR ADCs generally have unbuffered input circuits similar to the circuit shown in Figure 8.9 for the AD7858/59 ADC. During the acquisition time, the analog input must charge the 20pF equivalent input capacitance to the correct value. If the input is a DC signal, then the source resistance, R_S, in series with the 125Ω internal switch resistance creates a time constant. In order to settle to 12-bit accuracy, approximately 9 time constants must be allowed for settling, and this defines the minimum allowable acquisition time. (Settling to 14-bits requires about 10 time constants, and 16-bits requires about 11).

$$t_{ACQ} > 9 \times (R_S + 125)\Omega \times 20pF.$$

For example, if R_S = 50Ω, the acquisition time per the above formula must be at least 310ns.

For AC applications, a low impedance source should be used to prevent distortion due to the non-linear ADC input circuit. In a single supply application, a fast settling rail-to-rail op amp such as the AD820 should be used. Fast settling allows the op amp to settle quickly from the transient currents induced on its input by the internal ADC switches. In Figure 8.9, the AD820 drives a lowpass filter consisting of the 50Ω series resistor and the 10nF capacitor (cutoff frequency approximately 320kHz). This filter removes high frequency components which could result in aliasing and increased noise.

Using a single supply op amp in this application requires special consideration of signal levels. The AD820 is connected in the inverting mode and has a signal gain of –1. The noninverting input is biased at a common mode voltage of +1.3V with the 10.7kΩ/10kΩ divider, resulting in an output voltage of +2.6V for V_{IN}= 0V, and +0.1V for V_{IN} = +2.5V. This offset is provided because the AD820 output cannot go all the way to ground, but is limited to the V_{CESAT} of the output stage NPN transistor, which under these loading conditions is about 50mV. The input range of the ADC is also offset by +100mV by applying the +100mV offset from the 412Ω/10kΩ divider to the AIN– input.

The AD789X-family of single supply SAR ADCs (as well as the AD974, AD976, and AD977) includes a thin film resistive attenuator and level shifter on the analog input to allow a variety of input range options, both bipolar and unipolar. A simplified diagram of the input circuit of the AD7890-10 12-bit, 8-channel ADC is shown in Figure 8.10. This arrangement allows the converter to digitize a ±10V input while operating on a single +5V supply. The R1/R2/R3 thin film network provides the attenuation and level shifting to convert the ±10V input to a 0V to +2.5V signal which is digitized by the internal ADC. This type of input requires no special drive circuitry because R1 isolates the input from the actual converter circuitry. Nevertheless, the source resistance, R_S, should be kept reasonably low to prevent gain errors caused by the R_S/R1 divider.

DRIVING SWITCHED CAPACITOR INPUTS OF AD7858/59 12-BIT, 200kSPS ADC

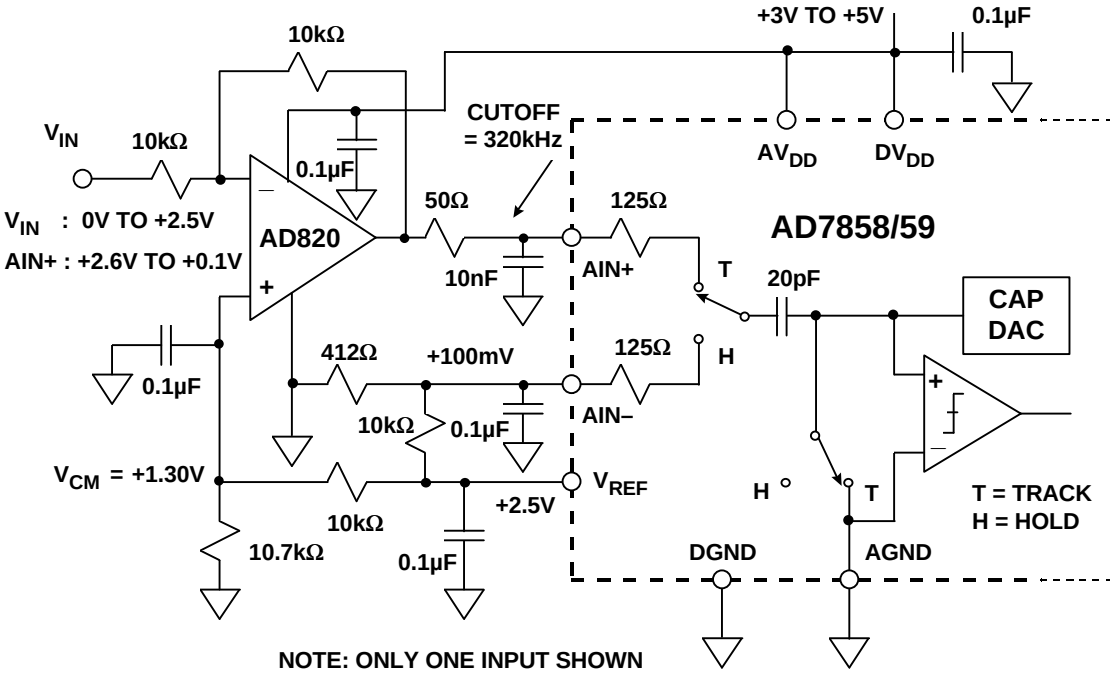


Figure 8.9

DRIVING SINGLE-SUPPLY ADCs WITH SCALED INPUTS

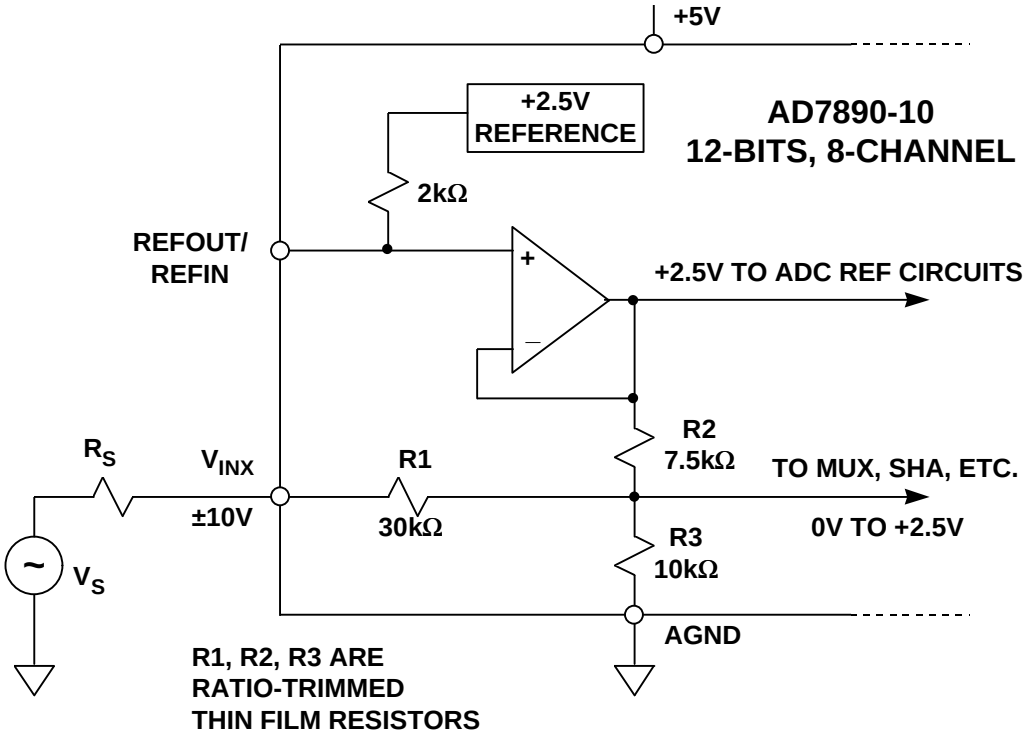


Figure 8.10

SAR ADCS WITH MULTIPLEXED INPUTS

Multiplexing is a fundamental part of many data acquisition systems, and a fundamental understanding of multiplexers is required to design a data acquisition system. Switches for data acquisition systems, especially when integrated into the IC, generally are CMOS-types shown in Figure 8.11. Utilizing the P-Channel and N-Channel MOSFET switches in parallel minimizes the change of on-resistance (R_{ON}) as a function of signal voltage. On-resistance can vary from less than 5Ω to several hundred ohms depending upon the device. Variation in on-resistance as a function of signal level (often called *R_{ON}-modulation*) can cause distortion if the multiplexer must drive a load, and therefore R_{ON} *flatness* is also an important specification.

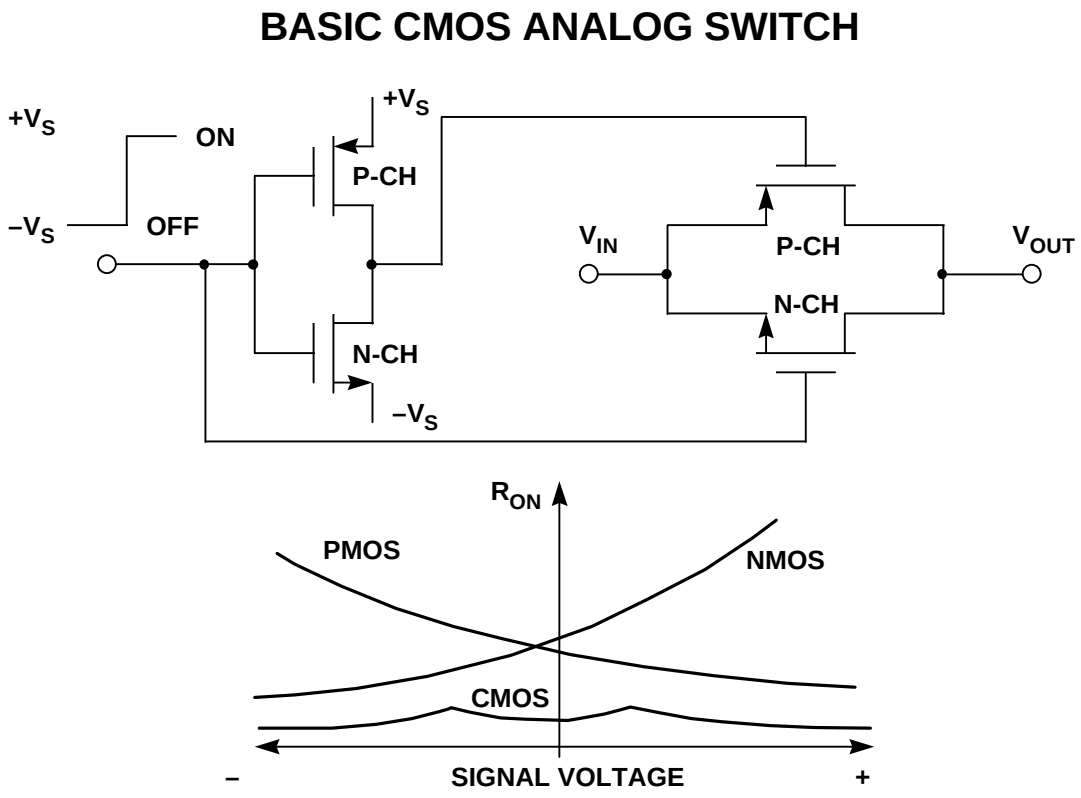


Figure 8.11

Because of non-zero R_{ON} and R_{ON}-modulation, multiplexer outputs should be isolated from the load with a suitable buffer amplifier. A separate buffer is not required if the multiplexer drives a high input impedance, such as a PGA, SHA or ADC - but beware! Some SHAs and ADCs draw high frequency pulse current at their sampling rate and cannot tolerate being driven by an unbuffered multiplexer.

The key multiplexer specifications are *switching time, on-resistance, on-resistance flatness,* and *off-channel isolation, and crosstalk*. Multiplexer switching time ranges from less than 20ns to over 1µs, R_{ON} from less than 5Ω to several hundred ohms, and off-channel isolation from 50 to 90dB.

A number of CMOS switches can be connected to form a multiplexer as shown in Figure 8.12. The number of input channels typically ranges from 4 to 16, and some multiplexers have internal channel-address decoding logic and registers, while with others, these functions must be performed externally. Unused multiplexer inputs *must* be grounded or severe loss of system accuracy may result.

Switches and multiplexers may be optimized for various applications as shown in Figure 8.13.

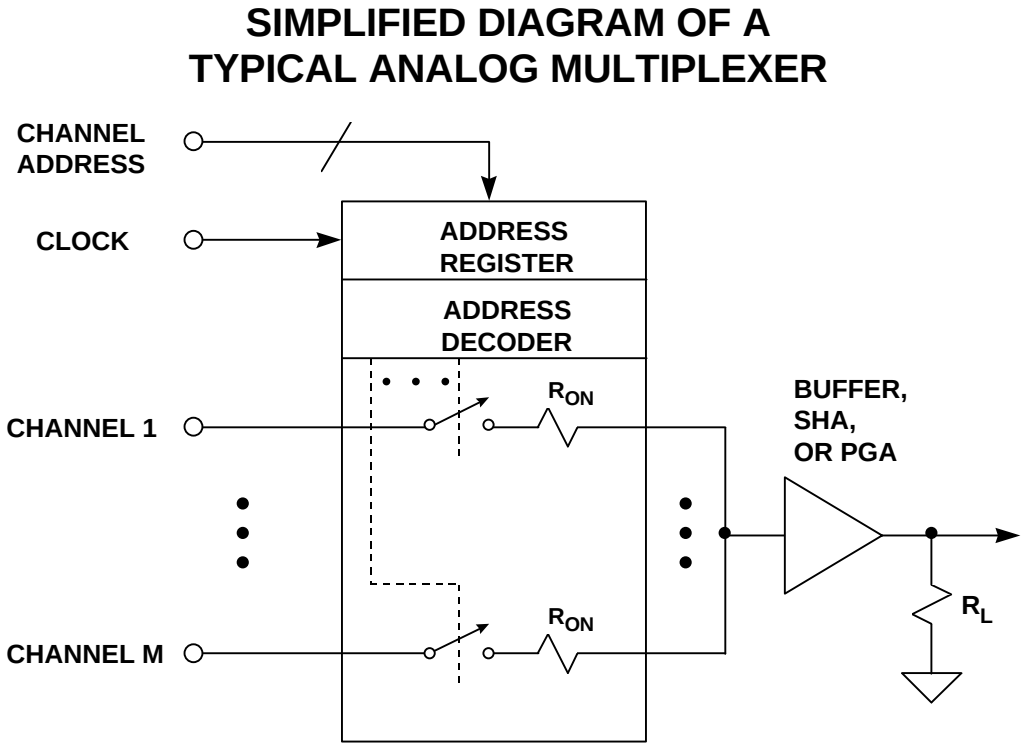


Figure 8.12

An M-channel multiplexed data acquisition system is shown in Figure 8.14. The typical timing associated with the SAR ADC is also shown in the diagram. The conversion process is initiated on the positive-going edge of the $\overline{\text{CONVST}}$ pulse. If maximum throughput is desired, the multiplexer is changed to the next channel at the same time. This allows nearly the entire sampling period ($1/f_S$) for the multiplexer to settle. Remember that it is possible to have a positive fullscale signal on one channel and a negative fullscale signal on the next, therefore the multiplexer output must settle from a fullscale output step change within the allocated time.

Also shown in Figure 8.14 are input filters on each channel. These filters serve as antialiasing filters to remove signals above one-half the effective per-channel sampling frequency. If the ADC is sampling at f_S, and the multiplexer is sequencing through all M channels, then the per-channel sampling rate is f_S/M. The input lowpass filters should have sufficient attenuation $f_S/2M$ to prevent dynamic range limitations due to aliasing.

WHAT'S NEW IN DISCRETE SWITCHES / MUXES?

- **ADG508F, ADG509F, ADG527F: ±15V Specified**
  - R_{ON} < 300Ω
  - Switching Time < 250ns
  - Fault Protection on Inputs and Outputs (–40V to + 55V)

- **ADG451, ADG452, ADG453: ±15V, +12V, ±5V Specified**
  - R_{ON} < 5Ω
  - Switching Time < 180ns
  - 2kV ESD Protection

- **ADG7XX-Family: Single-Supply, +1.8V to +5.5V**
  - R_{ON} < 5Ω, R_{ON} Flatness < 2Ω
  - Switching Time < 20ns

Figure 8.13

MULTIPLEXED SAR ADC FILTERING AND TIMING

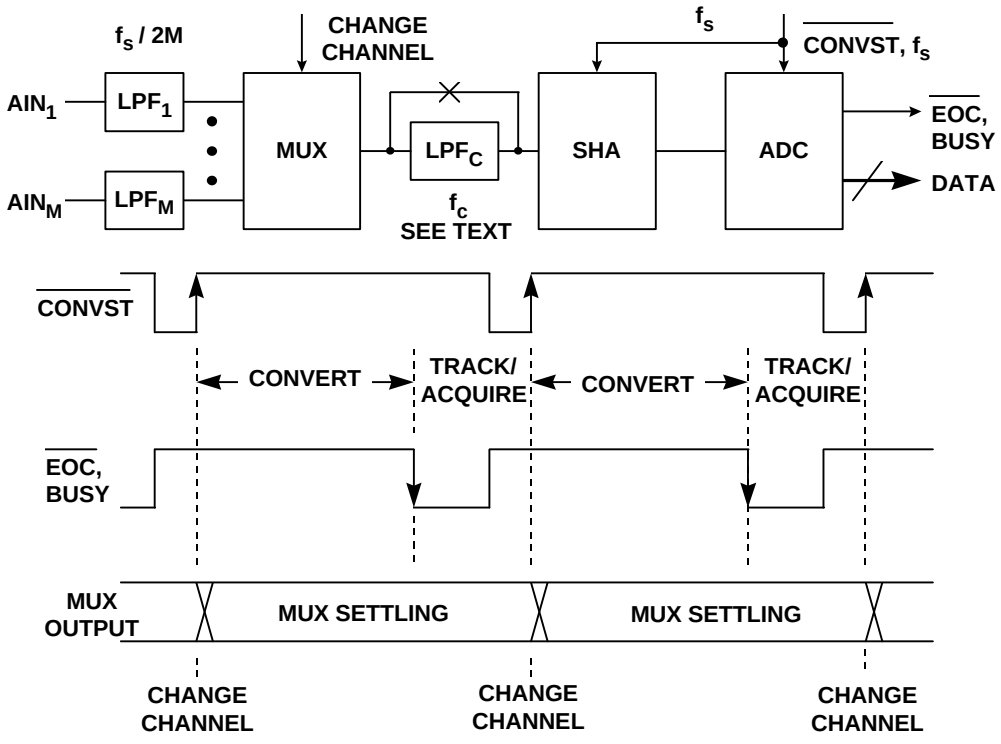


Figure 8.14

It is not necessary, however, that each channel be sampled at the same rate, and the various input lowpass filters can be individually tailored for the actual sampling rate and signal bandwidth expected on each channel.

An optional lowpass filter is often placed between the multiplexer output and the SHA input, designated LPF_C in Figure 8.14. Care must be exercised in selecting its cutoff frequency because its time constant directly affects the multiplexer settling time. If the filter is a single-pole, the number of time constants, n, required to settle to a desired accuracy is given in Figure 8.15.

SINGLE-POLE FILTER SETTLING TIME TO REQUIRED ACCURACY

RESOLUTION # OF BITS	LSB (%FS)	# OF TIME CONSTANTS, n	f_c/f_s
6	1.563	4.16	0.67
8	0.391	5.55	0.89
10	0.0977	6.93	1.11
12	0.0244	8.32	1.32
14	0.0061	9.70	1.55
16	0.00153	11.09	1.77
18	0.00038	12.48	2.00
20	0.000095	13.86	2.22
22	0.000024	15.25	2.44

f_S = ADC Sampling Frequency
f_C = Cutoff Frequency of LPF_C

Figure 8.15

If the time constant of LPF_C is τ, and its cutoff frequency f_c, then

$$f_C = \frac{1}{2\pi\tau}.$$

But the sampling frequency f_S is related to $n \cdot \tau$ by the equation:

$$f_S < \frac{1}{n \cdot \tau}.$$

Combining the two equations and solving for f_C in terms of n and f_S yields:

$$f_C > \frac{n \cdot f_S}{2\pi}.$$

As an example, assume that the ADC is a 12-bit one sampling at 100kSPS. From the table, n = 8.32, and therefore f_C > 132kSPS per the above equation. While this filter will help prevent wideband noise from entering the SHA, it does not provide the same function as the antialiasing filters at the input of each channel, whose individual cutoff frequencies can be much lower.

For this reason, only a few integrated data acquisition ICs with on-board multiplexers give access to the multiplexer output and the SHA input. If access is offered and LPF_C is used, the settling time requirement must be observed in order to achieve the desired accuracy.

COMPLETE DATA ACQUISITION SYSTEMS ON A CHIP

VLSI mixed-signal processing allows the integration of large and complex data acquisition circuits on a single chip. Most signal conditioning circuits including multiplexers, PGAs, and SHAs, can now be manufactured on the same chip as the ADC. This high level of integration permits data acquisition systems (DASs) to be specified and tested as a single complex function.

Such functionality relieves the designer of most of the burden of testing and calculating error budgets. The DC and AC characteristics of a complete data acquisition system are specified as a complete function, which removes the necessity of calculating performance from a collection of individual worst case device specifications. A complete monolithic system should achieve a higher performance at much lower cost than would be possible with a system built up from discrete functions. Furthermore, system calibration is easier, and in fact many monolithic DASs are self calibrating, offering both internal and system calibration functions.

The AD7858 is an example of a highly integrated IC DAS (see Figure 8.16). The device operates on a single supply voltage of +3V to +5.5V and dissipates only 15mW. The resolution is 12-bits, and the maximum sampling frequency is 200kSPS. The input multiplexer can be configured either as 8 single-ended inputs or 4 pseudo-differential inputs. The AD7858 requires an external 4MHz clock and initiates the conversion on the positive-going edge of the $\overline{\text{CONVST}}$ pulse which does not need to be synchronized to the high frequency clock. Conversion can also be initiated via software by setting a bit in the proper control register.

The AD7858 contains an on-chip 2.5V reference (which can be overridden with an external one), and the fullscale input voltage range is 0V to V_{REF}. The internal DAC is a switched capacitor type, and the ADC contains a self-calibration and system calibration option to ensure accurate operation over time and temperature. The input/output port is a serial one and is SPI, QSPI, 8051, and µP compatible.

The AD7858L is a lower power (5.5mW) version of the AD7858 which operates at a maximum sampling rate of 100kSPS.

AD7858 12-BIT, 200kSPS 8-CHANNEL SINGLE-SUPPLY ADC

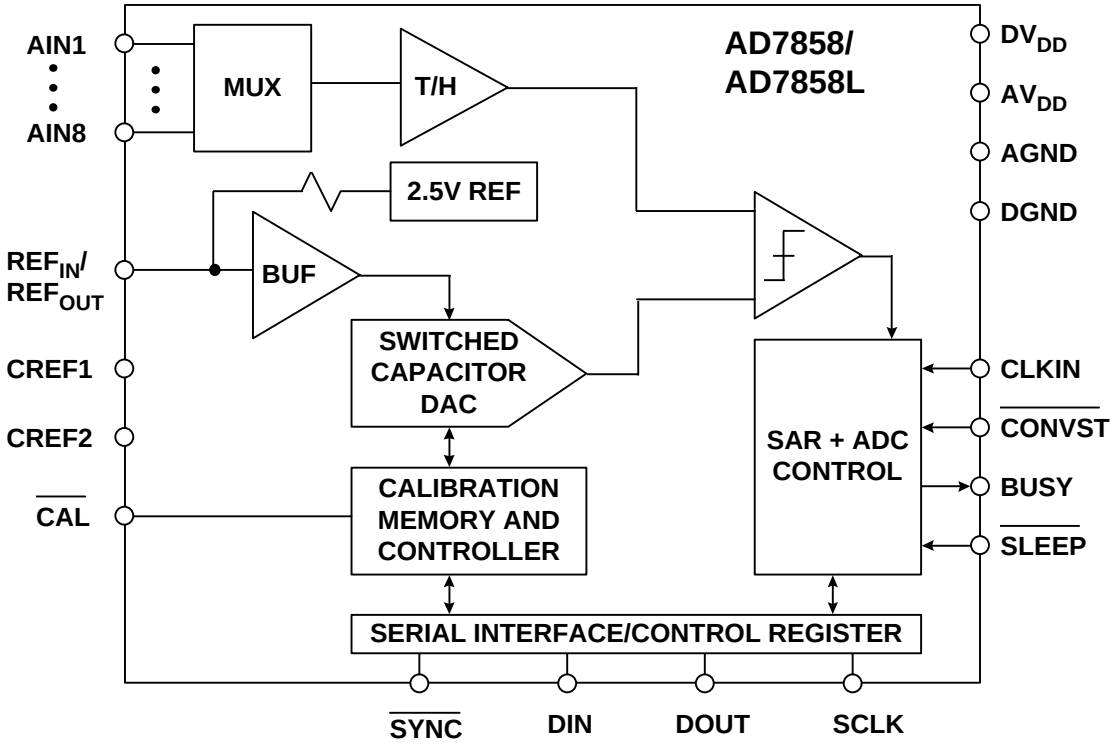


Figure 8.16

AD7858 / AD7858L DATA ACQUISITION ADCs KEY SPECIFICATIONS

- 12-Bit, 8Channel, 200kSPS (AD7858), 100kSPS (AD7858L)
- System and Self-Calibration with Autocalibration on Power-Up
- Automatic Power Down After Conversion (25µW)
- Low Power:
  - AD7858: 15mW (V_{DD} = +3V)
  - AD7858L: 5.5mW (V_{DD} = +3V)
- Flexible Serial Interface: 8051 / SPI / QSPI / µP Compatible
- 24-Pin DIP, SOIC, SSOP Packages
- AD7859, AD7859L: Parallel Output Devices, Similar Specifications

Figure 8.17

SIGMA-DELTA (ΣΔ) MEASUREMENT ADCS

James M. Bryant

Sigma-Delta Analog-Digital Converters (ΣΔ ADCs) have been known for nearly thirty years, but only recently has the technology (high-density digital VLSI) existed to manufacture them as inexpensive monolithic integrated circuits. They are now used in many applications where a low-cost, low-bandwidth, low-power, high-resolution ADC is required.

There have been innumerable descriptions of the architecture and theory of ΣΔ ADCs, but most commence with a maze of integrals and deteriorate from there. In the Applications Department at Analog Devices, we frequently encounter engineers who do not understand the theory of operation of ΣΔ ADCs and are convinced, from study of a typical published article, that it is too complex to comprehend easily.

There is nothing particularly difficult to understand about ΣΔ ADCs, as long as you avoid the detailed mathematics, and this section has been written in an attempt to clarify the subject. A ΣΔ ADC contains very simple analog electronics (a comparator, a switch, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. This circuitry consists of a digital signal processor (DSP) which acts as a filter (generally, but not invariably, a low pass filter). It is not necessary to know precisely how the filter works to appreciate what it does. To understand how a ΣΔ ADC works familiarity with the concepts of *over-sampling, quantization noise shaping, digital filtering,* and *decimation* is required.

SIGMA-DELTA ADCs

- **Low Cost, High Resolution (to 24-bits) Excellent DNL,**
- **Low Power, but Limited Bandwidth**
- **Key Concepts are Simple, but Math is Complex**
  - **Oversampling**
  - **Quantization Noise Shaping**
  - **Digital Filtering**
  - **Decimation**
- **Ideal for Sensor Signal Conditioning**
  - **High Resolution**
  - **Self, System, and Auto Calibration Modes**

Figure 8.18

Let us consider the technique of over-sampling with an analysis in the frequency domain. Where a DC conversion has a *quantization error* of up to ½ LSB, a sampled data system has *quantization noise.* A perfect classical N-bit sampling ADC has an RMS quantization noise of $q/\sqrt{12}$ uniformly distributed within the Nyquist band of DC to $f_S/2$ (where q is the value of an LSB and f_S is the sampling rate) as shown in Figure 8.19A. Therefore, its SNR with a full-scale sinewave input will be (6.02N + 1.76) dB. If the ADC is less than perfect, and its noise is greater than its theoretical minimum quantization noise, then its *effective* resolution will be less than N-bits. Its actual resolution (often known as its Effective Number of Bits or ENOB) will be defined by

$$\text{ENOB} = \frac{\text{SNR} - 1.76\text{dB}}{6.02\text{dB}}.$$

If we choose a much higher sampling rate, Kf_S (see Figure 8.19B), the quantization noise is distributed over a wider bandwidth DC to $Kf_S/2$. If we then apply a digital low pass filter (LPF) to the output, we remove much of the quantization noise, but do not affect the wanted signal - so the ENOB is improved. We have accomplished a high resolution A/D conversion with a low resolution ADC. The factor K is generally referred to as the *oversampling ratio.*

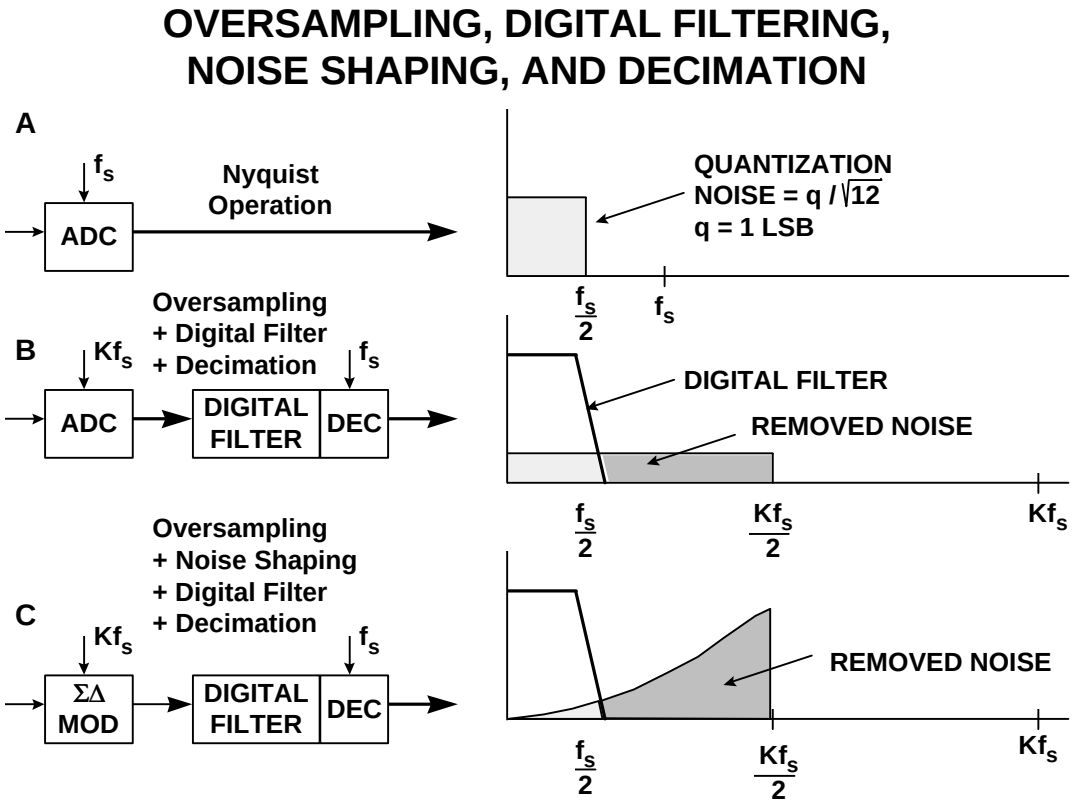


Figure 8.19

Since the bandwidth is reduced by the digital output filter, the output data rate may be lower than the original sampling rate (Kf_S) and still satisfy the Nyquist criterion. This may be achieved by passing every Mth result to the output and discarding the remainder. The process is known as "decimation" by a factor of M. Despite the origins of the term (*decem* is Latin for ten), M can have any integer value, provided that the output data rate is more than twice the signal bandwidth. Decimation does not cause any loss of information (see Figure 8.19B).

If we simply use over-sampling to improve resolution, we must over-sample by a factor of 2^{2N} to obtain an N-bit increase in resolution. The ΣΔ converter does not need such a high over-sampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband as shown in Figure 8.19C.

If we take a 1-bit ADC (generally known as a comparator), drive it with the output of an integrator, and feed the integrator with an input signal summed with the output of a 1-bit DAC fed from the ADC output, we have a first-order ΣΔ modulator as shown in Figure 8.20. Add a digital low pass filter (LPF) and decimator at the digital output, and we have a ΣΔ ADC: the ΣΔ modulator shapes the quantization noise so that it lies above the passband of the digital output filter, and the ENOB is therefore much larger than would otherwise be expected from the over-sampling ratio.

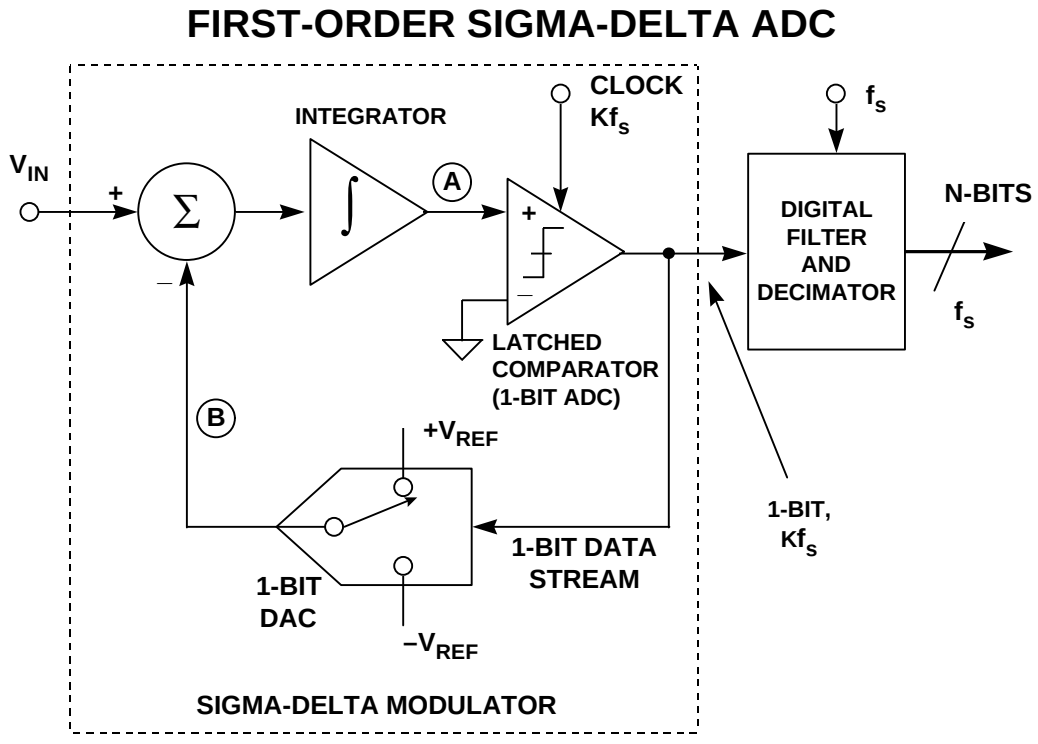
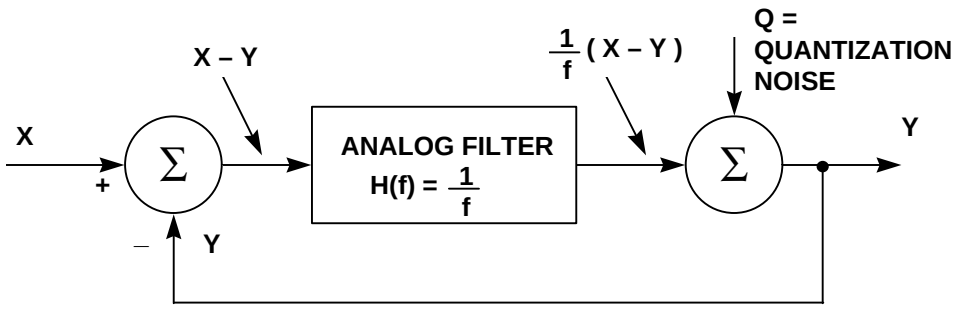


Figure 8.20

Intuitively, a ΣΔ ADC operates as follows. Assume a DC input at V_{IN}. The integrator is constantly ramping up or down at node A. The output of the comparator is fed back through a 1-bit DAC to the summing input at node B. The negative feedback loop from the comparator output through the 1-bit DAC back to the summing point will force the average DC voltage at node B to be equal to V_{IN}. This implies that the average DAC output voltage must equal to the input voltage V_{IN}. The average DAC output voltage is controlled by the *ones-density* in the 1-bit data stream from the comparator output. As the input signal increases towards $+V_{REF}$, the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. Similarly, as the signal goes negative towards $-V_{REF}$, the number of "ones" in the serial bit stream decreases, and the number of "zeros" increases. From a very simplistic standpoint, this analysis shows that the average value of the input voltage is contained in the serial bit stream out of the comparator. The digital filter and decimator process the serial bit stream and produce the final output data.

The concept of noise shaping is best explained in the frequency domain by considering the simple ΣΔ modulator model in Figure 8.21.

SIMPLIFIED FREQUENCY DOMAIN LINEARIZED MODEL OF A SIGMA-DELTA MODULATOR



$$Y = \frac{1}{f}(X - Y) + Q$$

REARRANGING, SOLVING FOR Y:

$$Y = \frac{X}{f+1} + \frac{Q\,f}{f+1}$$

SIGNAL TERM NOISE TERM

Figure 8.21

The integrator in the modulator is represented as an analog lowpass filter with a transfer function equal to H(f) = 1/f. This transfer function has an amplitude response which is inversely proportional to the input frequency. The 1-bit quantizer generates quantization noise, Q, which is injected into the output summing block. If we let the input signal be X, and the output Y, the signal coming out of the input summer must be X – Y. This is multiplied by the filter transfer function, 1/f, and the result goes to one input to the output summer. By inspection, we can then write the expression for the output voltage Y as:

$$Y = \frac{1}{f}(X - Y) + Q.$$

This expression can easily be rearranged and solved for Y in terms of X, f, and Q:

$$Y = \frac{X}{f+1} + \frac{Q \cdot f}{f+1}.$$

Note that as the frequency f approaches zero, the output voltage Y approaches X with no noise component. At higher frequencies, the amplitude of the signal component decreases, and the noise component increases. At high frequency, the output consists primarily of quantization noise. In essence, the analog filter has a lowpass effect on the signal, and a highpass effect on the quantization noise. Thus the analog filter performs the noise shaping function in the ΣΔ modulator model.

For a given input frequency, higher order analog filters offer more attenuation. The same is true of ΣΔ modulators, provided certain precautions are taken.

By using more than one integration and summing stage in the ΣΔ modulator, we can achieve higher orders of quantization noise shaping and even better ENOB for a given over-sampling ratio as is shown in Figure 8.22 for both a first and second-order ΣΔ modulator. The block diagram for the second-order ΣΔ modulator is shown in Figure 8.23. Third, and higher, order ΣΔ ADCs were once thought to be potentially unstable at some values of input - recent analyses using *finite* rather than infinite gains in the comparator have shown that this is not necessarily so, but even if instability does start to occur, it is not important, since the DSP in the digital filter and decimator can be made to recognize incipient instability and react to prevent it.

Figure 8.24 shows the relationship between the order of the ΣΔ modulator and the amount of over-sampling necessary to achieve a particular SNR. For instance, if the oversampling ratio is 64, an ideal second-order system is capable of providing an SNR of about 80dB. This implies approximately 13 effective number of bits (ENOB). Although the filtering done by the digital filter and decimator can be done to any degree of precision desirable, it would be pointless to carry more than 13 binary bits to the outside world. Additional bits would carry no useful signal information, and would be buried in the quantization noise unless post-filtering techniques were employed.

SIGMA-DELTA MODULATORS SHAPE QUANTIZATION NOISE

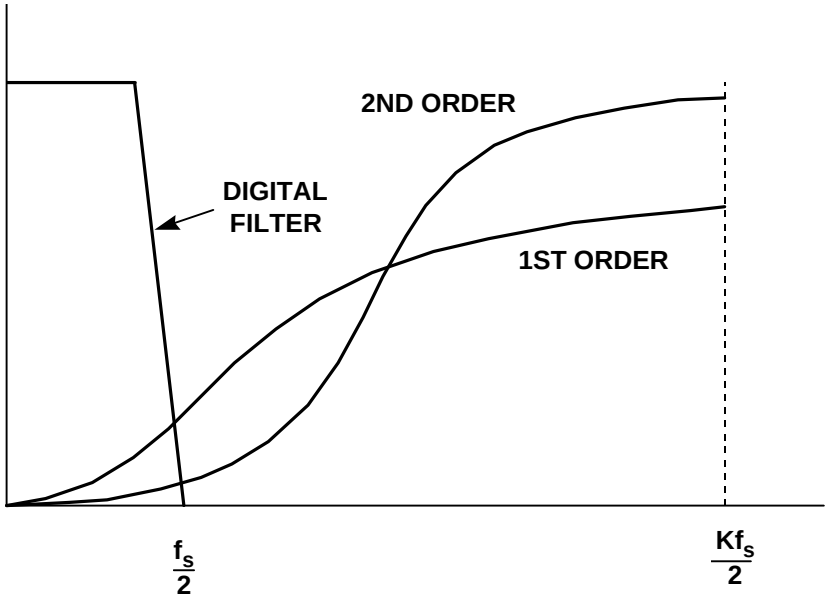


Figure 8.22

SECOND-ORDER SIGMA-DELTA ADC

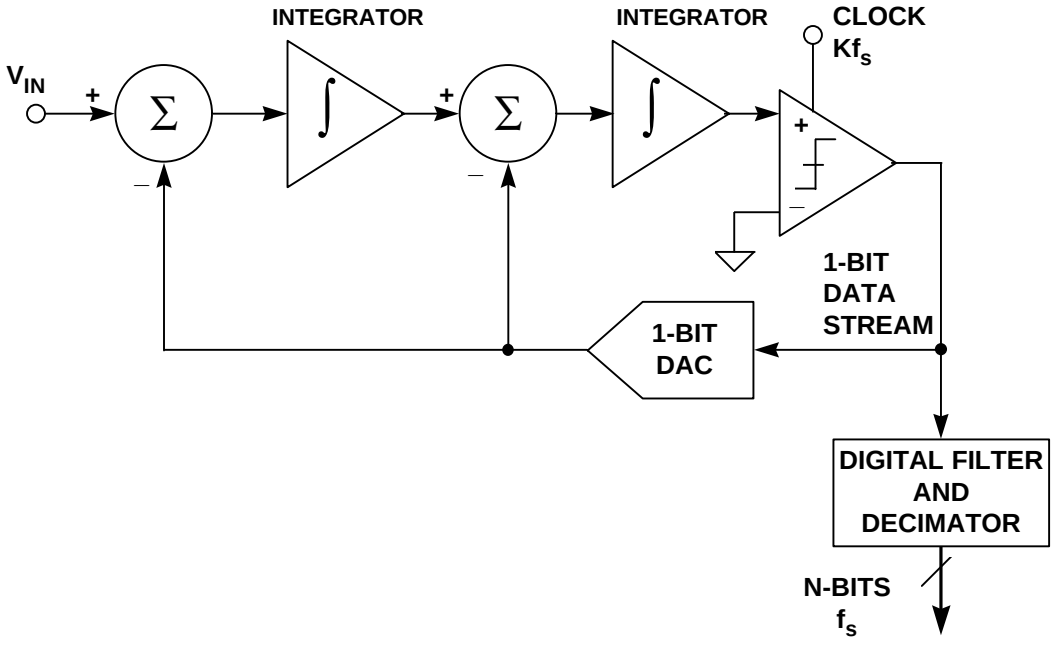


Figure 8.23

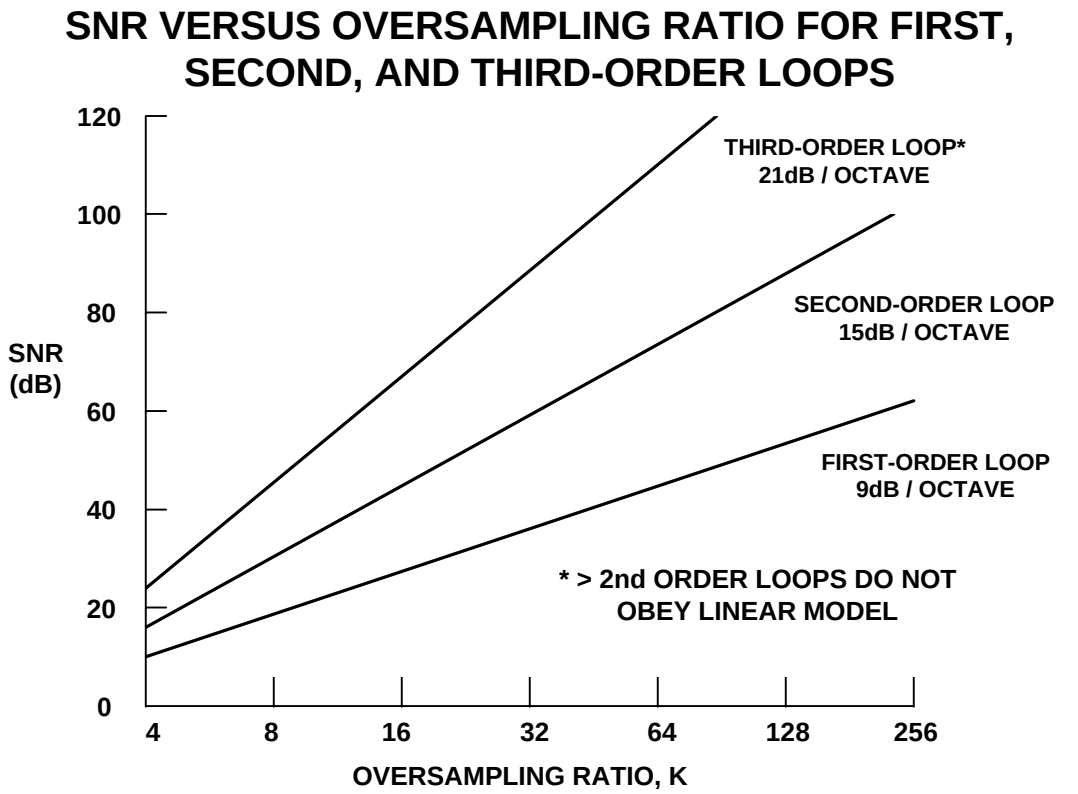


Figure 8.24

The ΣΔ ADCs that we have described so far contain integrators, which are low pass filters, whose passband extends from DC. Thus, their quantization noise is pushed up in frequency. At present, most commercially available ΣΔ ADCs are of this type (although some which are intended for use in audio or telecommunications applications contain bandpass rather than lowpass digital filters to eliminate any system DC offsets). Sigma-delta ADCs are available with resolutions up to 24-bits for DC measurement applications (AD77XX-family), and with resolutions of 18-bits for high quality digital audio applications (AD1879).

But there is no particular reason why the filters of the ΣΔ modulator should be LPFs, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than bandpass filters. If we replace the integrators in a ΣΔ ADC with bandpass filters (BPFs), the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the pass-band (see Reference 1). If the digital filter is then programmed to have its pass-band in this region, we have a ΣΔ ADC with a bandpass, rather than a lowpass characteristic. Although studies of this architecture are in their infancy, such ADCs would seem to be ideally suited for use in digital radio receivers, medical ultrasound, and a number of other applications.

A ΣΔ ADC works by over-sampling, where simple analog filters in the ΣΔ modulator shape the quantization noise so that the SNR *in the bandwidth of interest* is much greater than would otherwise be the case, and by using high performance digital filters and decimation to eliminate noise outside the required passband. Because the analog circuitry is so simple and undemanding, it may be built with the same digital

VLSI process that is used to fabricate the DSP circuitry of the digital filter. Because the basic ADC is 1-bit (a comparator), the technique is inherently linear.

Although the detailed analysis of ΣΔ ADCs involves quite complex mathematics, their basic design can be understood without the necessity of any mathematics at all. For further discussion on ΣΔ ADCs, refer to References 2 and 3.

HIGH RESOLUTION, LOW-FREQUENCY SIGMA-DELTA MEASUREMENT ADCS

The AD7710, AD7711, AD7712, AD7713, and AD7714, AD7730, and AD7731 are members of a family of sigma-delta converters designed for high accuracy, low frequency measurements. They have no missing codes to 24-bits, and their effective resolutions extend to 22.5 bits depending upon the device, update rate, programmed filter bandwidth, PGA gain, post-filtering, etc. They all use similar sigma-delta cores, and their main differences are in their analog inputs, which are optimized for different transducers. Newer members of the family, such as the AD7714, AD7730/7730L, and the AD7731/7731L are designed and specified for single supply operation.

There are also similar 16-bit devices available (AD7705, AD7706, AD7715) which also operate on single supplies.

The AD1555/AD1556 is a 24-bit two-chip ΣΔ modulator/filter specifically designed for seismic data acquisition systems. This combination yields a dynamic range of 120dB. The AD1555 contains a PGA and a 4th-order ΣΔ modulator. The AD1555 outputs a serial 1-bit data stream to the AD1556 which contains the digital filter and decimator.

Because of the high resolution of these converters, the effects of noise must be fully understood and how it affects the ADC performance. This discussion also applies to ADCs of lower resolution, but is particularly important when dealing with 16-bit or greater ΣΔ ADCs.

Figure 8.25 shows the output code distribution, or histogram, for a typical high resolution ADC with a DC, or "grounded" input centered on a code. If there were no noise sources present, the ADC output would always yield the same code, regardless of how many samples were taken. Of course, if the DC input happened to be in a transition zone between two adjacent codes, then the distribution would be spread between these two codes, but no further. Various noise sources internal to the converter, however, cause a distribution of codes around a primary one as shown in the diagram.

This noise in the ADC is generated by unwanted signal coupling and by components such as resistors (Johnson noise) and active devices like switches (kT/C noise). In addition, there is residual quantization noise which is not removed by the digital filter. The total noise can be considered to be an input noise source which is summed with the input signal into an ideal noiseless ADC. It is sometimes called *input-referred noise*, or *effective input noise*. The distribution of the noise is primarily

gaussian, and therefore an RMS noise value can be determined (i.e., the standard deviation of the distribution).

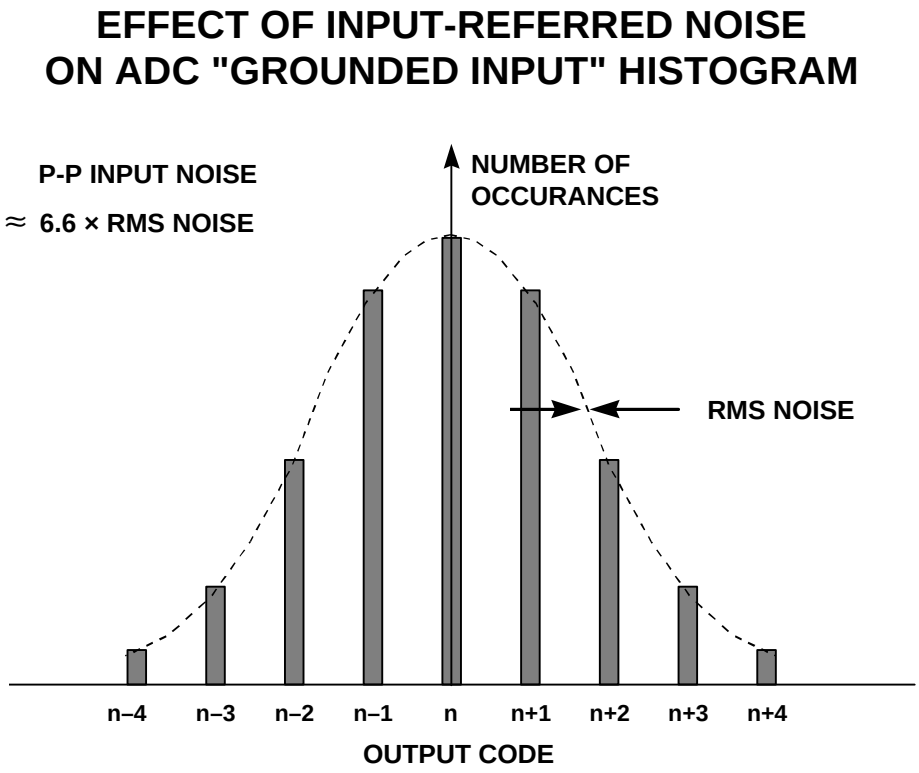


Figure 8.25

In order to characterize the input-referred noise, we introduce the concept of *Effective Resolution*, sometimes referred to as effective number of bits (ENOB). It should be noted, however, that ENOB is most often used to describe the dynamic performance of higher speed ADCs with AC input signals, and is not often used with respect to precision low frequency ΣΔ ADCs.

Effective Resolution is defined by the following equation:

$$\text{Effective Resolution} = \log_2\left[\frac{\text{Fullscale Range}}{\text{RMS Noise}}\right] \text{Bits}\,.$$

Noise-Free Code Resolution is defined by:

$$\text{Noise Free Code Resolution} = \log_2\left[\frac{\text{Fullscale Range}}{\text{Peak to Peak Noise}}\right] \text{Bits}\,.$$

Peak-to-peak noise is approximately 6.6 times the RMS noise, so Noise-Free Code Resolution can be expressed as:

$$\begin{aligned}\text{Noise Free Code Resolution} &= \log_2\left[\frac{\text{Fullscale Range}}{6.6 \times \text{RMS Noise}}\right] \text{Bits} \\ &= \text{Effective Resolution} - 2.72 \text{ Bits}\end{aligned}\quad .$$

Noise Free Code Resolution is therefore the maximum number of ADC bits that can be used and still always get a single-code output distribution for a DC input placed on a code center, i.e., there is no *code flicker*. This does not say that the rest of the LSBs are unusable, it is only a way to define the noise amplitude and relate it to ADC resolution. It should also be noted that additional external post-filtering and averaging of the ADC output data can further reduce input referred noise and increase the effective resolution.

DEFINITION OF "NOISE-FREE" CODE RESOLUTION

$$\text{EFFECTIVE RESOLUTION} = \log_2\left[\frac{\text{FULLSCALE RANGE}}{\text{RMS NOISE}}\right] \text{ BITS}$$

$$\text{NOISE-FREE CODE RESOLUTION} = \log_2\left[\frac{\text{FULLSCALE RANGE}}{\text{P-P NOISE}}\right] \text{ BITS}$$

$$\text{P-P NOISE} = 6.6 \times \text{RMS NOISE}$$

$$\text{NOISE-FREE CODE RESOLUTION} = \log_2\left[\frac{\text{FULLSCALE RANGE}}{6.6 \times \text{RMS NOISE}}\right] \text{ BITS}$$

$$= \text{EFFECTIVE RESOLUTION} - 2.72 \text{ BITS}$$

Figure 8.26

The AD7730 is one of the newest members of the AD77XX family and is shown in Figure 8.27. This ADC was specifically designed to interface directly to bridge outputs in weigh scale applications. The device accepts low-level signals directly from a bridge and outputs a serial digital word. There are two buffered differential inputs which are multiplexed, buffered, and drive a PGA. The PGA can be programmed for four differential unipolar analog input ranges: 0V to +10mV, 0V to +20mV, 0V to +40mV, and 0V to +80mV and four differential bipolar input ranges: ±10mV, ±20mV, ±40mV, and ±80mV. The maximum peak-to-peak, or noise-free resolution achievable is 1 in 230,000 counts, or approximately 18-bits. It should be noted that the noise-free resolution is a function of input voltage range, filter cutoff, and output word rate. Noise is greater using the smaller input ranges where the PGA gain must be increased. Higher output word rates and associated higher filter cutoff frequencies will also increase the noise.

The analog inputs are buffered on-chip allowing relatively high source impedances. Both analog channels are differential, with a common mode voltage range that comes within 1.2V of AGND and 0.95V of AVDD. The reference input is also differential, and the common mode range is from AGND to AVDD.

AD7730 SINGLE-SUPPLY BRIDGE ADC

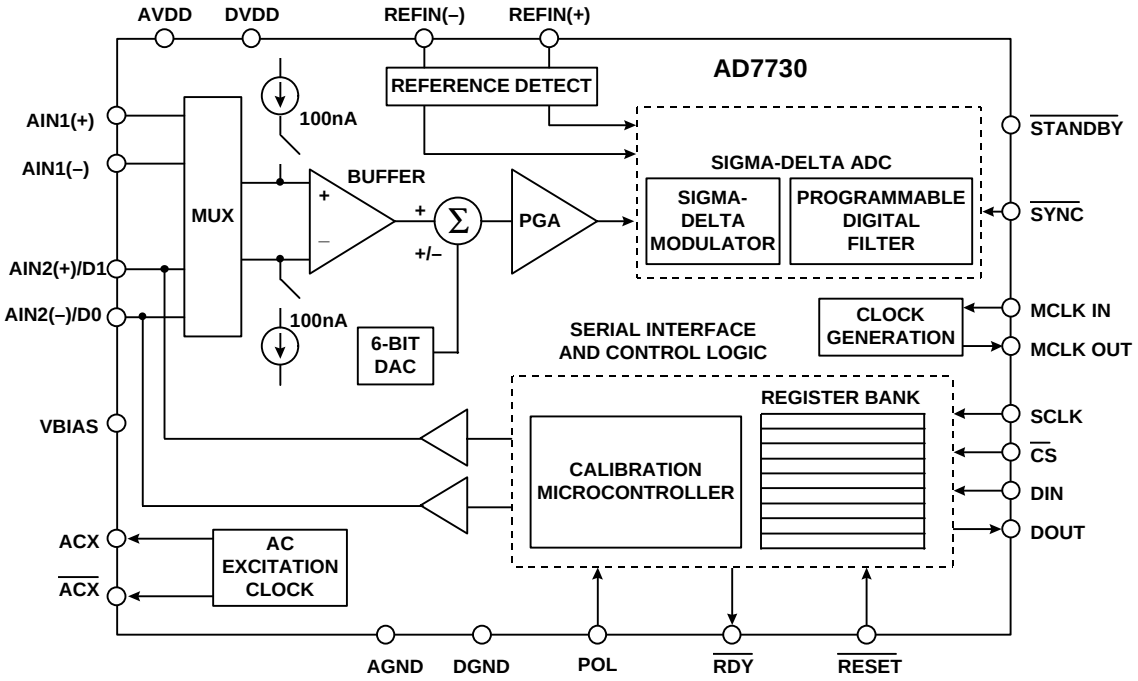


Figure 8.27

AD7730 KEY SPECIFICATIONS

- **Resolution of 80,000 Counts Peak-to-Peak (16.5-Bits) for ± 10mV Fullscale Range**
- **Chop Mode for Low Offset and Drift**
- **Offset Drift: 5nV/°C (Chop Mode Enabled)**
- **Gain Drift: 2ppm/°C**
- **Line Frequency Common Mode Rejection: > 150dB**
- **Two-Channel Programmable Gain Front End**
- **On-Chip DAC for Offset/TARE Removal**
- **FASTStep Mode**
- **AC Excitation Output Drive**
- **Internal and System Calibration Options**
- **Single +5V Supply**
- **Power Dissipation: 65mW, (125mW for 10mV FS Range)**
- **24-Lead SOIC and 24-Lead TSSOP Packages**

Figure 8.28

The 6-bit DAC is controlled by on-chip registers and can remove TARE (pan weight) values of up to ±80mV from the analog input signal range. The resolution of the TARE function is 1.25mV with a +2.5V reference and 2.5mV with a +5V reference.

The output of the PGA is applied to the ΣΔ modulator and programmable digital filter. The serial interface can be configured for three-wire operation and is compatible with microcontrollers and digital signal processors. The AD7730 contains self-calibration and system-calibration options and has an offset drift of less than 5nV/ºC and a gain drift of less than 2ppm/ºC. This low offset drift is obtained using a *chop* mode which operates similarly to a chopper-stabilized amplifier.

The oversampling frequency of the AD7730 is 4.9152MHz, and the output data rate can be set from 50Hz to 1200Hz. The clock source can be provided via an external clock or by connecting a crystal oscillator across the MCLK IN and MCLK OUT pins.

The AD7730 can accept input signals from a DC-excited bridge. It can also handle input signals from an AC-excited bridge by using the AC excitation clock signals (ACX and $\overline{ACX}$). These are non-overlapping clock signals used to synchronize the external switches which drive the bridge. The ACX clocks are demodulated on the AD7730 input.

The AD7730 contains two 100nA constant current generators, one source current from AVDD to AIN(+) and one sink current from AIN(–) to AGND. The currents are switched to the selected analog input pair under the control of a bit in the Mode Register. These currents can be used in checking that a sensor is still operational before attempting to take measurements on that channel. If the currents are turned on and a fullscale reading is obtained, then the sensor has gone open circuit. If the measurement is 0V, the sensor has gone short circuit. In normal operation, the burnout currents are turned off by setting the proper bit in the Mode Register to 0.

The AD7730 contains an internal programmable digital filter. The filter consists of two sections: a first stage filter, and a second stage filter. The first stage is a $sinc^3$ lowpass filter. The cutoff frequency and output rate of this first stage filter is programmable. The second stage filter has three modes of operation. In its normal mode, it is a 22-tap FIR filter that processes the output of the first stage filter. When a step change is detected on the analog input, the second stage filter enters a second mode (FASTStep™) where it performs a variable number of averages for some time after the step change, and then the second stage filter switches back to the FIR filter mode. The third option for the second stage filter (SKIP mode) is that it is completely bypassed so the only filtering provided on the AD7730 is the first stage. Both the FASTStep mode and SKIP mode can be enabled or disabled via bits in the control register.

Figure 8.29 shows the full frequency response of the AD7730 when the second stage filter is set for normal FIR operation. This response is with the chop mode enabled and an output word rate of 200Hz and a clock frequency of 4.9152MHz. The response is shown from DC to 100Hz. The rejection at 50Hz ± 1Hz and 60Hz ± 1Hz is better than 88dB.

Figure 8.30 shows the step response of the AD7730 with and without the FASTStep mode enabled. The vertical axis shows the code value and indicates the settling of the output to the input step change. The horizontal axis shows the number of output words required for that settling to occur. The positive input step change occurs at the 5th output. In the normal mode (FASTStep disabled), the output has not reached its final value until the 23rd output word. In FASTStep mode with chopping enabled, the output has settled to the final value by the 7th output word. Between the 7th and the 23rd output, the FASTStep mode produces a settled result, but with additional noise compared to the specified noise level for normal operating conditions. It starts at a noise level comparable to the SKIP mode, and as the averaging increases ends up at the specified noise level. The complete settling time required for the part to return to the specified noise level is the same for FASTStep mode and normal mode.

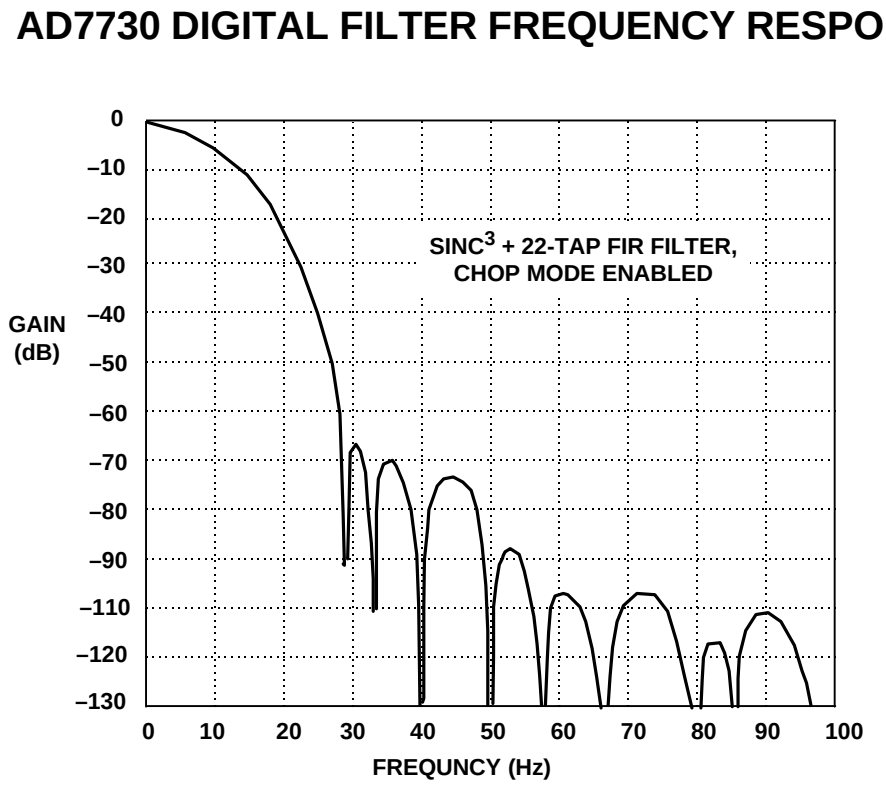


Figure 8.29

The FASTStep mode gives a much earlier indication of where the output channel is going and its new value. This feature is very useful in weigh scale applications to give a much earlier indication of the weight, or in an application scanning multiple channels where the user does not have to wait the full settling time to see if a channel has changed.

Note, however, that the FASTStep mode is not particularly suitable for multiplexed applications because of the excess noise associated with the settling time. For multiplexed applications, the full 23-cycle output word interval should be allowed for settling to a new channel. This points out the fundamental issue of using ΣΔ ADCs in multiplexed applications. There is no reason why they won't work, provided the internal digital filter is allowed to settle fully after switching channels.

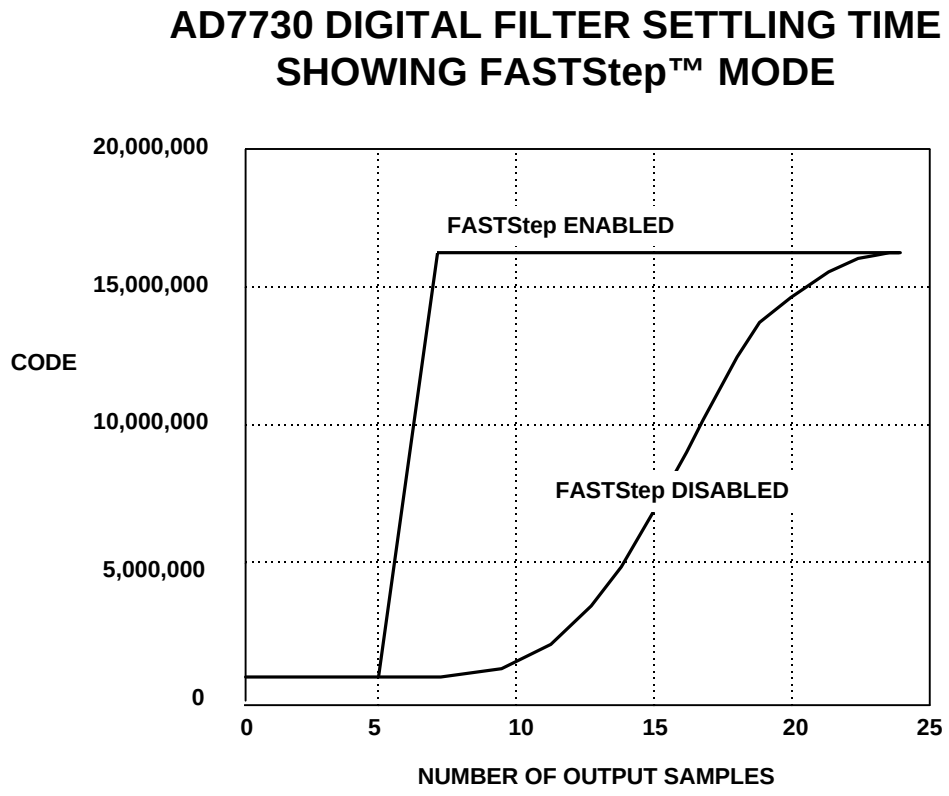


Figure 8.30

The calibration modes of the AD7730 are given in Figure 8.31. A calibration cycle may be initiated at any time by writing to the appropriate bits of the Mode Register. Calibration removes offset and gain errors from the device.

The AD7730 gives the user access to the on-chip calibration registers allowing an external microprocessor to read the device's calibration coefficients and also to write its own calibration coefficients to the part from prestored values in external E^2PROM. This gives the microprocessor much greater control over the AD7730's calibration procedure. It also means that the user can verify that the device has performed its calibration correctly by comparing the coefficients after calibration with prestored values in E^2PROM. Since the calibration coefficients are derived by

performing a conversion on the input voltage provided, the accuracy of the calibration can only be as good as the noise level the part provides in the normal mode. To optimize calibration accuracy, it is recommended to calibrate the part at its lowest output rate where the noise level is lowest. The coefficients generated at any output rate will be valid for all selected output update rates. This scheme of calibrating at the lowest output data rate does mean that the duration of the calibration interval is longer.

AD7730 SIGMA-DELTA ADC CALIBRATION OPTIONS

- **Internal Zero-ScaleCalibration**
  - **22 Output Cycles (CHP = 0)**
  - **24 Output Cycles (CHP = 1)**
- **Internal Full-Scale Calibration**
  - **44 Output Cycles (CHP = 0)**
  - **48 Output Cycles (CHP = 1)**
- **Calibration Programmed via the Mode Register**
- **Calibration Coefficients Stored in Calibration Registers**
- **External Microprocessor Can Read or Write to Calibration Coefficient Registers**

Figure 8.31

The AD7730 requires an external voltage reference, however, the power supply may be used as the reference in the ratiometric bridge application shown in Figure 8.32. In this configuration, the bridge output voltage is directly proportional to the bridge drive voltage which is also used to establish the reference voltages to the AD7730.

Variations in the supply voltage will not affect the accuracy. The SENSE outputs of the bridge are used for the AD7730 reference voltages in order to eliminate errors caused by voltage drops in the lead resistances.

AD7730 BRIDGE APPLICATION (SIMPLIFIED SCHEMATIC)

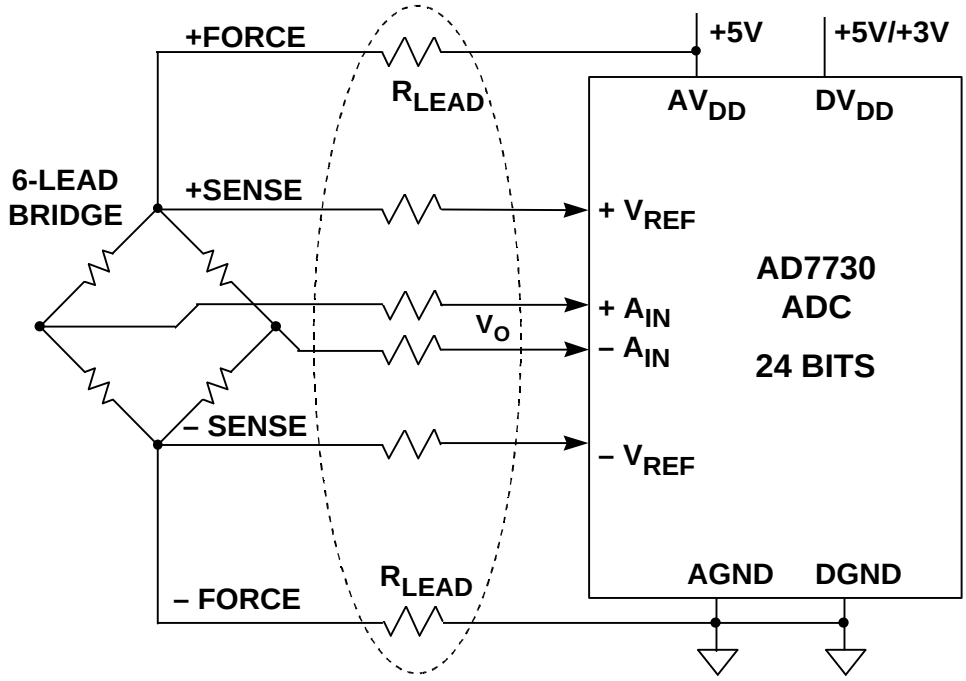
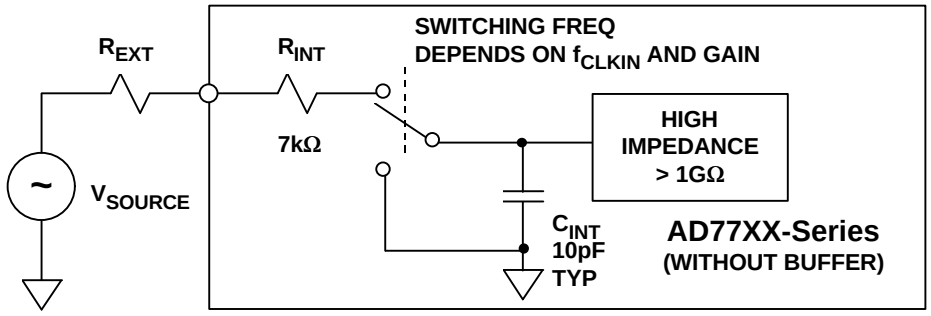


Figure 8.32

The AD7730 has a high impedance input buffer which isolates the analog inputs from switching transients generated in the PGA and the sigma-delta modulator. Therefore, no special precautions are required in driving the analog inputs. Other members of the AD77XX family, however, either do not have the input buffer, or if one is included on-chip, it can be switched either in or out under program control. Bypassing the buffer offers a slight improvement in noise performance. The equivalent input circuit of the AD77XX family without an input buffer is shown in Figure 8.33. The input switch alternates between the 10pF sampling capacitor and ground. The 7kΩ internal resistance, R_{INT}, is the on-resistance of the input multiplexer. The switching frequency is dependent on the frequency of the input clock and also the PGA gain. If the converter is working to an accuracy of 20-bits, the 10pF internal capacitor, C_{INT}, must charge to 20-bit accuracy during the time the switch connects the capacitor to the input. This interval is one-half the period of the switching signal (it has a 50% duty cycle). The input RC time constant due to the 7kΩ resistor and the 10pF sampling capacitor is 70ns. If the charge is to achieve 20-bit accuracy, the capacitor must charge for at least 14 time constants, or 980ns. Any external resistance in series with the input will increase this time constant. There are tables on the data sheets for the various AD77XX ADCs which give the maximum allowable values of R_{EXT} in order maintain a given level of accuracy. These tables should be consulted if the external source resistance is more than a few kΩ.

DRIVING UNBUFFERED AD77XX-SERIES ΣΔ ADC INPUTS



- **R_{EXT} Increases C_{INT} Charge Time and May Result in Gain Error**
- **Charge Time Dependent on the Input Sampling Rate and Internal PGA Gain Setting**
- **Refer to Specific Data Sheet for Allowable Values of R_{EXT} to Maintain Desired Accuracy**
- **Some AD77XX-Series ADCs Have Internal Buffering Which Isolates Input from Switching Circuits**

Figure 8.33

Simultaneous sampling of multiple channels is relatively common in data acquisition systems. If sigma-delta ADCs are used as shown in Figure 8.34, their outputs must be synchronized. Although the inputs are sampled at the same instant at a rate Kf_S, the decimated output word rate, f_S, is generally derived internally in each ADC by dividing the input sampling frequency by K. The output data must therefore be synchronized by the same clock at the f_S frequency. The SYNC input of the AD77XX family can be used for this purpose.

Products such as the AD7716 include multiple sigma-delta ADCs in a single IC, and provide the synchronization automatically. The AD7716 is a quad sigma-delta ADC with up to 22-bit resolution and an input oversampling rate of 570kSPS. A functional diagram of the AD7716 is shown in Figure 8.35, and key specifications in Figure 8.36. The cutoff frequency of the digital filters (which may be changed during operation, but only at the cost of a loss of valid data for a short time while the filters clear) is programmed by the data written to the control register. The output word rate depends on the cutoff frequency chosen. The AD7716 contains an auto-zeroing system to minimize input offset drift.

SYNCHRONIZING MULTIPLE SIGMA-DELTA ADCs IN SIMULTANEOUS SAMPLING APPLICATIONS

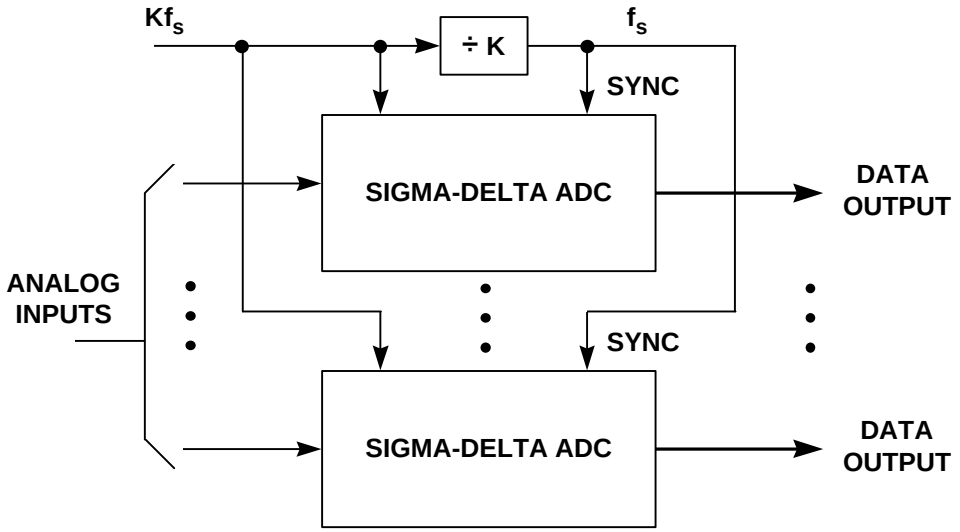


Figure 8.34

AD7716 MULTICHANNEL SIGMA-DELTA ADC

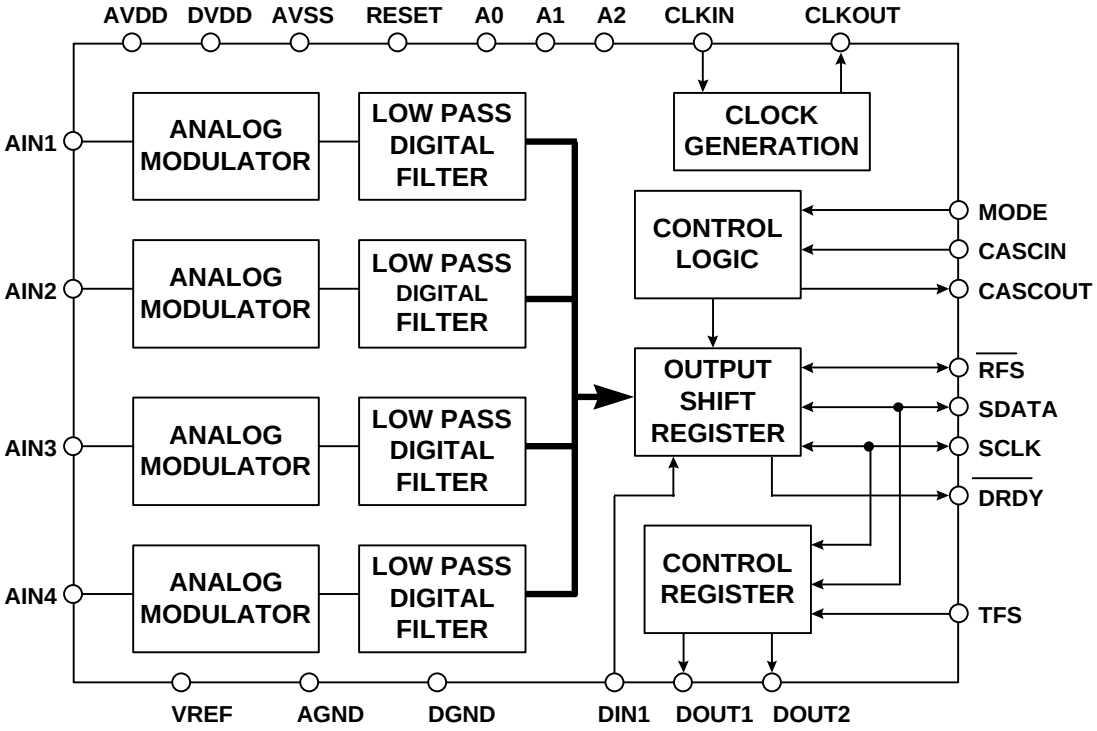


Figure 8.35

AD7716 KEY SPECIFICATIONS

- **Up to 22-Bit Resolution, 4 Input Channels**
- **Sigma-Delta Architecture, 570kSPS Oversampling Rate**
- **On-Chip Lowpass Filter, Programmable from 36.5Hz to 584Hz**
- **Serial Input / Output Interface**
- **±5V Power Supply Operation**
- **50mW Power Dissipation**

Figure 8.36

APPLICATIONS OF SIGMA-DELTA ADCS IN POWER METERS

While electromechanical energy meters have been popular for over 50 years, a solid-state energy meter delivers far more accuracy and flexibility. Just as important, a well designed solid-state meter will have a longer useful life. The AD7750 Product-to-Frequency Converter is the first of a family of ICs designed to implement this type of meter.

We must first consider the fundamentals of power measurement (see Figure 8.37). Instantaneous AC voltage is given by the expression $v(t) = V \times \cos(\omega t)$, and the current (assuming it is in phase with the voltage) by $i(t) = I \times \cos(\omega t)$. The *instantaneous power* is the product of v(t) and i(t):

$$p(t) = V \times I \times \cos^2(\omega t)$$

Using the trigonometric identity, $2\cos^2(\omega t) = 1 + \cos(2\omega t)$,

$$p(t) = \frac{V \times I}{2}\left[1 + \cos(2\omega t)\right] = \text{Instantaneous Power.}$$

The *instantaneous real power* is simply the average value of p(t). It can be shown that computing the instantaneous real power in this manner gives accurate results even if the current is not in phase with the voltage (i.e., the power factor is not unity. By definition, the power factor is equal to $\cos\theta$, where θ is the phase angle between the voltage and the current). It also gives the correct real power if the waveforms are non-sinusoidal.

BASICS OF POWER MEASUREMENTS

- $v(t) = V \times \cos(\omega t)$ (Instantaneous Voltage)
- $i(t) = I \times \cos(\omega t)$ (Instantaneous Current)
- $p(t) = V \times I \cos^2(\omega t)$ (Instantaneous Power)
- $p(t) = \frac{V \times I}{2}\left[1 + \cos(2\omega t)\right]$

Average Value of p(t) = Instantaneous *Real Power*

Includes Effects of Power Factor and Waveform Distortion

Figure 8.37

The AD7750 implements these calculations, and a block diagram is shown in Figure 8.38. There are two inputs to the device. The differential voltage between V1+ and V1– is a voltage corresponding to the instantaneous current. It is usually derived from a small transformer placed in series with the line. The AD7750 is designed with a switched capacitor architecture that allows a bipolar analog input with a single +5V supply. The input voltage passes through a PGA which can be set for a gain of 1 or 16. The gain of 16 option allows for low values of shunt impedances in the current monitoring circuit. The output of the PGA drives a 2nd order 16-bit sigma-delta modulator which samples the signal at a 900kHz rate. The serial bit stream from the modulator is passed through a digital highpass filter to remove any DC component. The highpass filter has a phase lead of 2.58º at 50Hz. In order to equalize the phase difference between the two channels, a fixed delay of 143µs is then introduced in the signal path. Because the time delay is fixed, external phase compensation will be required if the line frequency differs from 50Hz. There are several ways to accomplish this, and they are described in detail in the AD7750 data sheet.

The differential voltage applied between V2+ and V2– represents the voltage waveform (scaled to the AD7750 input range). It is passed through a gain of 2 amplifier and a second sigma-delta modulator. The voltage and current outputs are then multiplied digitally yielding the *instantaneous power*. The *instantaneous real power* is then obtained by passing the instantaneous power through a digital lowpass filter. The low frequency outputs F1 and F2 are generated by accumulating this real power information. The F1 and F2 outputs provide two alternating low-going pulses. This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the *average real power*. This average real power information can in turn be accumulated (e.g., an electromechanical pulse counter or full stepping two phase stepper-motor) to generate real energy information. The pulse width is set at 275ms. The frequency of these pulses is 0Hz to about 14Hz.

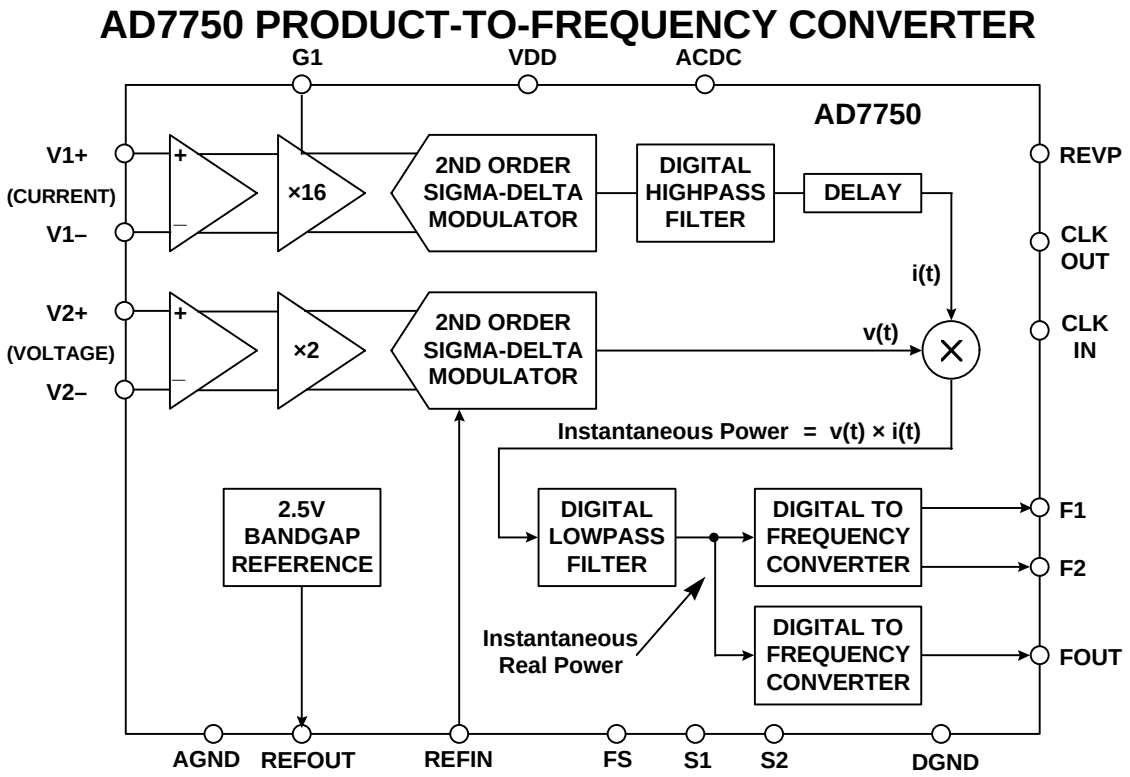


Figure 8.38

Because of its high output frequency and hence shorter integration time, the FOUT output is proportional to the *instantaneous* real power. This is useful for system calibration purposes which would take place under steady load conditions.

The error in the real power measurement is less than 0.2% over a dynamic range of 500:1 and less than 0.4% over a dynamic range of 1000:1.

A single-phase power meter application is shown in Figure 8.39. The ground for the entire circuit is referenced to the neutral line. The +5V power for the circuit is derived from an AC to DC supply which is powered from the phase (hot) line. This can be simple half-wave diode rectifier followed by a filter capacitor. The F1 and F2 outputs drive the kW-Hr counter which displays the energy usage.

The REVP output (reverse polarity) drives an LED and goes high when negative power is detected (i.e., when the voltage and current signals are 180º out of phase). This condition would generally indicate a potential mis-wiring condition.

The AD7751 Energy Metering IC operates in a similar fashion to the AD7750 but has inhanced performance features. It has on-chip fault detection circuits which monitor the current in both the phase (hot) and neutral line. A fault is indicated when these currents differ by more than 12.5%, and billing is continued using the larger of the two currents.

AD7750 SINGLE PHASE POWER METER APPLICATION (SIMPLIFIED SCHEMATIC)

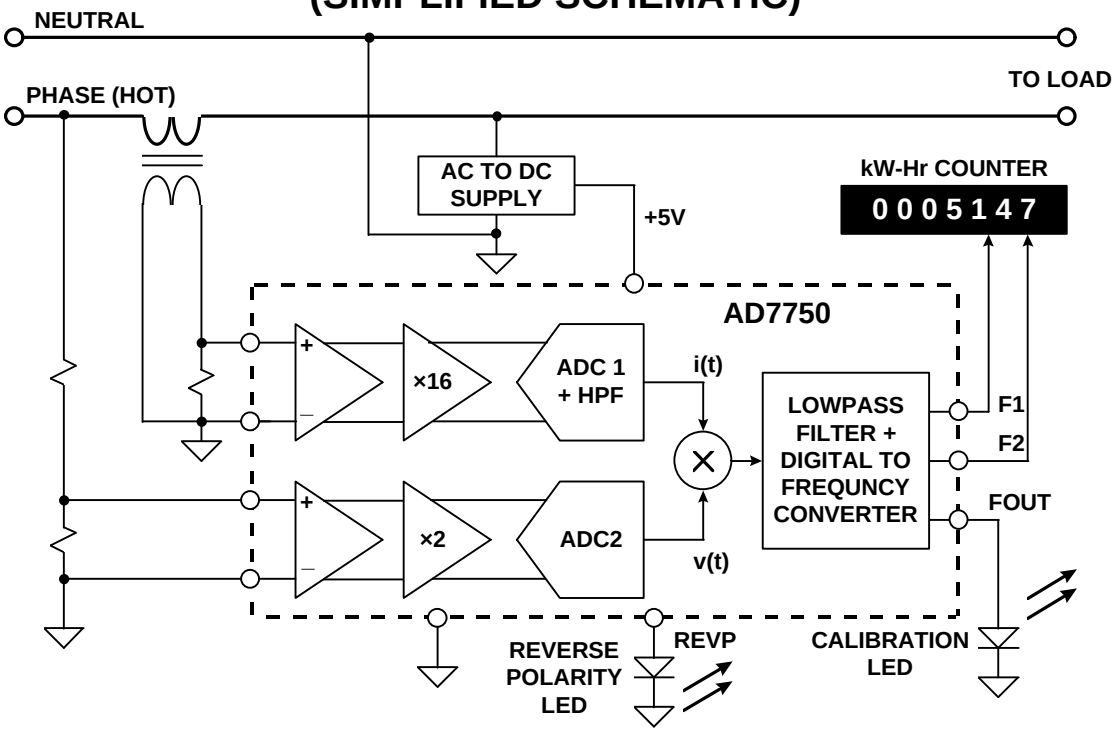


Figure 8.39

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SECTION 9
SMART SENSORS
Walt Kester, Bill Chestnut, Grayson King

4-20mA Control Loops

Industrial process control systems make extensive use of 4-20mA control loops. Many sensors and actuators are designed precisely for this mode of control. They are popular because they are simple to understand, offer a method of standardizing the sensor/control interface, and are relatively immune to noise. Figure 9.1 shows how a remote actuator is controlled via such a loop from a centrally located control room. Notice that the transmitter output to the actuator is controlled by a DAC, in this case, the AD420. The entire process is under the control of a host computer which interfaces to the microcontroller and the AD420. This diagram shows only one actuator, however an actual industrial control system would have many actuators and sensors. Notice that the "zero scale" output of the DAC is actually 4mA, and "fullscale" is 20mA. The choice of a non-zero output current for "zero scale" allows open circuit detection at the transmitter and allows the loop to actually power the remote sensor if its current requirement is less than 4mA.

CONTROLLING A REMOTE ACTUATOR USING A 4-20mA LOOP

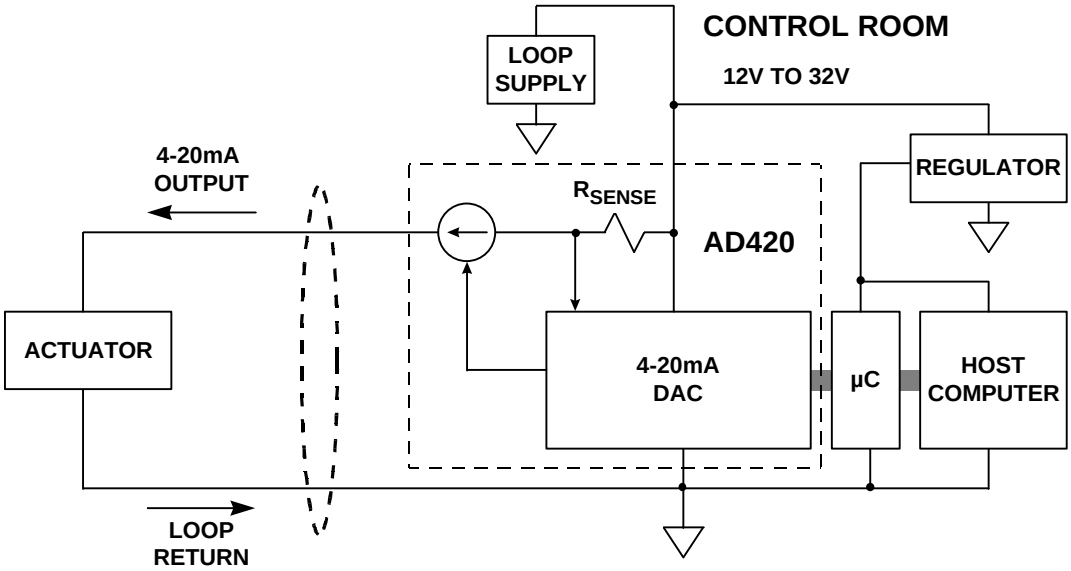


Figure 9.1

Many of the control room circuits are directly powered by the loop power supply which can range from approximately 12V to 36V. In many cases, however, this voltage must be regulated to supply such devices as amplifiers, ADCs, and microcontrollers. The loop current is sensed by the R_{SENSE} resistor which is actually a part of the AD420. The internal DAC in the AD420 is a sigma-delta type

with 16-bit resolution and monotonicity. The serial digital interface allows easy interface to the microcontroller.

Figure 9.2 shows a 4-20mA output "smart" sensor which is completely powered by the loop power supply. In order for this to work, the sum total of all the circuits under loop power can be no more than 4mA. The heart of the circuit is the AD421 loop-powered 16-bit DAC. The internal 4-20mA DAC current as well as the rest of the return current from the AD421 and the other circuits under loop power flows through the R_{SENSE} resistor. The sensing circuit compensates for the additional return current and ensures that the actual loop return current corresponds to that required by the digital code applied to the DAC through the microcontroller. The sensor output is digitized by the AD7714/AD7715 sigma-delta ADC. Note that the total current required by all the circuits under loop power is less than the required 4mA maximum. The AD421 contains a regulator circuit which controls the gate of the external DMOS FET and regulates the loop voltage to either 3V, 3.3V, or 5V to power the loop circuits. In this way the maximum loop supply voltage is limited only by the breakdown voltage of the DMOS FET.

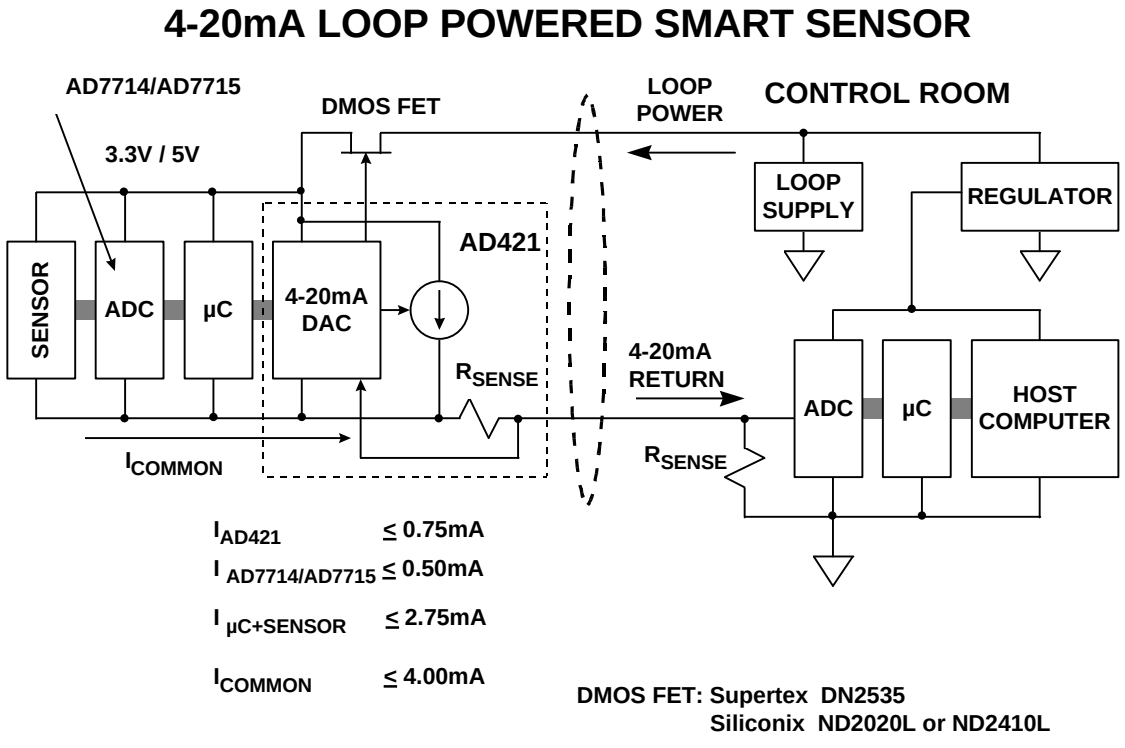


Figure 9.2

The HART protocol uses a frequency shift keying (FSK) technique based on the Bell 202 Communications Standard which is one of several standards used to transmit digital signals over the telephone lines. This technique is used to superimpose digital communication on to the 4-20mA current loop connecting the control room to the transmitter in the field. Two different frequencies, 1200Hz and 2200Hz, are used to represent binary 1 and 0 respectively. These sinewave tones are superimposed on the DC signal at a low level with the average value of the sinewave being zero. This allows simultaneous analog and digital communications. Additionally, no DC component is added to the existing 4-20mA signal regardless of the digital data

being sent over the line. The phase of the digital FSK signal is continuous, so there are no high frequency components injected onto the 4-20mA loop. Consequently, existing analog instruments continue to work in systems that implement HART, as the lowpass filtering usually present effectively removes the digital signal. A single pole 10Hz lowpass filter effectively reduces the communication signal to a ripple of about ±0.01% of the fullscale signal. The HART protocol specifies that master devices like a host control system transmit a voltage signal, whereas a slave or field device transmits a current signal. The current signal is converted into a corresponding voltage by the loop load resistor in the control room.

Figure 9.3 shows a block diagram of a smart and intelligent transmitter. An intelligent transmitter is a transmitter in which the function of the microprocessor are shared between deriving the primary measurement signal, storing information regarding the transmitter itself, its application data, and its location, and also managing a communication system which enables two-way communication to be superimposed on the same circuit that carries the measurement signal. A smart transmitter incorporating the HART protocol is an example of a smart intelligent transmitter.

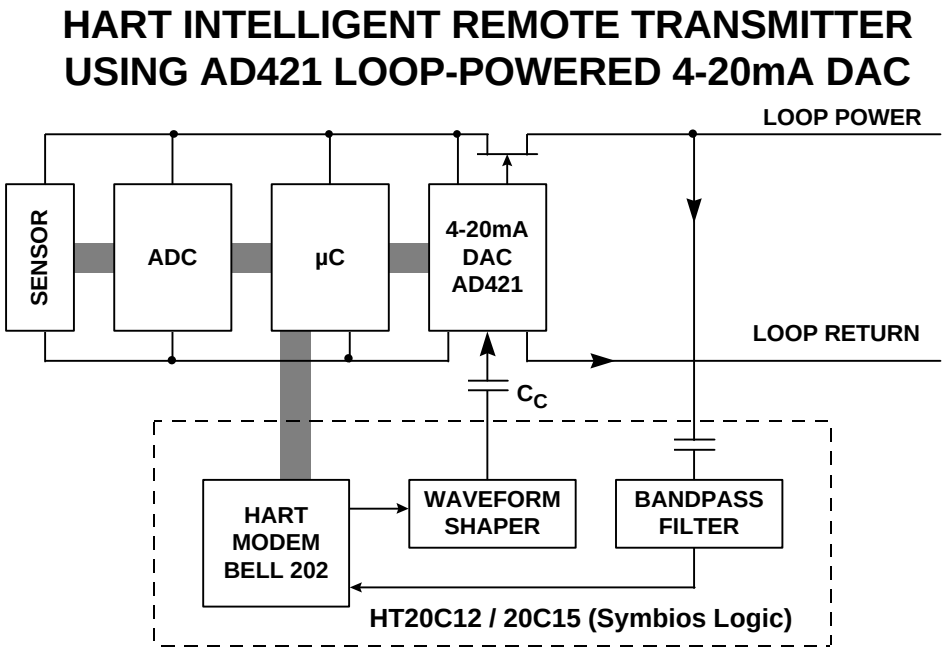


Figure 9.3

The HART data transmitted on the loop shown in Figure 9.3 is received by the transmitter using a bandpass filter and modem, and the HART data is transferred to the microcontroller's UART or asynchronous serial port to the modem. It is then waveshaped before being coupled onto the AD421's output through the coupling capacitor C_C. The block containing the Bell 202 Modem, waveshaper, and bandpass filter come in a complete solution with the 20C15 from Symbios Logic, Inc., or HT2012 from SMAR Research Corporation.

INTERFACING SENSORS TO NETWORKS
Grayson King

The HART protocol is just one of many standards for industrial networking. Most industrial networks run independently of analog 4-20mA lines, but many are intended to interface (directly or indirectly) with smart sensors as shown in Figure 9.4.

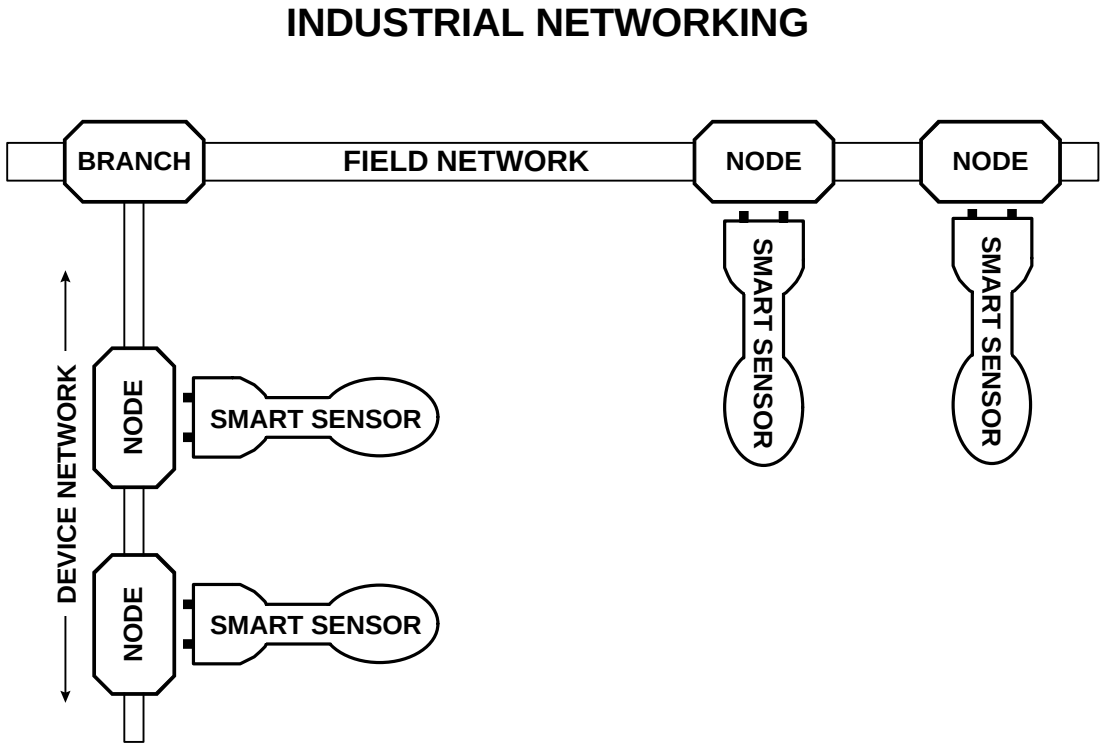


Figure 9.4

These industrial networks can take many forms. The "field network" in Figure 9.4 represents a wide bandwidth distributed network such as Ethernet or Lonwork. A field network by this definition is not generally intended to interface directly with a smart sensor. A "device network," on the other hand, is intended specifically to interface to smart sensors. Most "device networks" (such as ASI-bus, CAN-bus, and HART) also provide power to smart sensors on the same lines that carry serial data. Some of today's more popular industrial network standards are listed in Figure 9.5. Each offers its own advantages and disadvantages, and each has a unique hardware implementation and serial protocol. This means that a smart sensor designed for one industrial network is not necessarily compatible with another.

Since factories and many other networked environments often have multiple networks and sub-networks, a far more flexible solution is one where sensors are "plug and play" compatible with all different field and device networks. The goal of the IEEE 1451.2 sensor interface standard is to make network independent sensors a reality.

SOME OF THE STANDARDS

- Ethernet
- CAN-Bus
- Foundation Fieldbus
- Device-Net
- Lonwork
- WorldFIP
- Profibus
- P-NET
- Interbus-S
- HART
- Universal Serial Bus (USB)
- ASI

Figure 9.5

Figure 9.6 shows the basic components of an IEEE 1451.2 compatible system. The smart sensor (or smart actuator) is referred to as a "STIM" (Smart Transducer Interface Module). It contains one or more sensors and/or actuators in addition to any signal conditioning and A/D or D/A conversion required to interface the sensors/actuators with the resident microcontroller. The microcontroller also has access to nonvolatile memory that contains a "TEDS" field (or Transducer Electronic Data Sheet) which stores sensor/actuator specifications that can be read via the industrial network. The NCAP (Network Capable Application Processor) is basically a node on the network to which a STIM can be connected. At the heart of the IEEE 1451.2 is the standardized 10-wire serial interface between the sensor and the NCAP, called the TII (or Transducer Independent Interface). In an environment with multiple networks, the TII allows any STIM to be plugged into any NCAP node on any network as shown in Figure 9.7. When the STIM is first connected to the new NCAP, the STIM's digital information (including its TEDS) is made available to the network. This identifies what type of sensor or actuator has just been connected and indicates what input and output data are available, the units of input an output data (cubic meters per second, degrees Kelvin, kilopascals, etc.), the specified accuracy of the sensor (±2°C, etc.), and various other information about the sensor or actuator. This effectively eliminates the software configuration steps involved in replacing or adding a sensor, thereby allowing true "plug and play" performance with network independence.

THE IEEE 1451.2 SENSOR INTERFACE STANDARD

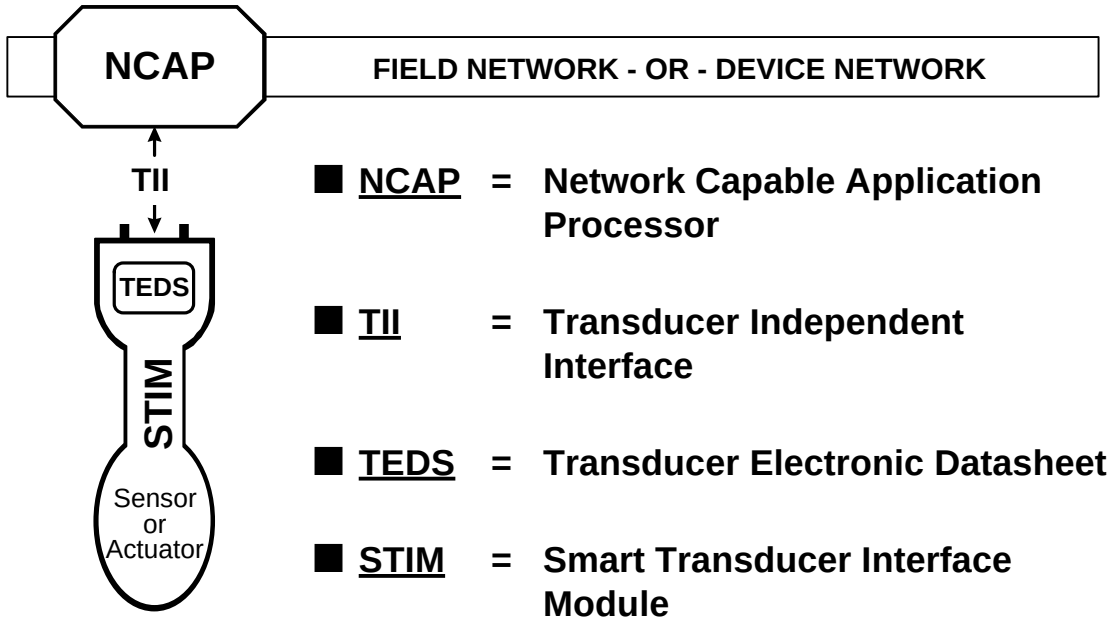


Figure 9.6

TRUE "PLUG AND PLAY"

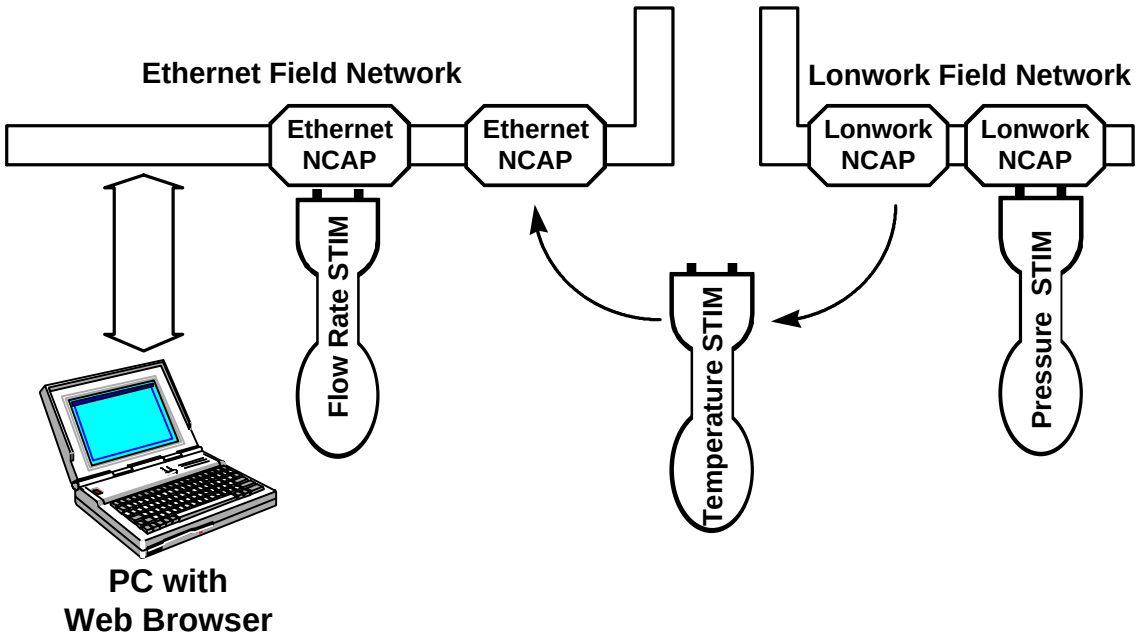


Figure 9.7

Most smart sensors (not limited to 1451.2 STIMs) contain the primary components shown in Figure 9.8. The Analog Devices MicroConverter™ products are the first to incorporate all of these components on a single chip (Figure 9.9).

THE SMART SENSOR

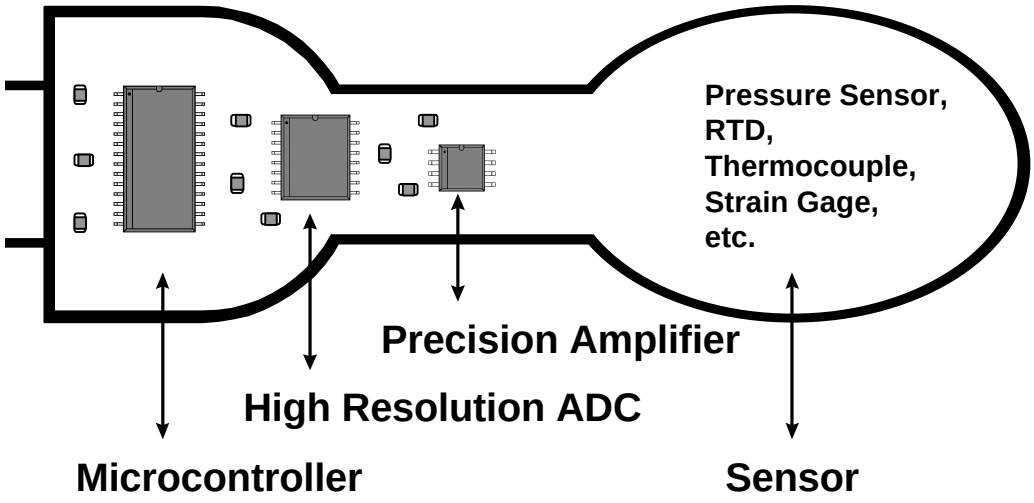


Figure 9.8

THE EVEN SMARTER SENSOR

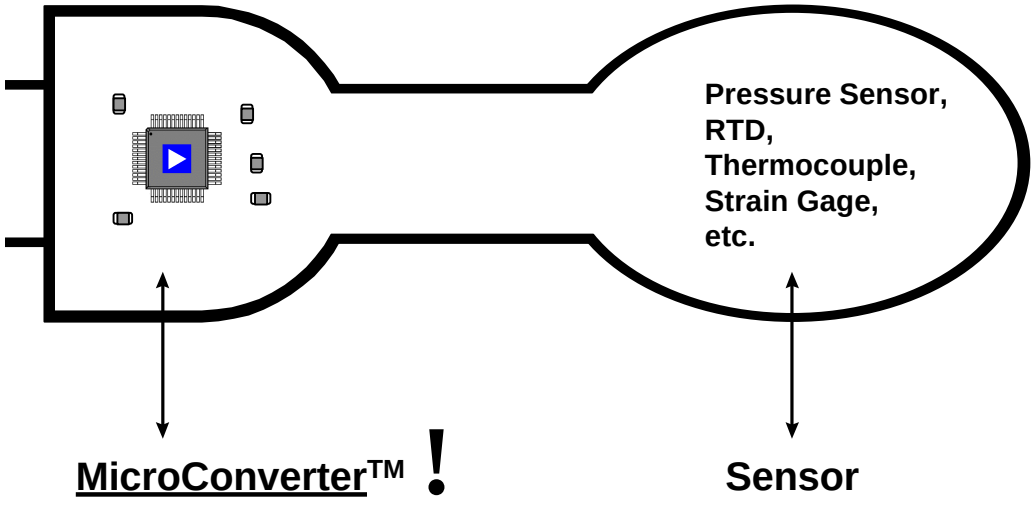


Figure 9.9

The three primary functions of every MicroConverter™ product (Figure 9.10), are: high resolution analog-to-digital and digital-to-analog conversion, non-volatile FLASH EEPROM for program and data storage, and a microcontroller. Of the first three MicroConverter™ products to be introduced, all contain a 12-bit voltage output DAC, a precision bandgap voltage reference, and an on-chip temperature

sensor. Figure 9.11 lists the basic analog I/O functionality of each. All three have exactly the same FLASH memory and microcontroller core, some features of which are highlighted in Figures 9.12 and 9.13.

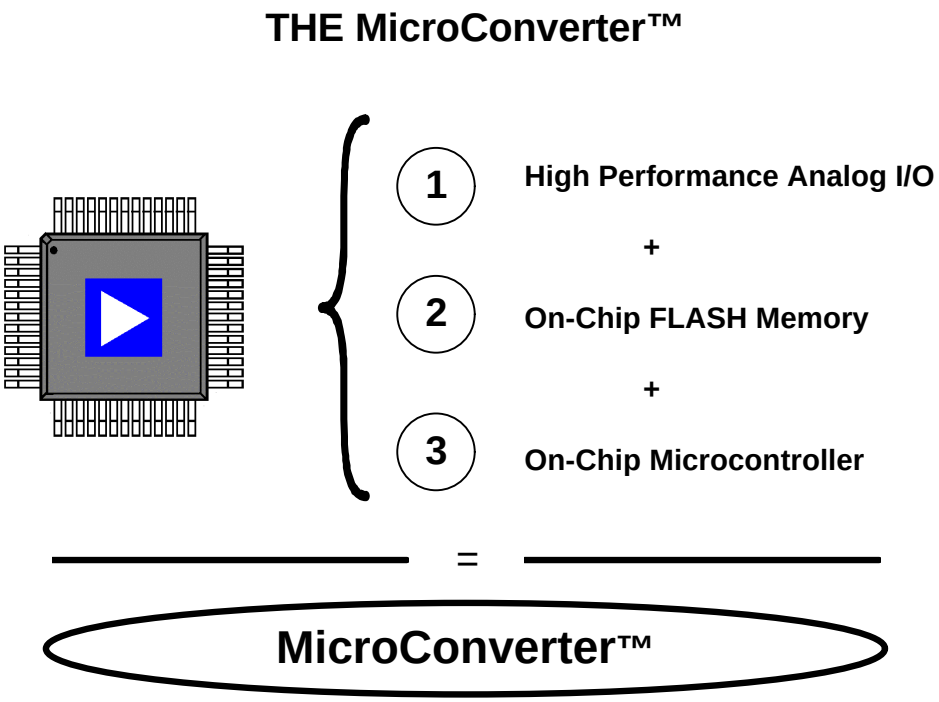


Figure 9.10

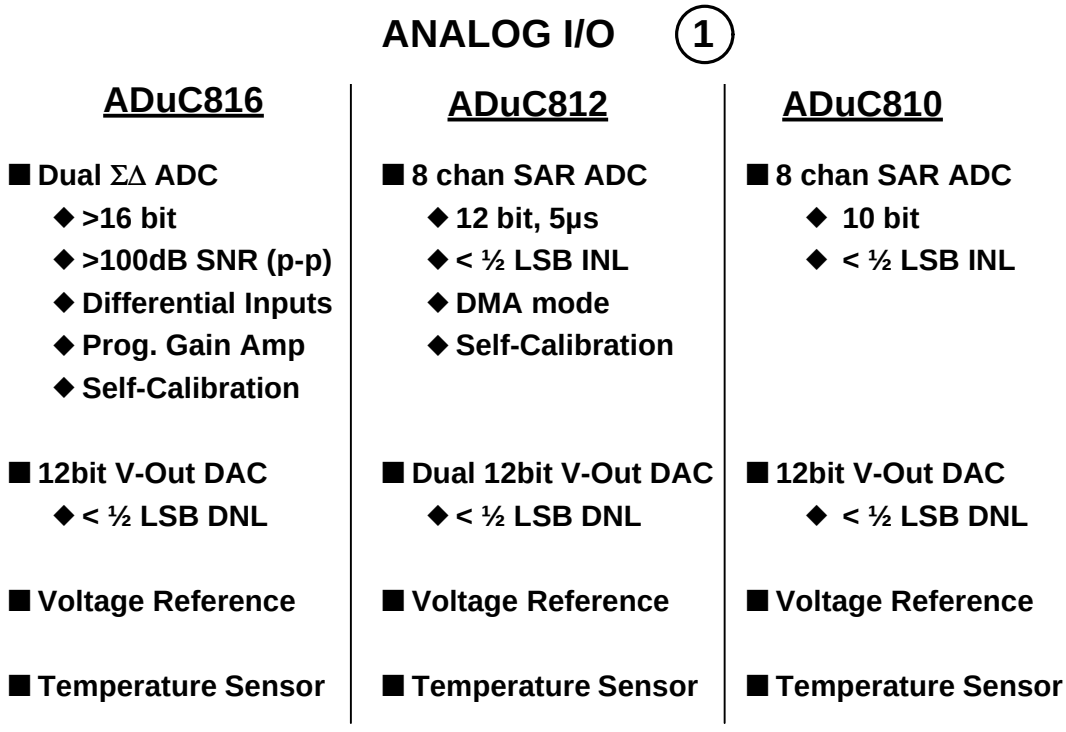


Figure 9.11

ON-CHIP FLASH MEMORY (2)

ADuC816 ; ADuC812 ; ADuC810

- **8K bytes Nonvolatile FLASH Program Memory**
  - **Stores Program and Fixed Lookup Tables**
  - **In-Circuit Serial Programmable or External Parallel Programmable**
  - **Read-Only to Microprocessor Core**

- **640 bytes Nonvolatile FLASH Data Memory**
  - **User "Scratch Pad" for Storing Data During Program Execution**
  - **Simple Read / Write Access Through SFR Space**

- **Programming Voltage (V_{PP}) Generated On-Chip**

Figure 9.12

ON-CHIP MICROCONTROLLER (3)

ADuC816 ; ADuC812 ; ADuC810

- **Industry Standard 8052 Core**
  - **12 Clock Machine Cycle w/ up to 16MHz Clock**
  - **32 Digital I/O Pins**
  - **Three 16bit Counter/Timers**
  - **Universal Asynchronous Receiver/Transmitter (UART) Serial Port**

- **...Plus Some Useful Extras**
  - **SPI or I2C Compatible Serial Interface**
  - **WatchDog Timer**
  - **Power Supply Monitor**
  - **Timer Interval Counter (ADuC816/810)**

Figure 9.13

The highest resolution MicroConverter™ product is the ADuC816. Its analog front end consists of two separate ΣΔ ADC converters with a flexible multiplexing scheme to access its two differential input channels as illustrated in the functional block diagram of Figure 9.14. The "primary channel" ADC is a 24-bit ΣΔ converter that offers better than 16-bit signal-to-noise ratio. This primary channel also features a programmable gain amplifier (PGA), allowing direct conversion of low-level signals such as thermocouples, RTDs, strain gages, etc. Two "burn out" current sources can be configured to force a very small current through the sensor to detect open circuit conditions when the sensor may have been disconnected or "burned out". The primary channel ADC can be multiplexed to convert both of the differential input channels, or the second differential input can be routed to the "auxiliary channel" ADC which is a 16-bit ΣΔ converter with better than 14-bits of signal-to-noise ratio. This auxiliary channel can also be used to read the on-chip temperature sensor. A pair of 200μA current sources ($I_{EXC}1$ & $I_{EXC}2$) can be used to provide excitation for sensors such as RTDs. Both ADCs as well as the DAC can be operated with the internal 2.5V bandgap reference, or with an external reference.

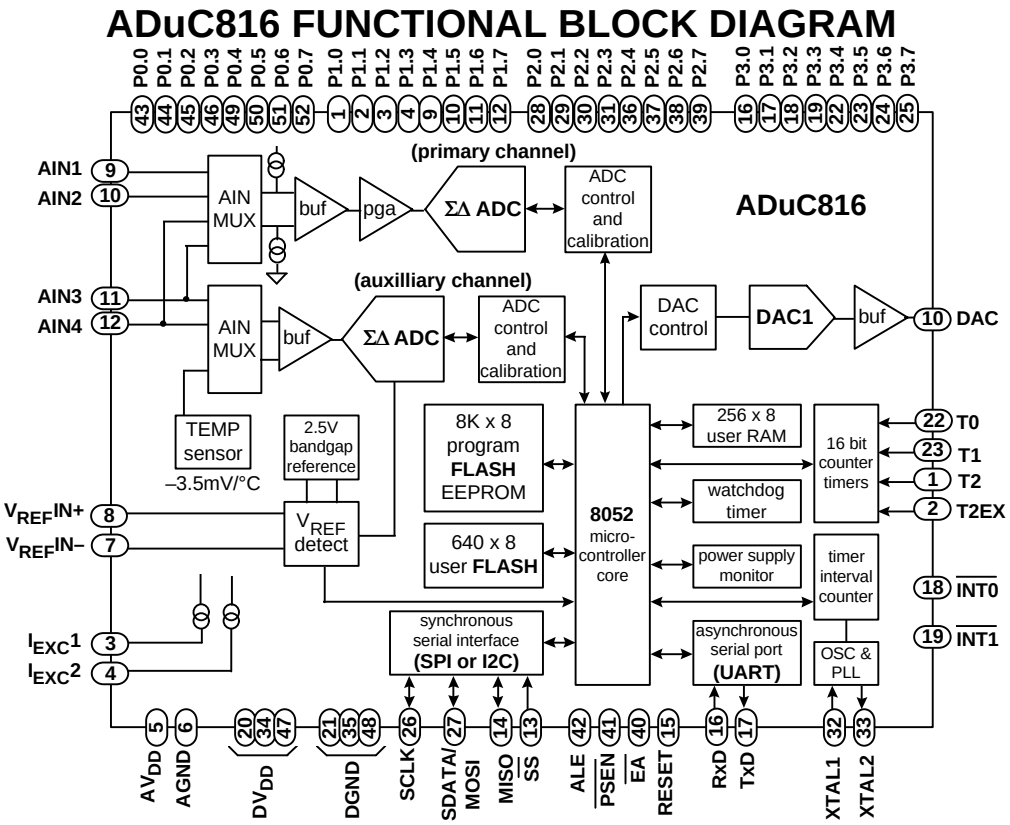


Figure 9.14

The primary performance specifications of the ADuC816 are given in Figure 9.15. All ADC specifications here refer to the "primary channel" ADC. Exceptionally low power dissipation can be achieved in low bandwidth applications by keeping the ADuC816 in the power down mode for much of the time. By using an internal PLL, the chip derives its 12MHz clock from a 32kHz watch crystal. When in power down mode, the 12MHz clock is disabled, but the 32kHz crystal continues to drive a real-time counter which can be set to wake the chip up at predefined intervals. The ADuC816 can also be configured to wake up upon receiving an external interrupt.

ADuC816 - PRIMARY SPECIFICATIONS

■ **ADC :**	**INL**	**-**	**± 30ppm**
	SNR (p-p)	**-**	**>102dB (17 Noise Free Bits)**
	Input Range	**-**	**± 20mV to ± 2.56V**
	Conv. Rate	**-**	**5.4Hz to 105Hz**
■ **DAC :**	**DNL**	**-**	**± ½LSB**
	Output Range	**-**	**0 to V_{REF} -or- 0 to V_{DD}**
	Settling Time	**-**	**<4µs**

■ **Power :** **Specified for 3V or 5V Operation**

	5V	3V
Normal	**7mA**	**3mA**
Idle	**4.5mA**	**1.5mA**
Powerdown	**<20µA**	**<20µA**

Figure 9.15

The ADuC812 offers a fast (5µs) 12-bit 8-channel successive approximation ADC with many of the same peripheral features of the ADuC816. The functional block diagram (Figure 9.16) illustrates its primary components. Since the 8-bit × 1MIPS microcontroller core cannot generally keep up with the 12-bit 200kSPS ADC output data, a DMA (direct memory access) controller is included on the ADuC812 to automatically write ADC results to external memory, thus freeing the microcontroller core for other tasks. Whether in DMA mode or in normal mode, the ADuC812 conversions can be triggered by several means. Conversions can be triggered in software, or a timer can be set to automatically initiate a conversion each time it overflows, thereby allowing precise control of sampling rate. A hardware convert-start can also be utilized for applications requiring critical timing.

The ADuC812 contains two 12-bit DACs that can be powered on or off independently of each other, and can be updated either simultaneously or independently. The DACs can be configured for an output range of 0 to V_{DD} or 0 to V_{REF}, where V_{REF} can be either the internal 2.5V bandgap reference or an externally applied reference voltage. The internal reference, if used, can also be buffered to drive external circuitry.

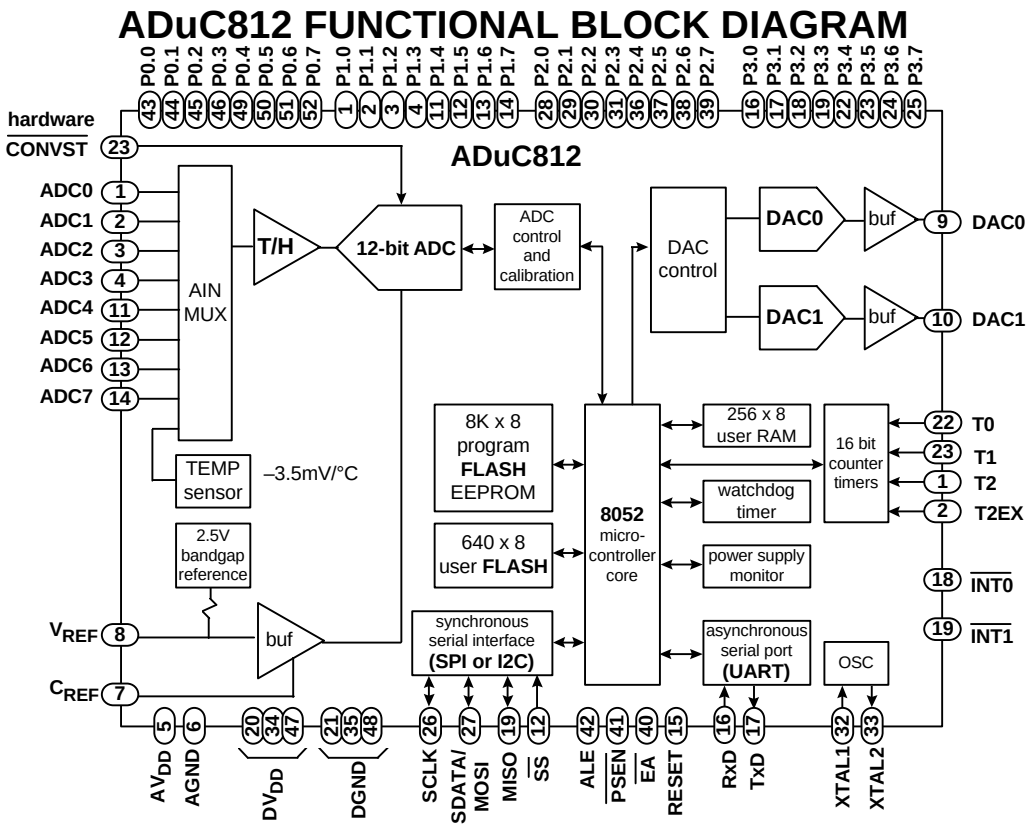


Figure 9.16

Figure 9.17 lists some primary performance specifications of the ADuC812. The power specifications are given assuming a 12MHz crystal. Since all on-chip logic is static, the clock can be slowed to any frequency, allowing exceptionally low power dissipation in low bandwidth applications. For applications requiring greater speed, the clock can be increased to as much as 16MHz to achieve slightly faster microcontroller operation (1.33MIPS).

Because MicroConverter™ products are based on an industry standard 8052 core, developers can draw from a wealth of software, reference material, and third party tools that already exist for 8051/8052 MCUs. The MicroConverter™ web site provides links to many sources of such material, in addition to offering downloads of internally generated tools, data sheets, and example software.

ADuC812 - PRIMARY SPECIFICATIONS

■ **ADC :**	**INL**	**-**	**± ½LSB**
	SNR (p-p)	**-**	**>70dB**
	Input Range	**-**	**0 to V_{REF}**
	Conv. Time	**-**	**<5µs (200kSPS)**
■ **DAC :**	**DNL**	**-**	**± ½LSB**
	Output Range	**-**	**0 to V_{REF} -or- 0 to V_{DD}**
	Settling Time	**-**	**<4µs**

■ **Power :** **Specified for 3V or 5V Operation**

	5V	3V
Normal	**18mA**	**12mA**
Idle	**10mA**	**6mA**
Powerdown	**<50µA**	**<50µA**

Figure 9.17

MicroConverter™ DESIGN SUPPORT

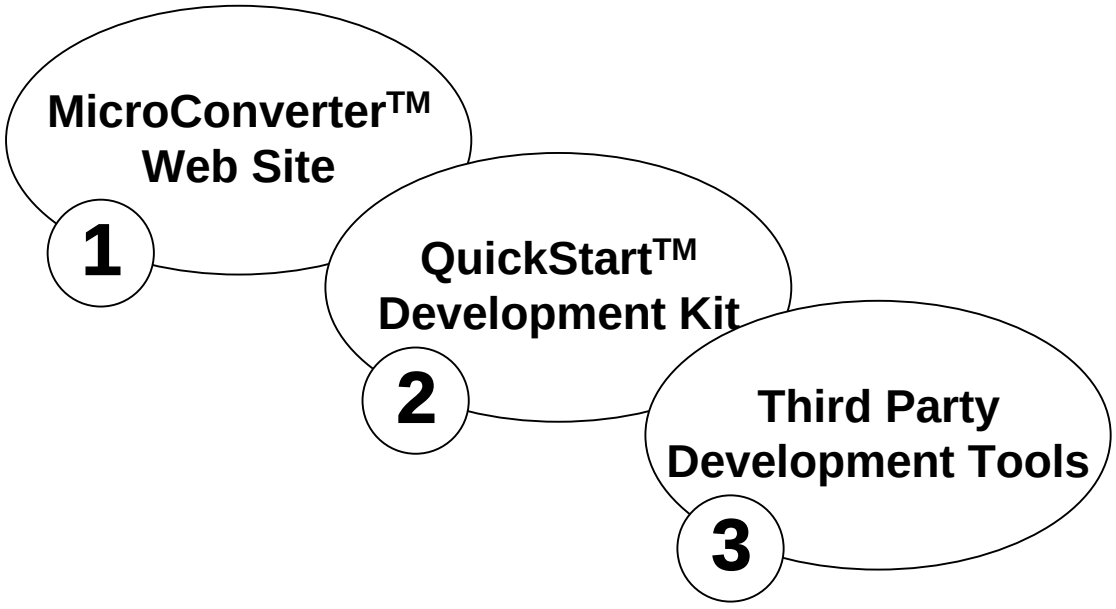


Figure 9.18

MicroConverter™ WEB SITE

- Data Sheets
- Application Notes
- 8051 Reference Material
- Free Windows MicroConverter™ Simulator
- Free Keil 'C' Compiler (2K limited version)

Figure 9.19

To get any designer or developer started with a MicroConverter product, Analog Devices offers a QuickStart™ Development Kit which contains all of the necessary features for many designers to complete a design without the added expense of additional simulation or in-circuit emulation packages.

MicroConverter™ - QuickStart™ DEVELOPMENT KIT

- Documentation
  - User's Guide
  - Datasheet
  - Tools Tutorial
  - Quick Reference Guide
- Evaluation Board
  - RS-232 Serial Comms
  - 32K External SRAM
  - Buffered Analog I/O
- Regulated Power Supply
- Serial Port Cable
- Software
  - Metalink Assembler
  - 'C' Compiler (Limited 2K)
  - Windows Simulator
  - Serial Downloader
  - Windows Debugger
  - Example Code

Figure 9.20

For designs that require the added power of full in-circuit emulation, or the added ease of C coding with mixed-mode debugging, Keil and Metalink offer the first of many third party tools to be endorsed by Analog Devices. These tools are fully compatible with the MicroConverter™ products, and other third party developers will soon offer additional MicroConverter™-specific tools to further expand the options available to designers.

MicroConverter™ - THIRD PARTY DEVELOPMENT TOOLS

The First Two of Many Third Party Tools to Fully Support MicroConverter™ Products:

3

Power Tools

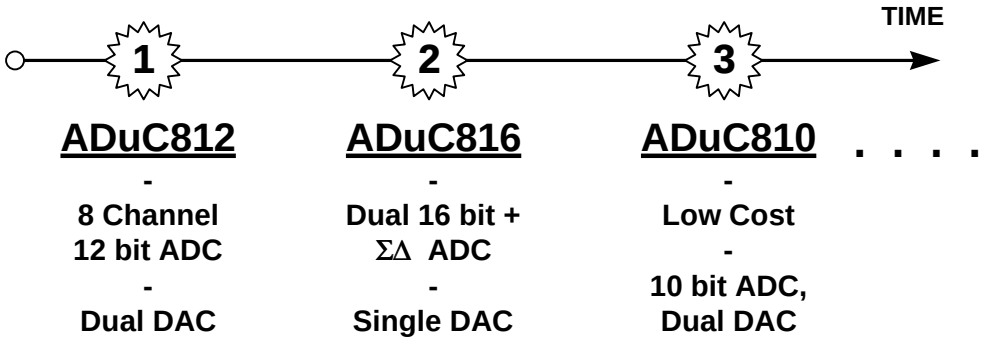
- **Keil Compiler**
  - **A full function *windows based 'C' compiler* environment featuring a simulator for source and assembly level debugging.**
- **MetaLink Emulator**
  - **A high end *in circuit emulation* system offering a complete windows based environment for in-system debug sessions.**

All tools will fully integrate with each MicroConverter product

Figure 9.21

While the ADuC812, ADuC816, and ADuC810 offer a mix of features and performance not previously available in a single chip, future MicroConverter™ products will offer even greater levels of integration and functionality. Larger FLASH memory versions will be offered to compliment one or more of the existing products. Additional hardware communications may also be added to future MicroConverter™ products to allow direct communication with industrial networks or PC platforms. Eventually, there will be MicroConverter™ products with greater MCU processing bandwidth. However, comparing these devices to basic microcontrollers is a mistake. The performance level of MicroConverter™ analog I/O is far superior to that available in microcontrollers with analog I/O ports.

MicroConverter™ PRODUCT ROADMAP



. . . . Future Products May Include:

- **Larger FLASH Memory Capacity (Data and Program)**
- **Hardware Communications Interface Enhancements (CAN Bus, USB Bus)**
- **Increased Microcontroller Horsepower**

Figure 9.22

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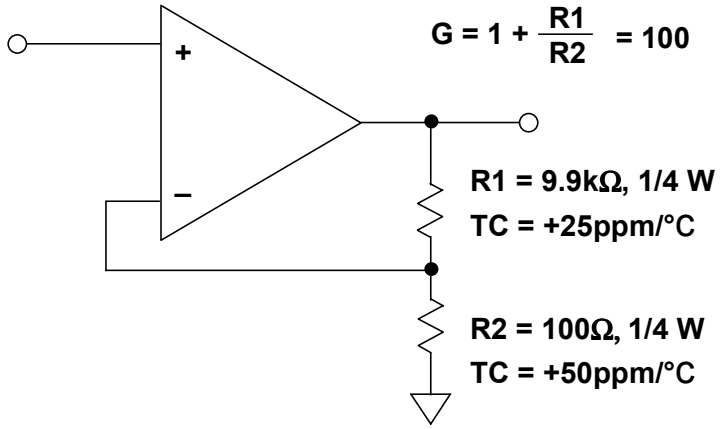
SECTION 10
HARDWARE DESIGN TECHNIQUES
Walt Kester

RESISTOR AND THERMOCOUPLE ERRORS IN HIGH ACCURACY SYSTEMS
Walt Kester, Walt Jung, and James Bryant

Resistor accuracy is crucial in precision systems. The circuit element called a *resistor* should not be taken for granted! Figure 10.1 shows a simple non-inverting op amp where the gain of 100 is set by the external resistors R1 and R2. The temperature coefficients of the two resistors are a somewhat obvious source of error. Assume that the op amp gain errors are negligible, and that the resistors are perfectly matched at +25ºC. If the temperature coefficients of the resistors differ by only 25ppm/ºC, the gain of the amplifier will change by 250ppm for a 10ºC temperature change. This is about 1 LSB in a 12-bit system, and a major disaster in a 16-bit system.

RESISTOR TEMPERATURE COEFFICIENT MISMATCHES CAUSE GAIN VARIATION WITH TEMPERATURE



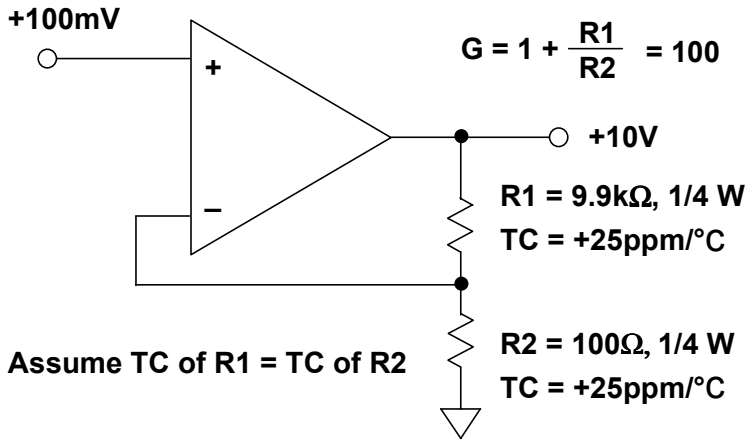
- **Temperature change of 10°C causes gain change of 250ppm**
- **This is 1LSB in a 12-bit system and a disaster in a 16-bit system**

Figure 10.1

Even if the temperature coefficients are identical, there still may be significant errors. Suppose R1 and R2 have identical temperature coefficients of +25ppm/ºC and are both ¼W resistors. If the signal input in Figure 10.2 is zero, the resistors will dissipate no heat, but if it is 100mV there will be 9.9V across R1 which will dissipate 9.9mW and experience a temperature rise of 1.24ºC (the thermal resistance of a ¼W resistor is 125ºC/W). The 1.24ºC rise causes a resistance change

of 31ppm, and a corresponding change in gain. R2, with only 100mV across it, is only heated 0.0125ºC, which is negligible. The 31ppm gain error represents a fullscale error of ½ LSB at 14-bits, and is a disaster for a 16-bit system.

RESISTOR SELF-HEATING EVEN IN MATCHED RESISTORS CAN CAUSE GAIN VARIATION WITH INPUT LEVEL



- R1, R2 Thermal Resistance = 125°C / W
- Temperature of R1 will rise by 1.24°C, P_D = 9.9mW
- Temperature rise of R2 is negligible, P_D = 0.1mW
- Gain is altered by 31ppm, or 1/2 LSB @ 14-bits

Figure 10.2

These, and similar errors, are avoided by selecting critical resistors that are accurately matched for both value and temperature coefficient, and ensuring tight thermal coupling between resistors whose matching is important. This is best achieved by using a resistor network on a single substrate - such a network may be within an IC or may be a separately packaged thin-film resistor network.

Another more subtle problem with resistors is the thermocouple effect, sometimes referred to as thermal EMF. Wherever there is a junction between two different conductors there is a thermoelectric voltage. If two junctions are present in a circuit, we have a thermocouple, and if these two junctions are at different temperatures, there will be a net voltage in the circuit. This effect is used to measure temperature, but is a potential source of inaccuracy in low level circuits, since wherever two different conductors meet, we have a thermocouple, whether we like it or not. This will cause errors if the various junctions are at different temperatures. The effect is hard to avoid, even if we are only making connections with copper wire, since a copper-to-copper junction formed by copper wire from two different manufacturers may have a thermoelectric voltage of up to 0.2µV/ºC.

Consider the resistor model shown in Figure 10.3. The connections between the resistor material and the leads form two thermocouple junctions. The thermocouple EMF can be as high as 400µV/ºC for carbon composition resistors and as low as

0.05µV/ºC for specially constructed resistors (Reference 1). Metal film resistors (RN-types) are typically about 20µV/ºC.

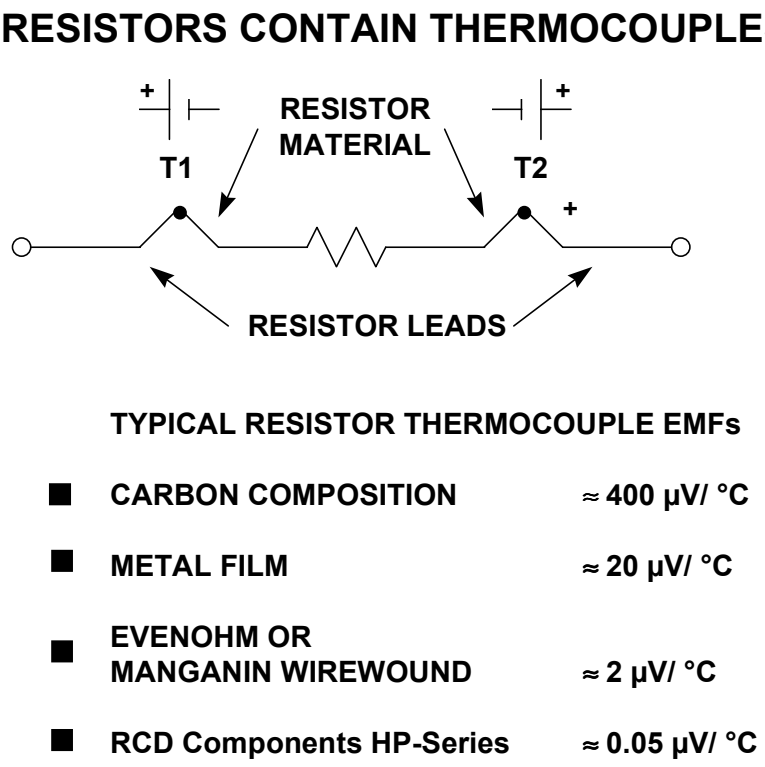


Figure 10.3

These thermocouple effects are unimportant at AC or where the resistor is at a uniform temperature, but if the dissipation in a resistor, or its orientation with respect to heat sources, can cause one of its ends to be warmer than the other, then there will be a net thermocouple voltage differential, which will introduce a DC error into the circuit. For instance, using ordinary metal film resistors, a temperature differential of 1ºC will cause a thermocouple voltage of 20µV which is quite significant when compared to the input offset voltage of truly precision op amps such as the OP177 or the AD707, and extremely significant when compared to chopper-stabilized op amps.

Figure 10.4 shows how resistor orientation can make a difference in the net thermocouple voltage. Standing the resistor on end in order to conserve board space will invariable cause a temperature gradient across the resistor, especially if it is dissipating any significant power. Placing the resistor flat on the PC board will eliminate this problem unless there is airflow across the resistor parallel to its axis. Orienting the resistor axis perpendicular to the airflow will minimize the error, since this tends to force the resistor ends towards the same temperature.

Figure 10.5 shows how to orient the resistor on a vertically mounted PC board, where the convection cooling air currents flow up the board. Again, the thermal axis of the resistor should be perpendicular to the convection flow to minimize the effect.

Because of their small size, the thermocouple effect in surface mount resistors is generally less than leaded types because of the tighter thermal coupling between the ends of the resistor.

AVOIDING THERMAL GRADIENTS MINIMIZES THERMOCOUPLE ERROR VOLTAGES

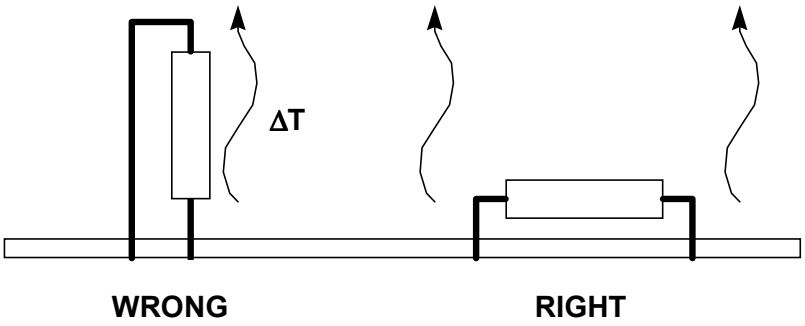


Figure 10.4

PROPER ORIENTATION OF SURFACE MOUNT RESISTORS MINIMIZES THERMOCOUPLE ERROR VOLTAGE

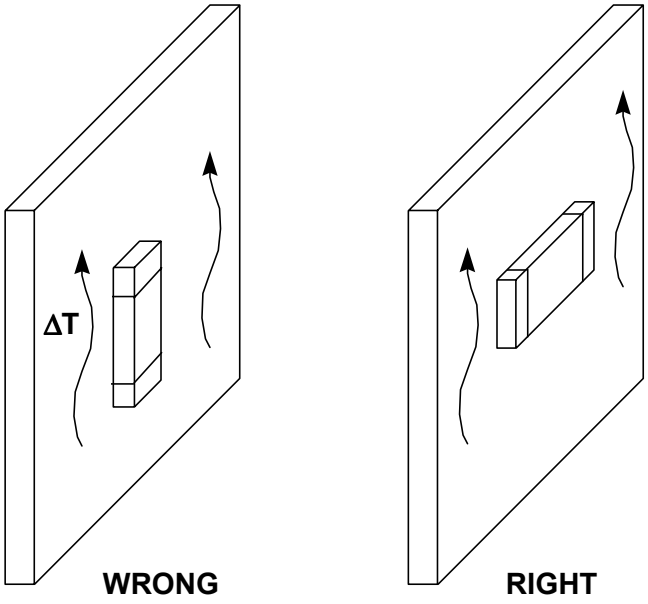


Figure 10.5

A simple circuit shown in Figure 10.6 will further illustrate the parasitic thermocouple problem. Here, we have a remote bridge driving an instrumentation amplifier which has current limiting resistors in each lead. Each resistor has four thermocouples: two are internal to the resistor, and two are formed where the resistor leads connect to the copper wires. Another pair of thermocouples is formed where the copper wire connects to the Kovar pins of the in-amp. The Copper/Kovar junction has a thermocouple voltage of about 35µV/ºC. Most molded plastic ICs use copper leadframes which would be an order of magnitude or so less (e.g., the AD620 in-amp).

In addition, the copper wire has a resistance temperature coefficient (TC of 30 gage copper wire is approximately 0.385%/ºC) which can introduce error if the temperature of the wires is significantly different, or if they are different lengths. In this example, however, this error is negligible because there is minimal current flow in the wires.

Obviously, this simple circuit must have a good thermal as well as electrical design in order to maintain microvolt precision. Some good design precautions include minimizing number of thermocouple junctions, minimizing thermal gradients by proper layout or blocking airflow to critical devices using metallic or plastic shields, minimizing power dissipation in sensitive devices, proper selection of precision resistors, and matching the number of junctions in each half of a differential signal path by adding "dummy" components if required. Sockets, connectors, switches, or relays in the critical signal path can introduce unstable contact resistances as well as "unknown" thermocouple junctions which may not track to the required accuracy. They should be avoided if possible.

PARASITIC THERMOCOUPLES IN SIMPLE CIRCUIT

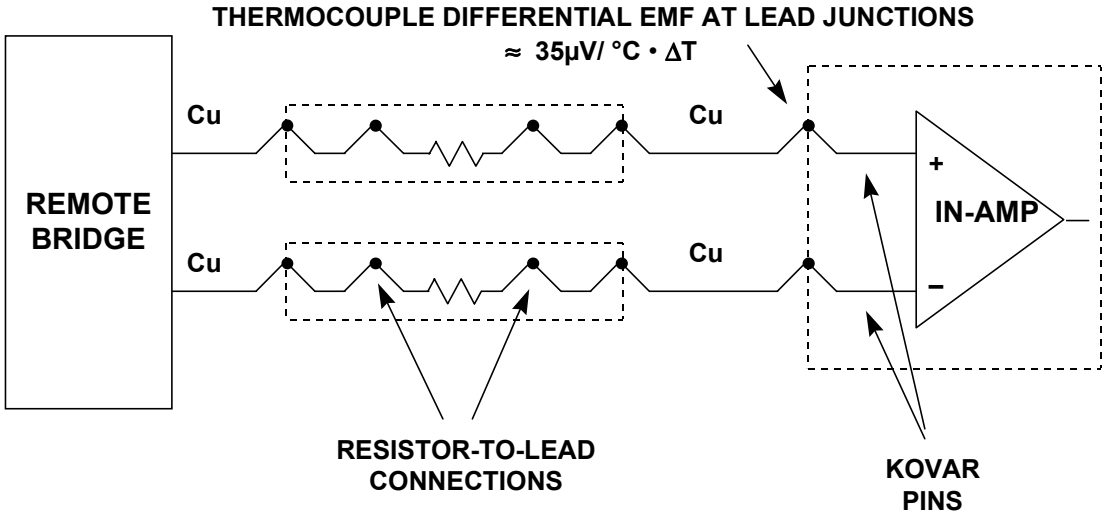


Figure 10.6

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GROUNDING IN MIXED SIGNAL SYSTEMS

Walt Kester, James Bryant

Today's signal processing systems generally require mixed-signal devices such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) as well as fast digital signal processors (DSPs). Requirements for processing analog signals having wide dynamic ranges increases the importance of high performance ADCs and DACs. Maintaining wide dynamic range with low noise in hostile digital environments is dependent upon using good high-speed circuit design techniques including proper signal routing, decoupling, and grounding.

In the past, "high precision, low-speed" circuits have generally been viewed differently than so-called "high-speed" circuits. With respect to ADCs and DACs, the sampling (or update) frequency has generally been used as the distinguishing speed criteria. However, the following two examples show that in practice, most of today's signal processing ICs are really "high-speed," and must therefore be treated as such in order to maintain high performance. This is certainly true of DSPs, and also true of ADCs and DACs.

All sampling ADCs (ADCs with an internal sample-and-hold circuit) suitable for signal processing applications operate with relatively high speed clocks with fast rise and fall times (generally a few nanoseconds) and must be treated as high speed devices, even though throughput rates may appear low. For example, the 12-bit AD7892 successive approximation (SAR) ADC operates on an 8MHz internal clock, while the sampling rate is only 600kSPS.

Sigma-delta (Σ-Δ) ADCs also require high speed clocks because of their high oversampling ratios. The AD7722 16-bit ADC has an output data rate (effective sampling rate) of 195kSPS, but actually samples the input signal at 12.5MSPS (64-times oversampling). Even high resolution, so-called "low frequency" Σ-Δ industrial measurement ADCs (having throughputs of 10Hz to 7.5kHz) operate on 5MHz or higher clocks and offer resolution to 24-bits (for example, the Analog Devices AD7730 and AD7731).

To further complicate the issue, mixed-signal ICs have both analog and digital ports, and because of this, much confusion has resulted with respect to proper grounding techniques. Digital and analog design engineers tend to view these devices from different perspectives, and the purpose of this section is to develop a general grounding philosophy that will work for most mixed signal devices, without having to know the specific details of their internal circuits.

Ground and Power Planes

The importance of maintaining a low impedance large area ground plane is critical to all analog circuits today. The ground plane not only acts as a low impedance return path for decoupling high frequency currents (caused by fast digital logic) but

also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuits susceptibility to external EMI/RFI is also reduced.

Ground planes also allow the transmission of high speed digital or analog signals using transmission line techniques (microstrip or stripline) where controlled impedances are required.

The use of "buss wire" is totally unacceptable as a "ground" because of its impedance at the equivalent frequency of most logic transitions. For instance, #22 gauge wire has about 20nH/inch inductance. A transient current having a slew rate of 10mA/ns created by a logic signal would develop an unwanted voltage drop of 200mV at this frequency flowing through 1 inch of this wire:

$$\Delta v = L\frac{\Delta i}{\Delta t} = 20nH \times \frac{10mA}{ns} = 200mV.$$

For a signal having a 2V peak-to-peak range, this translates into an error of about 200mV, or 10% (approximate 3.5-bit accuracy). Even in all-digital circuits, this error would result in considerable degradation of logic noise margins.

Figure 10.7 shows an illustration of a situation where the digital return current modulates the analog return current (top figure). The ground return wire inductance and resistance is shared between the analog and digital circuits, and this is what causes the interaction and resulting error. A possible solution is to make the digital return current path flow directly to the GND REF as shown in the bottom figure. This is the fundamental concept of a "star," or single-point ground system. Implementing the true single-point ground in a system which contains multiple high frequency return paths is difficult because the physical length of the individual return current wires will introduce parasitic resistance and inductance which can make obtaining a low impedance high frequency ground difficult. In practice, the current returns must consist of large area ground planes for low impedance to high frequency currents. Without a low-impedance ground plane, it is therefore almost impossible to avoid these shared impedances, especially at high frequencies.

All integrated circuit ground pins should be soldered directly to the low-impedance ground plane to minimize series inductance and resistance. The use of traditional IC sockets is not recommended with high-speed devices. The extra inductance and capacitance of even "low profile" sockets may corrupt the device performance by introducing unwanted shared paths. If sockets must be used with DIP packages, as in prototyping, individual "pin sockets" or "cage jacks" may be acceptable. Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6). They have spring-loaded gold contacts which make good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade their performance.

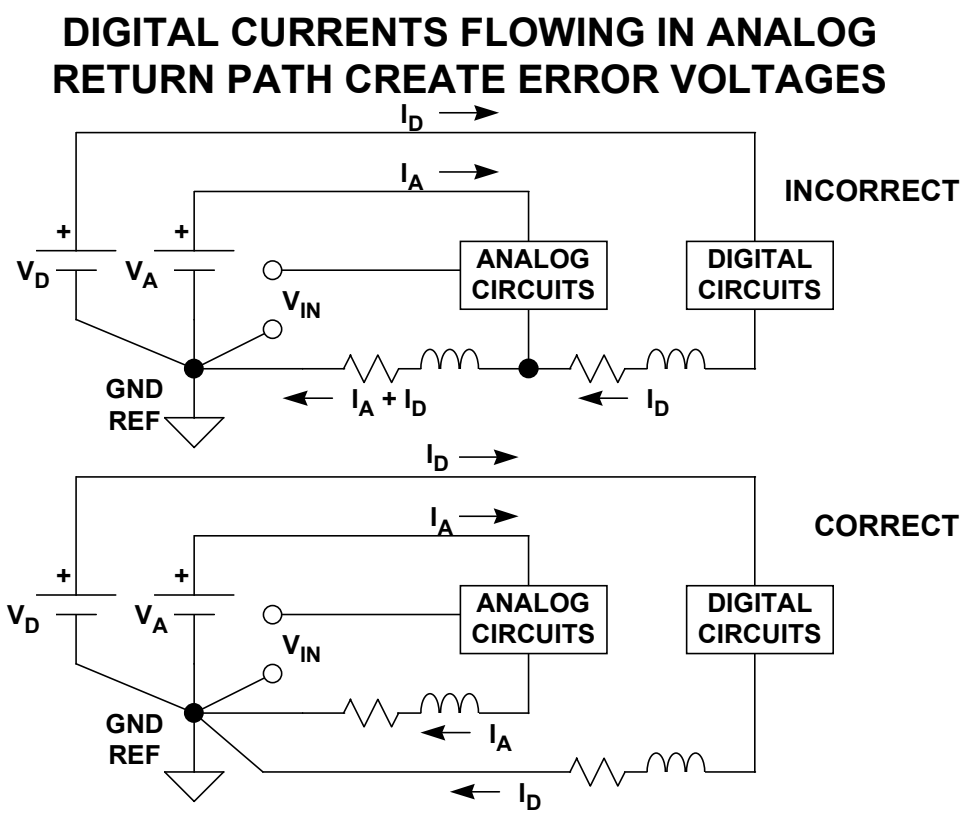

Figure 10.7

Power supply pins should be decoupled directly to the ground plane using low inductance ceramic surface mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1mm. The ceramic capacitors should be located as close as possible to the IC power pins. Ferrite beads may be also required for additional decoupling.

Double-Sided vs. Multilayer Printed Circuit Boards

Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side completely dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers, vias, and through-holes. Nevertheless, as much area as possible should be preserved, and at least 75% should remain. After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated ground "islands," because IC ground pins located in a ground "island" have no current return path to the ground plane. Also, the ground plane should be checked for "skinny" connections between adjacent large areas which may significantly reduce the effectiveness of the ground plane. Needless to say, auto-routing board layout techniques will generally lead to a layout disaster on a mixed-signal board, so manual intervention is highly recommended.

Systems that are densely packed with surface mount ICs will have a large number of interconnections; therefore multilayer boards are preferred. This allows a complete layer to be dedicated to ground. A simple 4-layer board would have internal ground and power plane layers with the outer two layers used for interconnections between the surface mount components. Placing the power and ground planes adjacent to each other provides additional inter-plane capacitance which helps high frequency decoupling of the power supply.

GROUND PLANES ARE MANDATORY!

- **Use Large Area Ground (and Power) Planes for Low Impedance Current Return Paths (Must Use at Least a Double-Sided Board!)**
- **Double-Sided Boards:**
  - **Avoid High-Density Interconnection Crossovers and Feedthroughs Which Reduce Ground Plane Area**
  - **Keep > 75% Board Area on One Side for Ground Plane**
- **Multilayer Boards**
  - **Dedicate at Least One Layer for the Ground Plane**
  - **Dedicate at Least One Layer for the Power Plane**
- **Use at Least 30% to 40% of PCB Connector Pins for Ground**
- **Continue the Ground Plane on the Backplane Motherboard to Power Supply Return**

Figure 10.8

Multicard Mixed-Signal Systems

The best way of minimizing ground impedance in a multicard system is to use a "motherboard" PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the backplane. The PCB connector should have at least 30-40% of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities:

1. The backplane ground plane can be connected to chassis ground at numerous points, thereby diffusing the various ground current return paths. This is commonly referred to as a "multipoint" grounding system and is shown in Figure 10.9.

2. The ground plane can be connected to a single system "star ground" point (generally at the power supply).

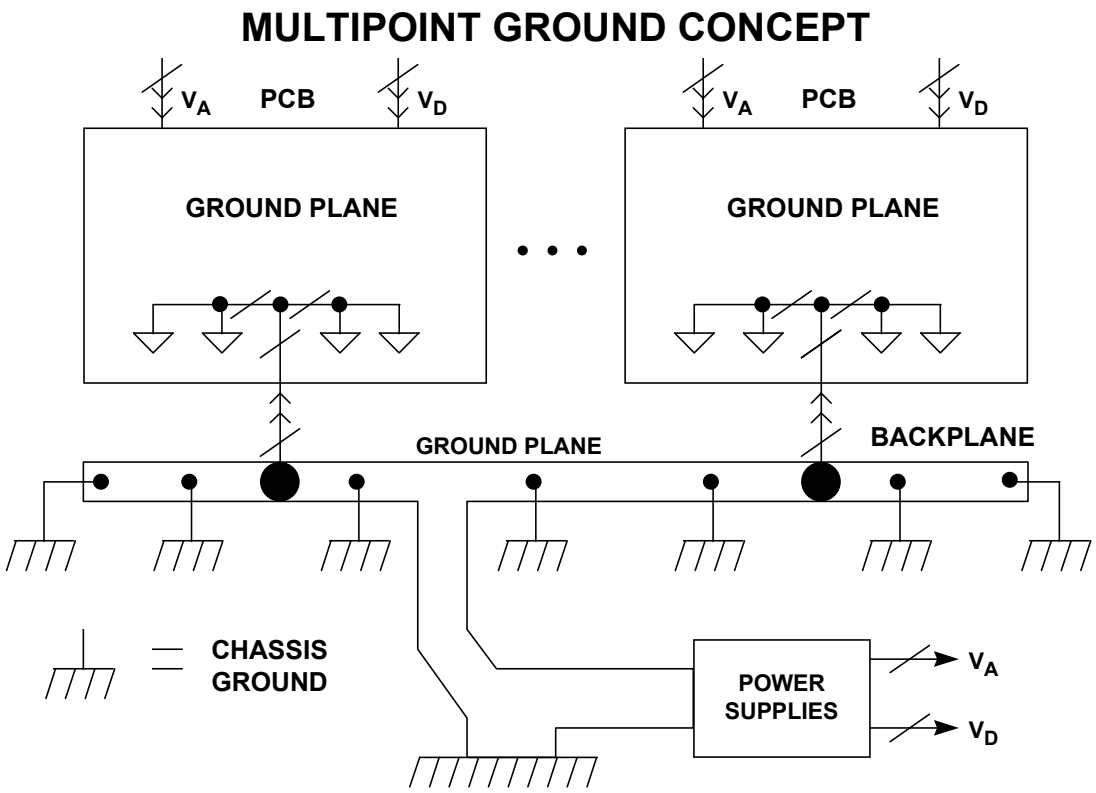

Figure 10.9

The first approach is most often used in all-digital systems, but can be used in mixed-signal systems provided the ground currents due to digital circuits are sufficiently diffused over a large area. The low ground impedance is maintained all the way through the PC boards, the backplane, and ultimately the chassis. However, it is critical that good electrical contact be made where the grounds are connected to the sheet metal chassis. This requires self-tapping sheet metal screws or "biting" washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

The second approach ("star ground") is often used in high speed mixed-signal systems having separate analog and digital ground systems and warrants considerable further discussion.

Separating Analog and Digital Grounds

In mixed-signal systems with large amounts of digital circuitry, it is highly desirable to *physically* separate sensitive analog components from noisy digital components. It may also be beneficial to use separate ground planes for the analog and the digital circuitry. These planes should not overlap in order to minimize capacitive coupling between the two. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground

screens" which are made up of a series of wired interconnections between the connector ground pins. The arrangement shown in Figure 10.10 illustrates that the two planes are kept separate all the way back to a common system "star" ground, generally located at the power supplies. The connections between the ground planes, the power supplies, and the "star" should be made up of multiple bus bars or wide copper brads for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental DC voltage from developing between the two ground systems when cards are plugged and unplugged. Schottky diodes are used because of their low capacitance to prevent coupling between the analog and digital ground planes. However, Schottky diodes begin to conduct at about 300mV, so if the total differential peak-to-peak voltage (the sum of the AC and DC components) between the two ground planes exceeds this value, additional diodes in series should be used.

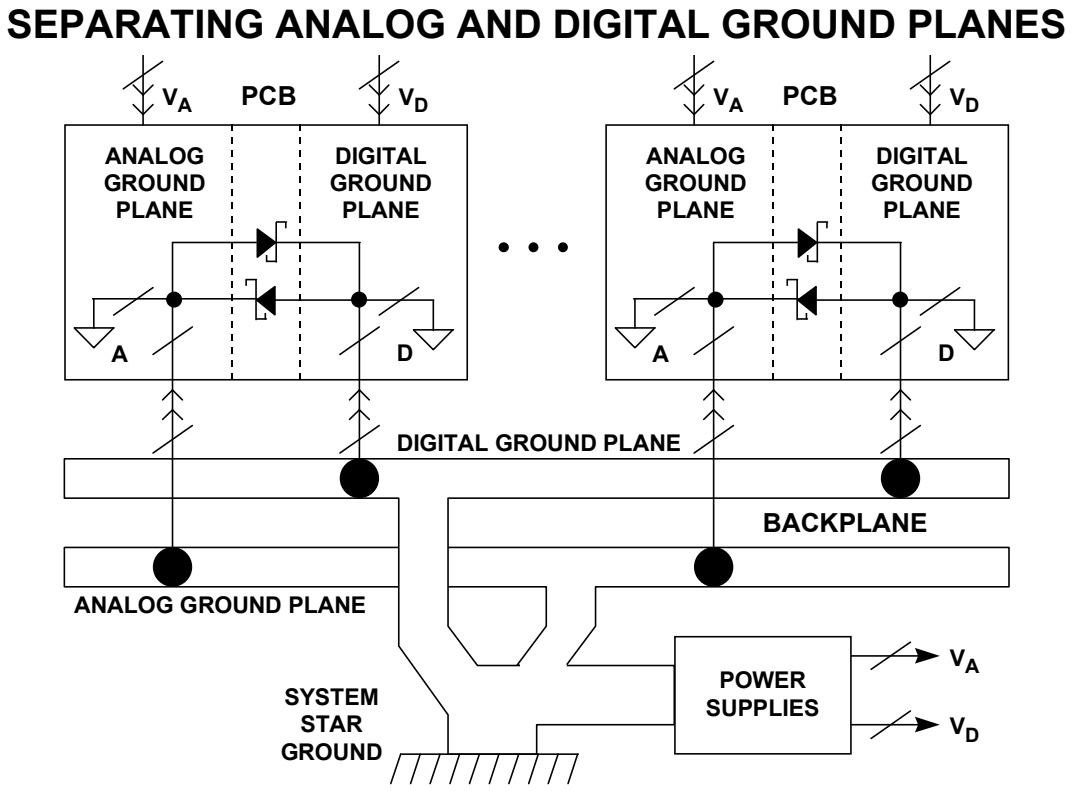

Figure 10.10

Grounding and Decoupling Mixed-Signal ICs

Sensitive analog components such as amplifiers and voltage references are always referenced and decoupled to the analog ground plane. *The ADCs and DACs (and other mixed-signal ICs) should generally be treated as analog components and also grounded and decoupled to the analog ground plane.* At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as *analog ground* (AGND) and *digital ground* (DGND). The diagram shown in Figure 10.11 will help to explain this seeming dilemma.

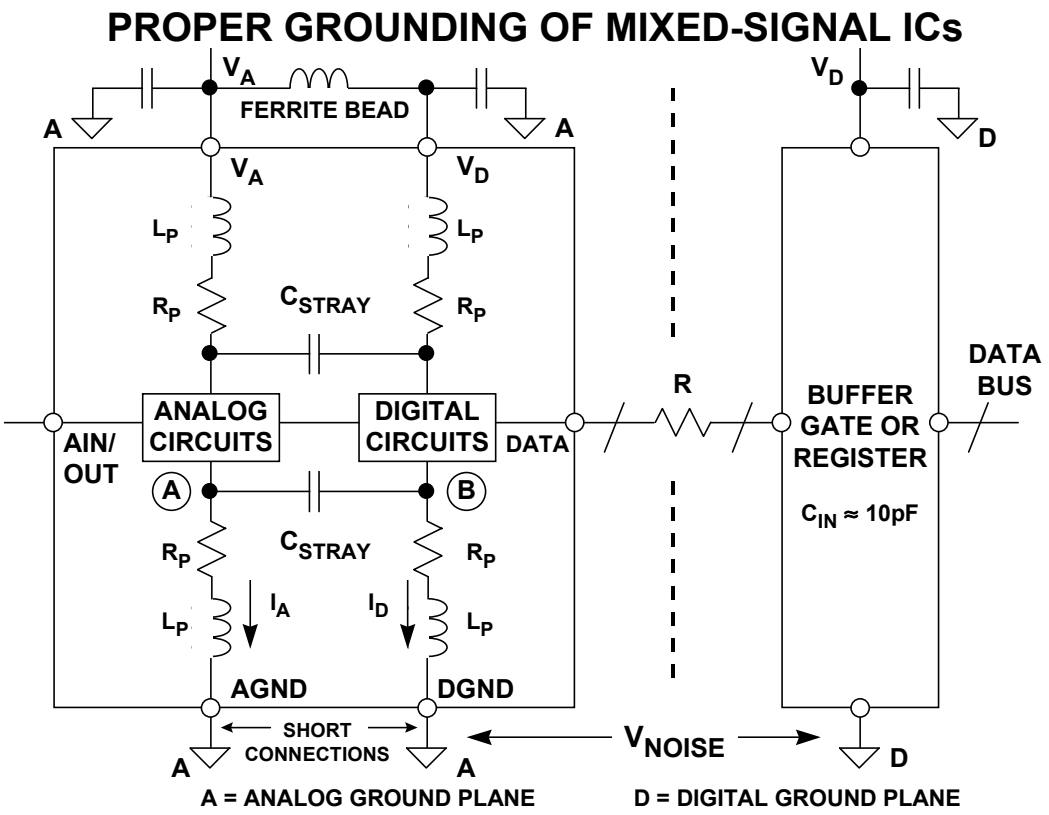

Figure 10.11

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 10.11 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the bond pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance. *Note that connecting DGND to the digital ground plane applies V_{NOISE} across the AGND and DGND pins and invites disaster!*

The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system.

It is true that this arrangement will inject a small amount of digital noise onto the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter output does not drive a large fanout (they normally

can't, by design). Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing and minimize digital switching currents, and thereby reducing any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Figure 10.11. The internal digital currents of the converter will return to ground through the V_D pin decoupling capacitor (mounted as close to the converter as possible) and will not appear in the external ground circuit. These decoupling capacitors should be low inductance ceramic types, typically between 0.01μF and 0.1μF.

Treat the ADC Digital Outputs with Care

It is always a good idea (as shown in Figure 10.11) to place a buffer register adjacent to the converter to isolate the converter's digital lines from noise on the data bus. The register also serves to minimize loading on the digital outputs of the converter and acts as a Faraday shield between the digital outputs and the data bus. Even though many converters have three-state outputs/inputs, this isolation register still represents good design practice.

The series resistors (labeled "R" in Figure 10.11) between the ADC output and the buffer register input help to minimize the digital transient currents which may affect converter performance. The resistors isolate the digital output drivers from the capacitance of the buffer register inputs. In addition, the RC network formed by the series resistor and the buffer register input capacitance acts as a lowpass filter to slow down the fast edges.

A typical CMOS gate combined with PCB trace and through-hole will create a load of approximately 10pF. A logic output slew rate of 1V/ns will produce 10mA of dynamic current if there is no isolation resistor:

$$\Delta I = C\frac{\Delta v}{\Delta t} = 10pF \times \frac{1V}{ns} = 10mA\ .$$

A 500Ω series resistors will minimize this output current and result in a rise and fall time of approximately 11ns when driving the 10pF input capacitance of the register:

$$t_r = 2.2 \times \tau = 2.2 \times R \cdot C = 2.2 \times 500\Omega \times 10pF = 11ns.$$

TTL registers should be avoided, since they can appreciably add to the dynamic switching currents because of their higher input capacitance.

The buffer register and other digital circuits should be grounded and decoupled to the *digital* ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter. The analog ground plane will generally not be very noisy, but if the noise on the digital ground plane (relative to the analog ground plane) exceeds a few hundred millivolts, then steps should be taken to reduce the digital

ground plane impedance, thereby maintaining the digital noise margins at an acceptable level.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane as shown in Figure 10.12. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

In some cases it may not be possible to connect V_D to the analog supply. Some of the newer, high speed ICs may have their analog circuits powered by +5V, but the digital interface powered by +3V to interface to 3V logic. In this case, the +3V pin of the IC should be decoupled directly to the analog ground plane. It is also advisable to connect a ferrite bead in series with power trace that connects the pin to the +3V digital logic supply.

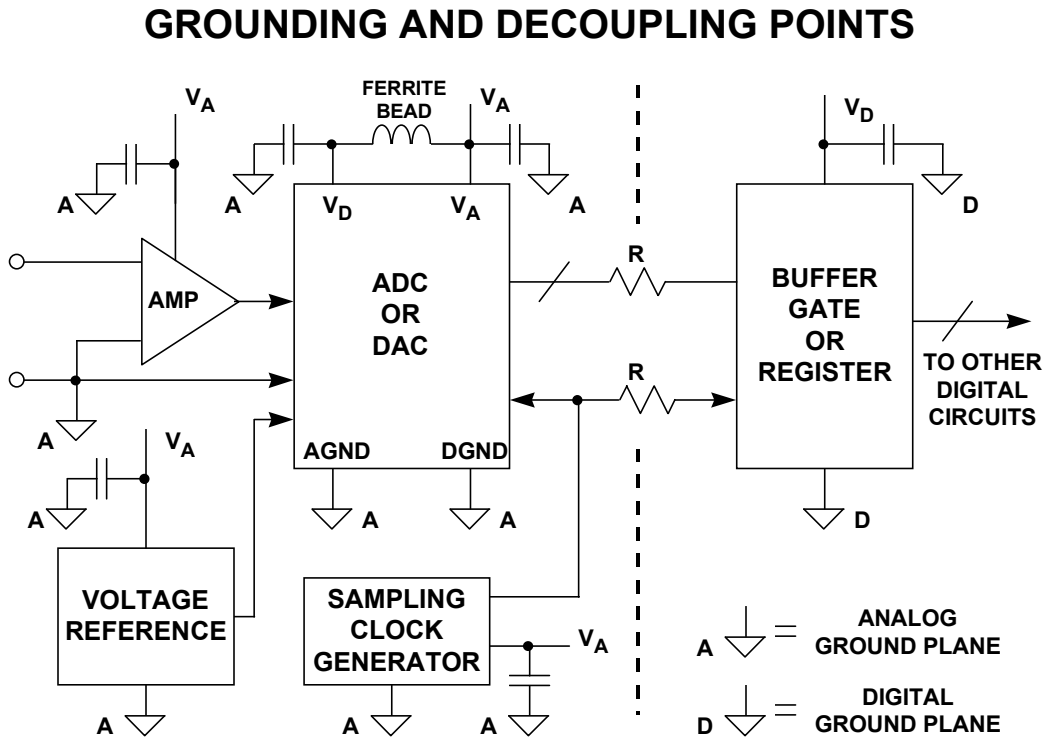

Figure 10.12

The sampling clock generation circuitry should be treated like analog circuitry and also be grounded and heavily-decoupled to the analog ground plane. Phase noise on the sampling clock produces degradation in system SNR as will be discussed shortly.

The Origins of the Confusion about Mixed-Signal Grounding: Applying Single-Card Grounding Concepts to Multicard Systems

Most ADC, DAC, and other mixed-signal device data sheets discuss grounding relative to a single PCB, usually the manufacturer's own evaluation board. This has been a source of confusion when trying to apply these principles to multicard or multi-ADC/DAC systems. The recommendation is usually to split the PCB ground plane into an analog one and a digital one. It is then further recommended that the AGND and DGND pins of a converter be tied together and that the analog ground plane and digital ground planes be connected at that same point. This essentially creates the system "star" ground at the mixed-signal device. While this approach will generally work in a simple system with a single PCB and single ADC/DAC, it is not optimum for multicard mixed-signal systems. In systems having several ADCs or DACs on different PCBs (or on the same PCB, for that matter), the analog and digital ground planes become connected at several points, creating the possibility of ground loops and making a single-point "star" ground system impossible. These ground loops can also occur if there is more than one mixed-signal device on a single PCB. For these reasons, this grounding approach is not recommended for multicard systems, and the approach previously discussed should be used.

Sampling Clock Considerations

In a high performance sampled data system a low phase-noise crystal oscillator should be used to generate the ADC (or DAC) sampling clock because sampling clock jitter modulates the analog input/output signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

The effect of sampling clock jitter on ADC Signal-to-Noise Ratio (SNR) is given approximately by the equation:

$$\mathrm{SNR} = 20\log_{10}\left[\frac{1}{2\pi f t_j}\right],$$

where SNR is the SNR of a perfect ADC of infinite resolution where the only source of noise is that caused by the RMS sampling clock jitter, t_j. Note that f in the above equation is the analog input frequency. Just working through a simple example, if t_j = 50ps RMS, f = 100kHz, then SNR = 90dB, equivalent to about 15-bits dynamic range.

It should be noted that t_j in the above example is the root-sum-square (RSS) value of the external clock jitter *and* the internal ADC clock jitter (called aperture jitter). However, in most high performance ADCs, the internal aperture jitter is negligible compared to the jitter on the sampling clock.

Since degradation in SNR is primarily due to external clock jitter, steps must be taken to ensure the sampling clock is as noise-free as possible and has the lowest possible phase jitter. This requires that a crystal oscillator be used. There are several manufacturers of small crystal oscillators with low jitter (less than 5ps

RMS) CMOS compatible outputs. (For example, MF Electronics, 10 Commerce Dr., New Rochelle, NY 10801, Tel. 914-576-6570.)

Ideally, the sampling clock crystal oscillator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multi-purpose system clock which is generated on the digital ground plane. It must then pass from its origin on the digital ground plane to the ADC on the analog ground plane. Ground noise between the two planes adds directly to the clock signal and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics. This can be remedied somewhat by transmitting the sampling clock signal as a differential signal using either a small RF transformer as shown in Figure 10.13 or a high speed differential driver and receiver IC. If an active differential driver and receiver are used, they should be ECL to minimize phase jitter. In a single +5V supply system, ECL logic can be connected between ground and +5V (PECL), and the outputs AC coupled into the ADC sampling clock input. In either case, the original master system clock must be generated from a low phase noise crystal oscillator.

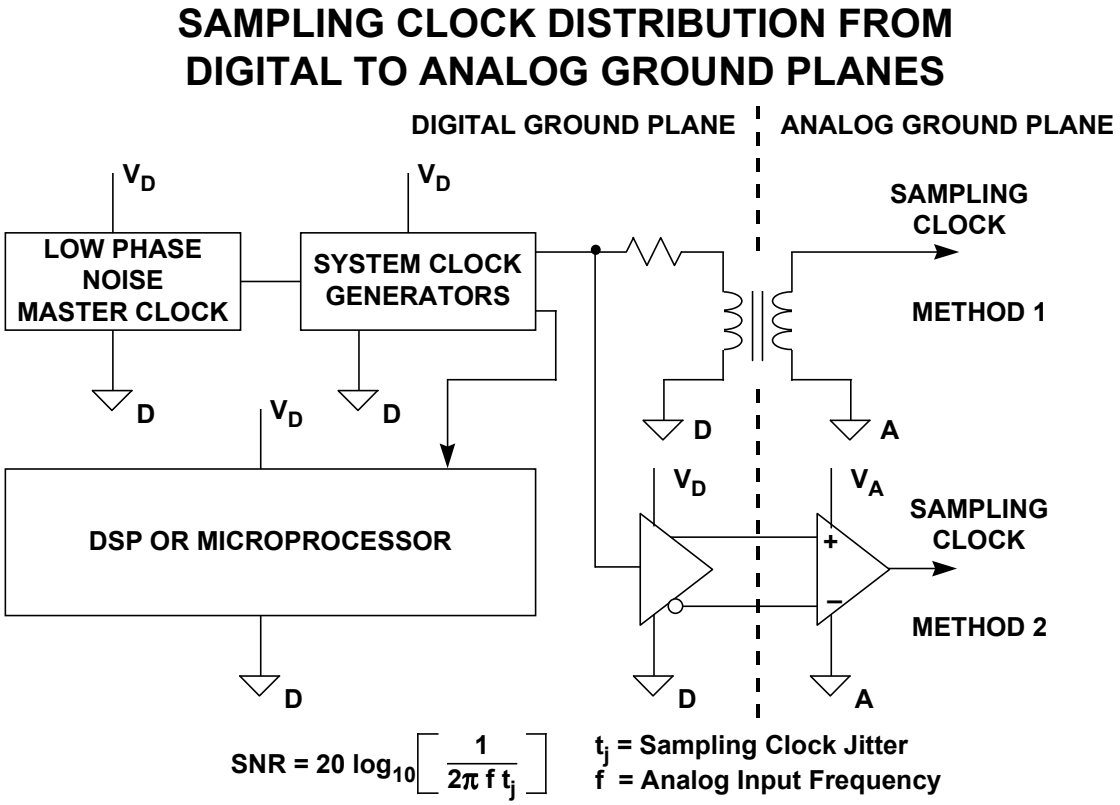

Figure 10.13

Some PC Board Layout Guidelines for Mixed-Signal Systems

It is evident that noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

The ground plane can act as a shield where sensitive signals cross. Figure 10.14 shows a good layout for a data acquisition board where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

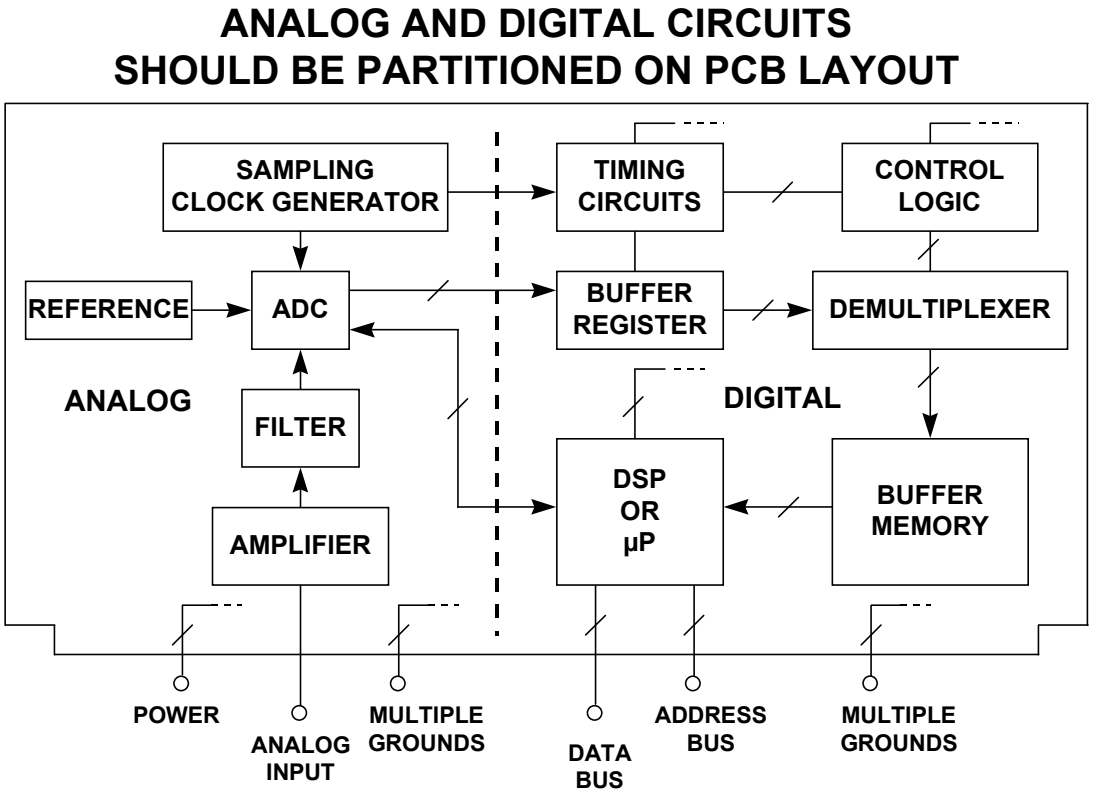

Figure 10.14

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run in parallel - it is therefore imperative to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10mΩ) when the board is new - as the board gets older the contact resistance is likely to

rise, and the board's performance may be compromised. It is therefore well worthwhile to allocate extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

Manufacturers of high performance mixed-signal ICs like Analog Devices offer evaluation boards to assist customers in their initial evaluations and layout. ADC evaluation boards generally contain an on-board low-jitter sampling clock oscillator, output registers, and appropriate power and signal connectors. They also may have additional support circuitry such as the ADC input buffer amplifier and external reference.

The layout of the evaluation board is optimized in terms of grounding, decoupling, and signal routing and can be used as a model when laying out the ADC PC board in the system. The actual layout is usually available from the ADC manufacturer in the form of computer CAD files (Gerber files).

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12. Ralph Morrison, **Solving Interference Problems in Electronics**, John Wiley, 1995.

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POWER SUPPLY NOISE REDUCTION AND FILTERING

Walt Jung, Walt Kester, Bill Chestnut

Precision analog circuitry has traditionally been powered from well regulated, low noise linear power supplies. During the last decade however, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight.

In spite of these benefits, switchers *do* have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20kHz to 1MHz, the spikes can contain frequency components extending to 100MHz or more. While specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the *peak* (or p-p) amplitudes of the switching spikes, at the output loading of your system.

The following section discusses filter techniques for rendering a switching regulator output *analog ready*, that is sufficiently quiet to power precision analog circuitry with relatively small loss of DC terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes various DC-DC converters as well as popular 5V (PC type) supplies.

An understanding of the EMI process is necessary to understand the effects of supply noise on analog circuits and systems. Every interference problem has a *source*, a *path*, and a *receptor* [Reference 1]. In general, there are three methods for dealing with interference. First, source emissions can be minimized by proper layout, pulse-edge rise time control/reduction, filtering, and proper grounding. Second, radiation and conduction paths should be reduced through shielding and physical separation. Third, receptor immunity to interference can be improved, via supply and signal line filtering, impedance level control, impedance balancing, and utilizing differential techniques to reject undesired common-mode signals. This section focuses on reducing switching power supply noise with external post filters.

Tools useful for combating high frequency switcher noise are shown by Figure 10.15. They differ in electrical characteristics as well as practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small in size.

SWITCHING REGULATOR NOISE REDUCTION TOOLS

- **Capacitors**
- **Inductors**
- **Ferrites**
- **Resistors**
- **Linear Post Regulation**
- **Proper Layout and Grounding Techniques**
- **PHYSICAL SEPARATION FROM SENSITIVE ANALOG CIRCUITS!!**

Figure 10.15

Capacitors are probably the single most important filter component for switchers. There are many different types of capacitors, and an understanding of their individual characteristics is absolutely mandatory to the design of effective practical supply filters. There are generally three classes of capacitors useful in 10kHz-100MHz filters, broadly distinguished as the generic dielectric types; *electrolytic*, organic, *film*, and *ceramic*. These can in turn can be further sub-divided. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 10.16.

TYPES OF CAPACITORS

	Aluminum Electrolytic (General Purpose)	Aluminum Electrolytic (Switching Type)	Tantalum Electrolytic	OS-CON Electrolytic	Polyester (Stacked Film)	Ceramic (Multilayer)
Size	100 µF	120 µF	120 µF	100 µF	1 µF	0.1 µF
Rated Voltage	25 V	25 V	20 V	20 V	400 V	50 V
ESR	0.6 Ω @ 100 kHz	0.18 Ω @ 100 kHz	0.12 Ω @ 100 kHz	0.02 Ω @ 100 kHz	0.11 Ω @ 1 MHz	0.12 Ω @ 1 MHz
Operating Frequency (*)	≅ 100 kHz	≅ 500 kHz	≅ 1 MHz	≅ 1 MHz	≅ 10 MHz	≅ 1 GHz

(*) Upper frequency strongly size and package dependent

Figure 10.16

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from capacitive to inductive. This varies from as low as 10kHz in some electrolytics to as high as 100MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general purpose aluminum electrolytic* types, available in working voltages from below 10V up to about 500V, and in size from 1 to several thousand μF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They also have relatively high leakage currents (up to tens of μA, and strongly dependent upon design specifics).

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100V or less, with capacitance of up to 500μF [Reference 3]. In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 4]. This capacitor type competes directly with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte [Reference 5]. The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of low low-temperature ESR degradation.

Film capacitors are available in a very broad range of values and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10μF/50V polyester capacitor (for example) is actually the size of your hand. Metalized (as opposed to foil) electrodes do help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10mΩ or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

Film capacitors using a wound layer-type construction can be inductive. This can limit their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see References 4, 5, 6]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 7].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10MHz. At the highest frequencies, only stacked film types should be considered. Some manufacturers are now supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several µF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200V [see ceramic families of Reference 3]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). NP0 types are limited to values of 0.1µF or less, with 0.01µF representing a more practical upper limit.

Multilayer ceramic "chip caps" are very popular for bypassing/ filtering at 10MHz or higher, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

All capacitors have some finite ESR. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying "free" damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted by the impedance vs. frequency plot. This occurs where |Z| falls to a minimum level, nominally equal to the capacitor's ESR at that frequency. This low Q resonance can generally cover a relatively wide frequency range of several octaves. Contrasted to the very high Q sharp resonances of film and ceramic caps, the low Q behavior of electrolytics can be useful in controlling resonant peaks.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4-6 times at –55°C vs. the room temperature value. For circuits where ESR is critical to performance, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the –10°C ESR at 100kHz is no more than 2× that at room temperature. The OSCON electrolytics have a ESR vs. temperature characteristic which is relatively flat.

As noted, all real capacitors have parasitic elements which limit their performance. The equivalent electrical network representing a real capacitor models both ESR and ESL as well as the basic capacitance, plus some shunt resistance (see Figure 10.17). In such a practical capacitor, at low frequencies the net impedance is almost purely capacitive. At intermediate frequencies, the net impedance is determined by ESR, for example about 0.12Ω to 0.4Ω at 125kHz, for several types. Above about 1MHz these capacitor types become inductive, with impedance dominated by the effect of ESL. All electrolytics will display impedance curves similar in general shape to that of Figure 10.18. The minimum impedance will vary with the ESR, and the inductive region will vary with ESL (which in turn is strongly effected by package style).

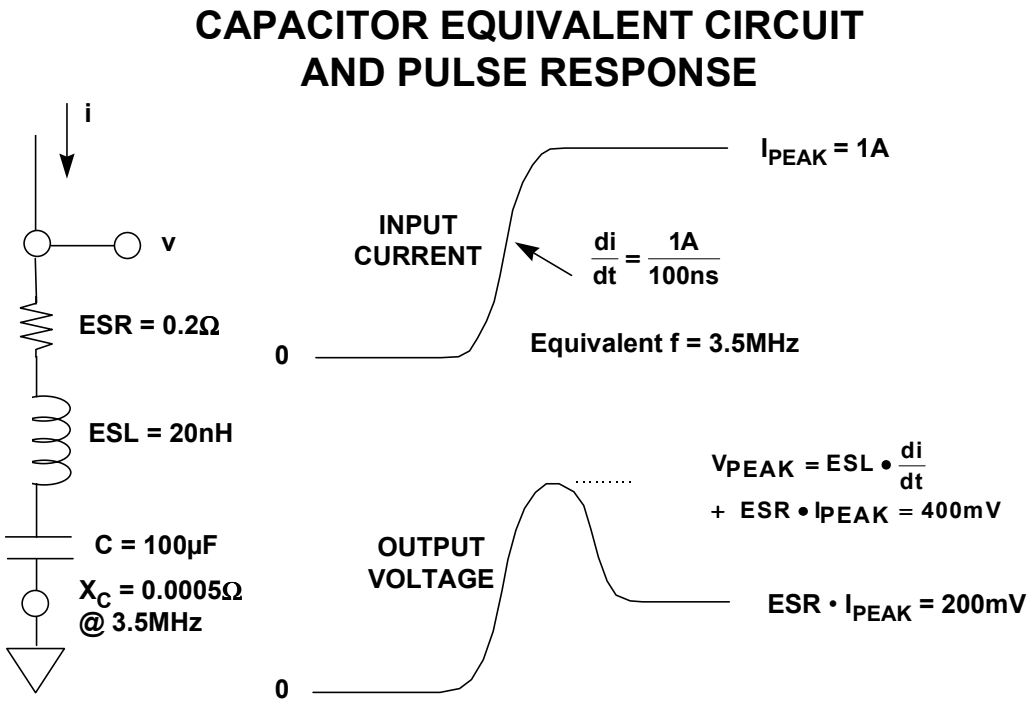


Figure 10.17

Regarding inductors, *Ferrites* (non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are extremely useful in power supply filters [Reference 9]. At low frequencies (<100kHz), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100kHz, ferrites become resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, DC bias current, number of turns, size, shape, and temperature. Figure 10.19 summarizes a number of ferrite characteristics, and Figure 10.20 shows the impedance characteristic of several ferrite beads from Fair-Rite (http://www.fair-rite.com).

ELECTROLYTIC CAPACITOR IMPEDANCE VERSUS FREQUENCY

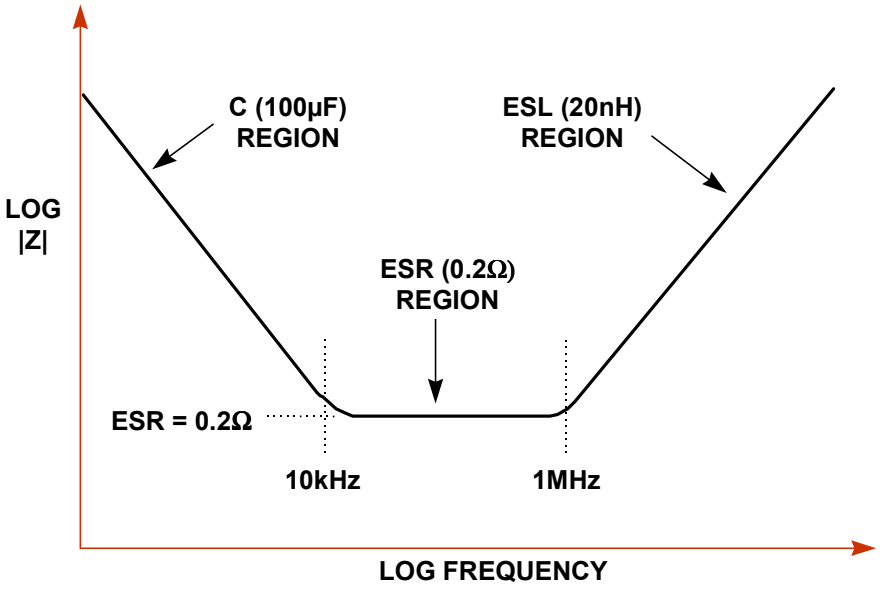
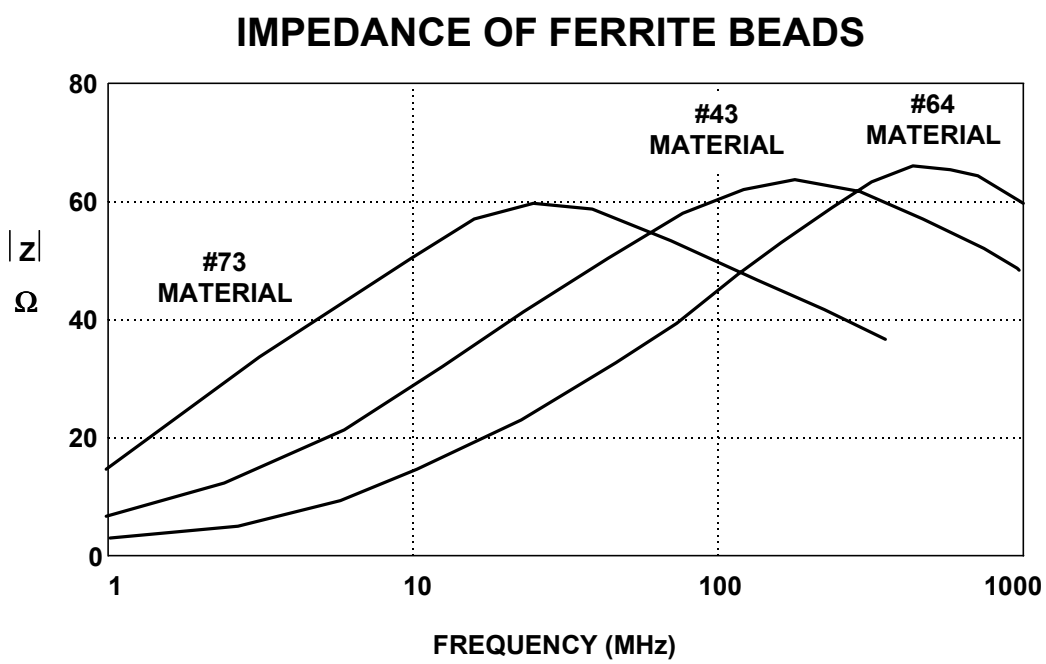


Figure 10.18

FERRITES SUITABLE FOR HIGH FREQUENCY FILTERS

- Ferrites Good for Frequencies Above 25kHz
- Many Sizes and Shapes Available Including Leaded "Resistor Style"
- Ferrite Impedance at High Frequencies Primarily Resistive -- Ideal for HF Filtering
- Low DC Loss: Resistance of Wire Passing Through Ferrite is Very Low
- High Saturation Current Versions Available
- Choice Depends Upon:
  - Source and Frequency of Interference
  - Impedance Required at Interference Frequency
  - Environmental: Temperature, AC and DC Field Strength, Size / Space Available
- Always Test the Design!

Figure 10.19



Courtesy: Fair-Rite Products Corp, Wallkill, NY
(http://www.fair-rite.com)

Figure 10.20

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 10 and 11). A simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, pre-mounted on a length of wire and used as a component (see Reference 11). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount beads are also available.

PSpice ferrite models for Fair-Rite materials are available, and allow ferrite impedance to be estimated [see Reference 12]. These models have been designed to match measured impedances rather than theoretical impedances.

A ferrite's impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the peak DC current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with some experimentation with the actual filter connected to the supply output under system load conditions, should lead to a proper ferrite selection.

Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switcher's DC output to produce an *analog ready* 5V supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies. A basic stage can be used to carry all of the DC load current, and filter noise by 60dB or more up to a 1-10MHz range. This larger filter is used as a *card entry filter* providing broadband filtering for all power entering a PC card. Smaller, more simple local filter stages are also used to provide higher frequency decoupling right at the power pins of individual stages.

Switching Regulator Experiments

In order to better understand the challenge of filtering switching regulators, a series of experiments were conducted with a representative device, the ADP1148 synchronous buck regulator with a 9V input and a 3.3V/1A output.

In addition to observing typical input and output waveforms, the objective of these experiments was to reduce the output ripple to less than 10mV peak-to-peak, a value suitable for driving most analog circuits.

Measurements were made using a Tektronix wideband digitizing oscilloscope with the input bandwidth limited to 20MHz so that the ripple generated by the switching regulators could be more readily observed. In a system, power supply ripple frequencies above 20MHz are best filtered locally at each IC power pin with a low inductance ceramic capacitor and perhaps a series-connected ferrite bead.

Probing techniques are critical for accurate ripple measurements. A standard passive 10X probe was used with a "bayonet" probe tip adapter for making the ground connection as short as possible (see Figure 10.21). Use of the "ground clip lead" is not recommended in making this type of measurement because the lead length in the ground connection forms an unwanted inductive loop which picks up high frequency switching noise, thereby corrupting the signal being measured.

Note: Schematic representation of proper physical grounding is almost impossible. In all the following circuit schematics, the connections to ground are made to the ground plane using the shortest possible connecting path, regardless of how they are indicated in the actual circuit schematic diagram.

The circuit for the ADP1148 9V to 3.3V/1A buck regulator is shown in Figure 10.22. The output waveform of the ADP1148 buck regulator is shown in Figure 10.23. The fundamental switching frequency is approximately 150kHz, and the output ripple is approximately 40mV.

Adding an output filter consisting of a 50µH inductor and a 100µF leaded tantalum capacitor reduced the ripple to approximately 3mV.

PROPER PROBING TECHNIQUES

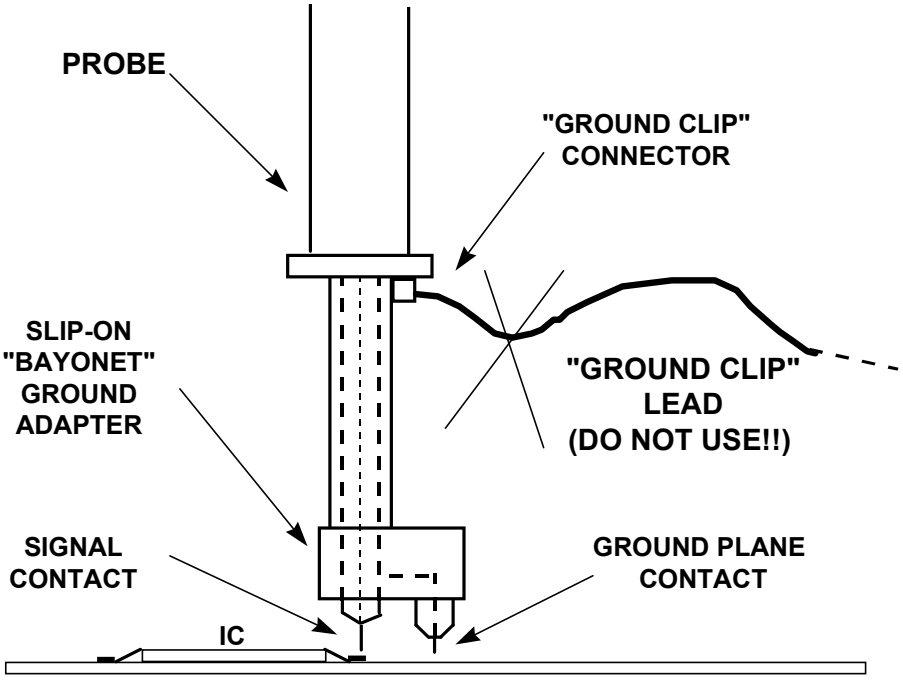


Figure 10.21

ADP1148 BUCK REGULATOR CIRCUIT

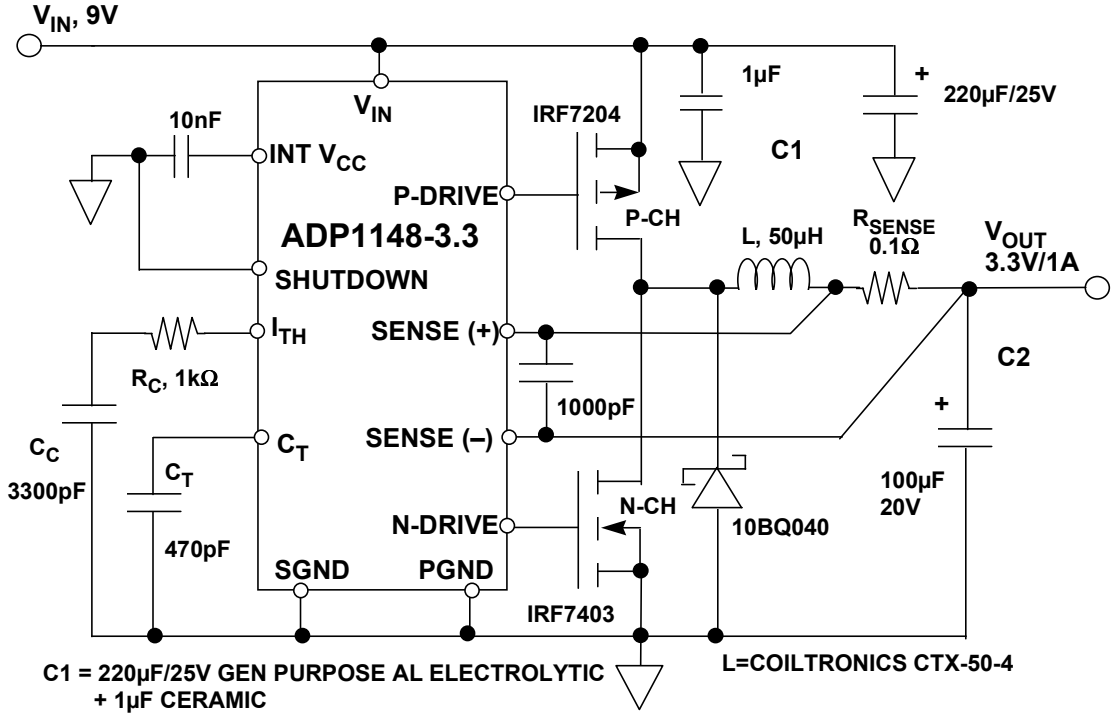
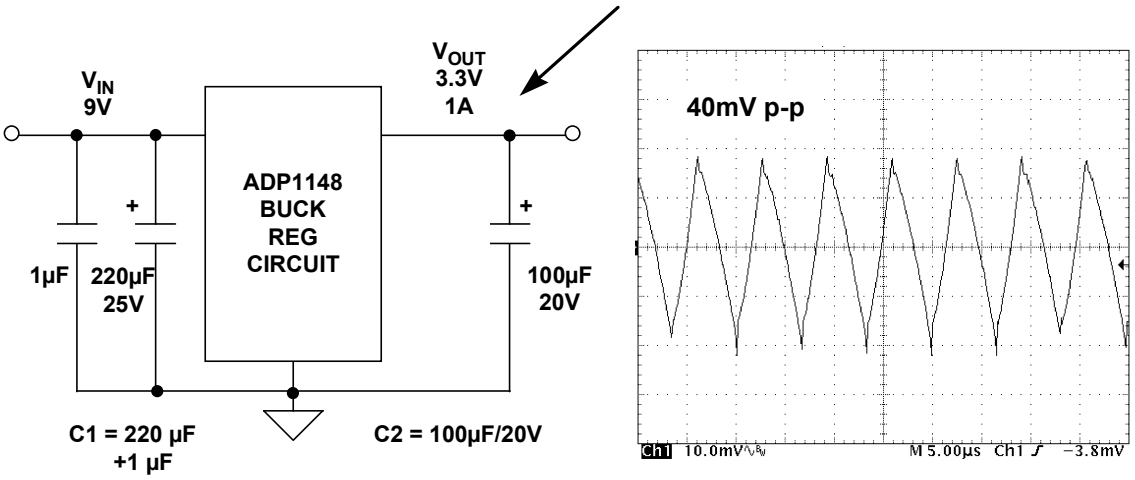


Figure 10.22

ADP1148 BUCK OUTPUT WAVEFORM

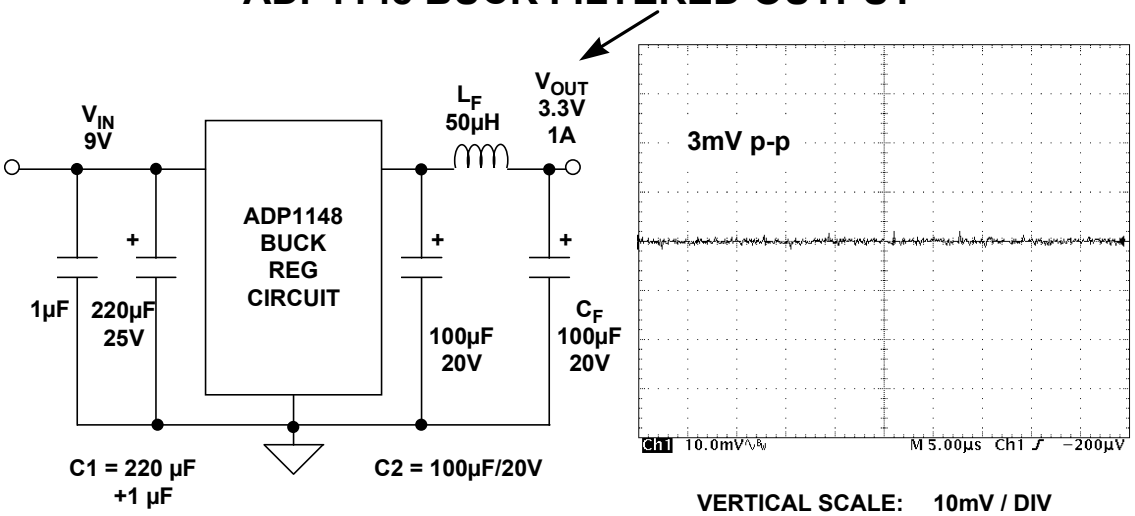


VERTICAL SCALE: 10mV / DIV
HORIZ. SCALE: 5µs / DIV

C1 = 1µF CERAMIC + 220µF/25V GENERAL PURPOSE AL ELECTROLYTIC
C2 = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES (ESR = 0.6Ω)

Figure 10.23

ADP1148 BUCK FILTERED OUTPUT



VERTICAL SCALE: 10mV / DIV
HORIZ. SCALE: 5µs / DIV

C1 = 1µF CERAMIC + 220µF/25V GENERAL PURPOSE AL ELECTROLYTIC
C2 = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES (ESR = 0.6Ω)

OUTPUT FILTER
L_F=COILTRONICS CTX-50-4
C_F = 100µF/20V LEADED TANTALUM, KEMET T356-SERIES

Figure 10.24

Linear regulators are often used following switching regulators for better regulation and lower noise. Low dropout (LDO) regulators such as the ADP3310 are desirable in these applications because they require only a small input-to-output series

voltage to maintain regulation. This minimizes power dissipation in the pass device and may eliminate the need for a heat sink. Figure 10.25 shows the ADP1148 buck regulator configured for a 9V input and a 3.75V/1A output. The output drives an ADP3310 linear LDO regulator configured for 3.75V input and 3.3V/1A output. The input and output of the ADP3310 is shown in Figure 10.26. Notice that the regulator reduces the ripple from 40mV to approximately 5mV.

ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

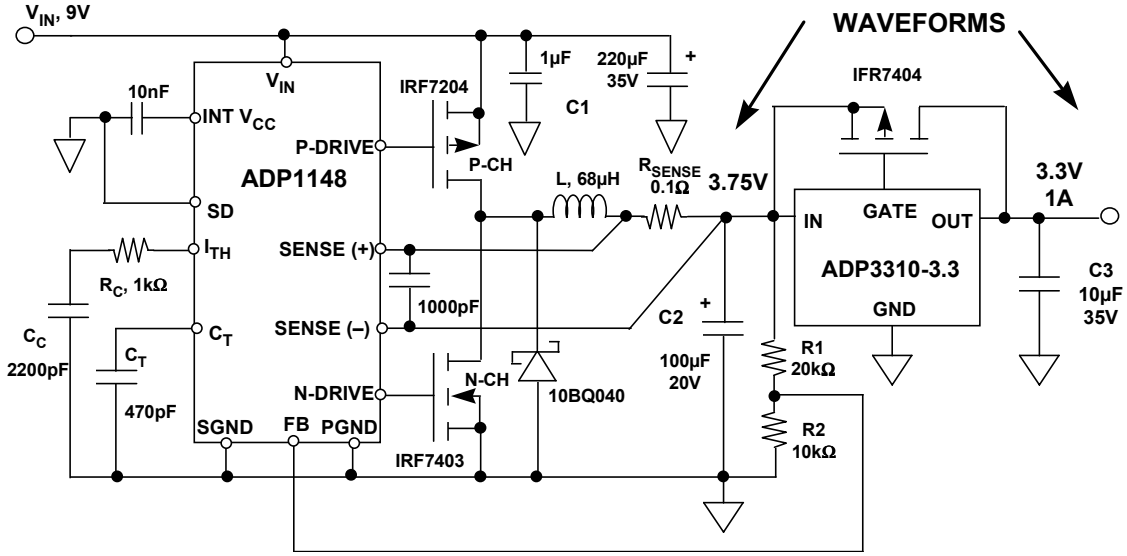
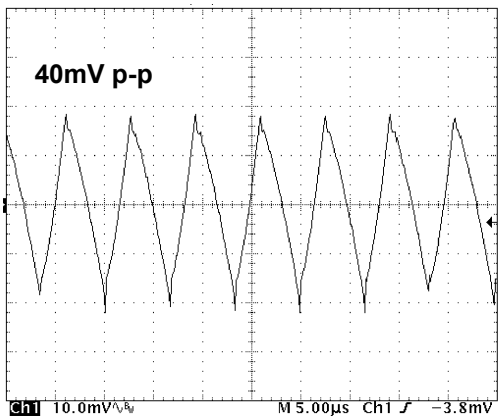


Figure 10.25

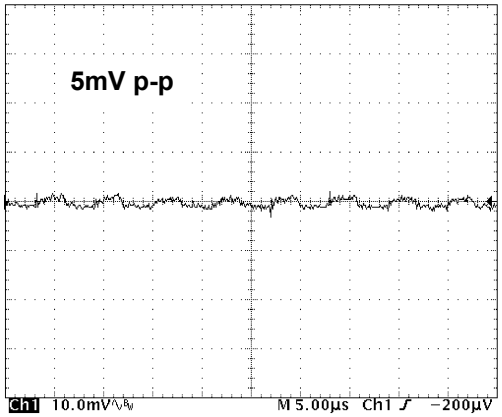
WAVEFORMS FOR ADP1148 BUCK REGULATOR DRIVING ADP3310 LOW DROPOUT REGULATOR

ADP1148 OUTPUT (ADP3310 INPUT)



VERTICAL SCALE: 10mV/DIV
HORIZ. SCALE: 5µs/DIV

ADP3310 OUTPUT



VERTICAL SCALE: 10mV/DIV
HORIZ. SCALE: 5µs/DIV

Figure 10.26

There are many tradeoffs in designing power supply filters. The success of any filter circuit is highly dependent upon a compact layout and the use of a large area ground plane. As has been stated earlier, all connections to the ground plane should be made as short as possible to minimize parasitic resistance and inductance.

Output ripple can be reduced by the addition of low ESL/ESR capacitors to the output. However, it may be more efficient to use an LC filter to accomplish the ripple reduction. In any case, proper component selection is critical. The inductor should not saturate under the maximum load current, and its DC resistance should be low enough as not to induce significant voltage drop. The capacitors should have low ESL and ESR and be rated to handle the required ripple current.

Low dropout linear post regulators provide both ripple reduction as well as better regulation and can be effective, provided the sacrifice in efficiency is not excessive.

Finally, it is difficult to predict the output ripple current analytically, and there is no substitute for a prototype using the real-world components. Once the filter is proven to provide the desired ripple attenuation (with some added safety margin), care must be taken that parts substitutions or vendor changes are not made in the final production units without first testing them in the circuit for equivalent performance.

SWITCHING SUPPLY FILTER SUMMARY

- **Proper Layout and Grounding (using Ground Plane) Mandatory**
- **Low ESL/ESR Capacitors Give Best Results**
- **Parallel Capacitors Lower ESR/ESL and Increase Capacitance**
- **External LC Filters Very Effective in Reducing Ripple**
- **Linear Post Regulation Effective for Noise Reduction and Best Regulation**
- **Completely Analytical Approach Difficult, Prototyping is Required for Optimum Results**
- **Once Design is Finalized, Do Not Switch Vendors or Use Parts Substitutions Without First Verifying Their Performance in Circuit**
- **High Frequency Localized Decoupling at IC Power Pins is Still Required**

Figure 10.27

Localized High Frequency Power Supply Filtering

The LC filters described in the previous section are useful in filtering switching regulator outputs. However, it may be desirable to place similar filters on the individual PC boards where the power first enters the board. Of course, if the switching regulator is placed on the PC board, then the LC filter should be an integral part of the regulator design.

Localized high frequency filters may also be required at each IC power pin (see Figure 10.28). Surface mount ceramic capacitors are ideal choices because of their low ESL. It is important to make the connections to the power pin and the ground plane as short as possible. In the case of the ground connection, a via directly to the ground plane is the shortest path. Routing the capacitor ground connection to another ground pin on the IC is not recommended due to the added inductance of the trace. In some cases, a ferrite bead in series with the power connection may also be desirable.

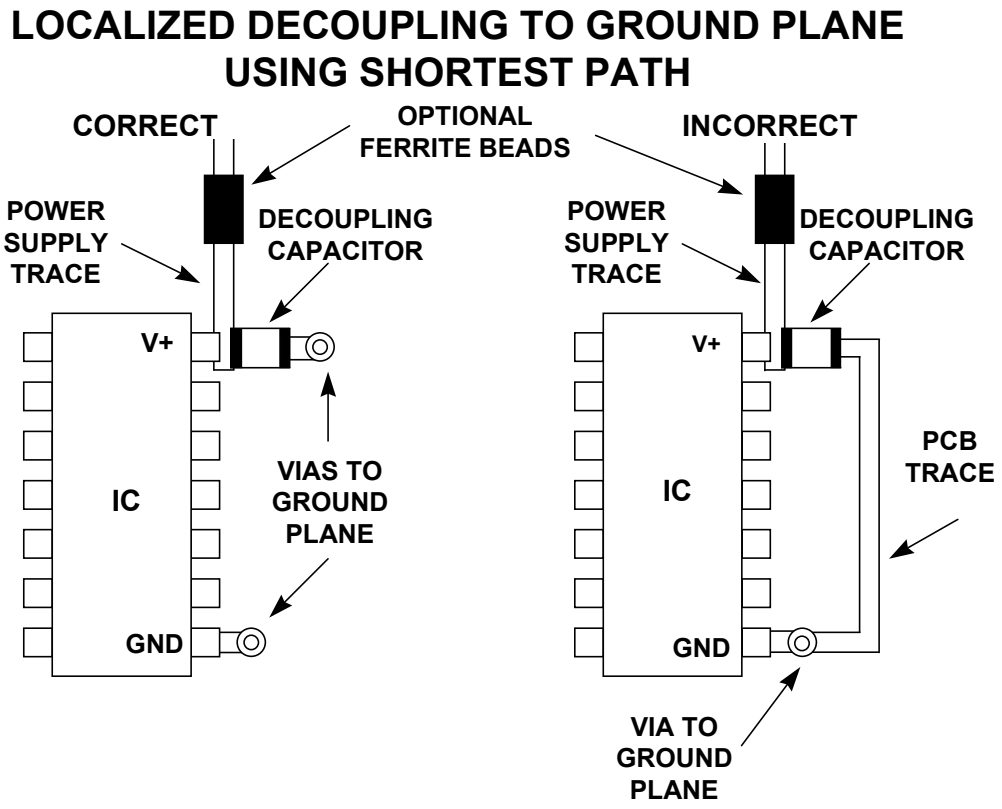


Figure 10.28

The following list summarizes the switching power supply filter layout/construction guidelines which will help ensure that the filter does the best possible job:

(1) *Pick the highest electrical value and voltage rating for filter capacitors which is consistent with budget and space limits. This minimizes ESR, and maximizes filter performance. Pick chokes for low ΔL at the rated DC current, as well as low DCR.*

(2) *Use short and wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mils for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance.*

(3) *Use short leads or better yet,* leadless *components, to minimize lead inductance. This minimizes the tendency to add excessive ESL and/or ESR. Surface mount packages are preferred. Make all connections to the ground plane as short as possible.*

(4) *Use a large-area ground plane for minimum impedance.*

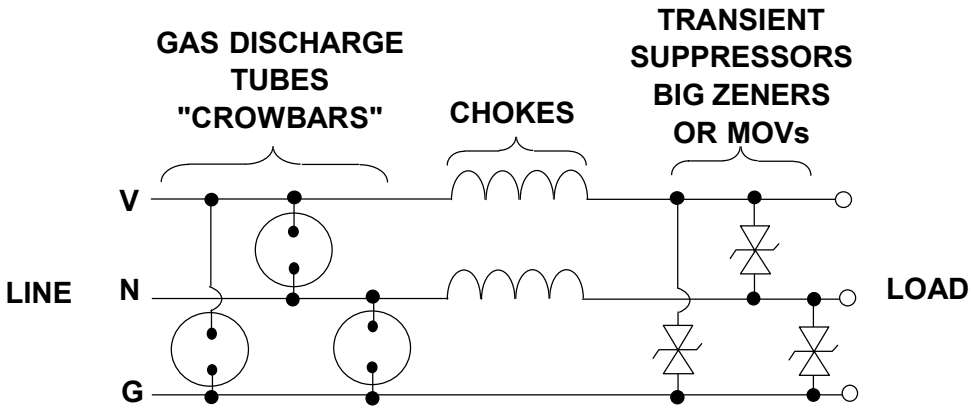
(5) *Know what your components do over frequency, current and temperature variations! Make use of vendor component models for the simulation of prototype designs, and make sure that lab measurements correspond reasonably with the simulation. While simulation is not* absolutely *necessary, it does instill confidence in a design when correlation is achieved* (see Reference 15).

Filtering the AC Power Lines

The AC power line can also be an EMI entry/exit path! To remove this noise path and reduce emissions caused by the switching power supply or other circuits, a *power line filter* is required.

Figure 10.29 is an example of a hybrid power transient protection network commonly used in many applications where lightning transients or other power-line disturbances are prevalent. These networks can be designed to provide protection against transients as high as 10kV and as fast as 10ns. Gas discharge tubes (crowbars) and large geometry zener diodes or Transient Voltage Suppressers (TVSs) are used to provide both differential and common-mode protection. Metal-oxide varistors (MOVs) can be substituted for the zener diodes or TVSs in less critical, or in more compact designs. Chokes are used to limit the surge current until the gas discharge tubes fire.

POWER LINE DISTURBANCES CAN GENERATE EMI



■ **COMMON-MODE AND DIFFERENTIAL MODE PROTECTION**

Figure 10.29

Commercial EMI filters, as illustrated in Figure 10.30, can be used to filter less catastrophic transients or high-frequency interference. These EMI filters provide both common-mode and differential mode filtering. An optional choke in the safety ground can provide additional protection against common-mode noise. The value of

this choke cannot be too large, however, because its resistance may affect power-line fault clearing. These filters work in both directions: they not only protect the equipment from surges on the power line but also prevent transients from the internal switching power supplies from corrupting the power line.

SCHEMATIC FOR A COMMERCIAL POWER LINE FILTER

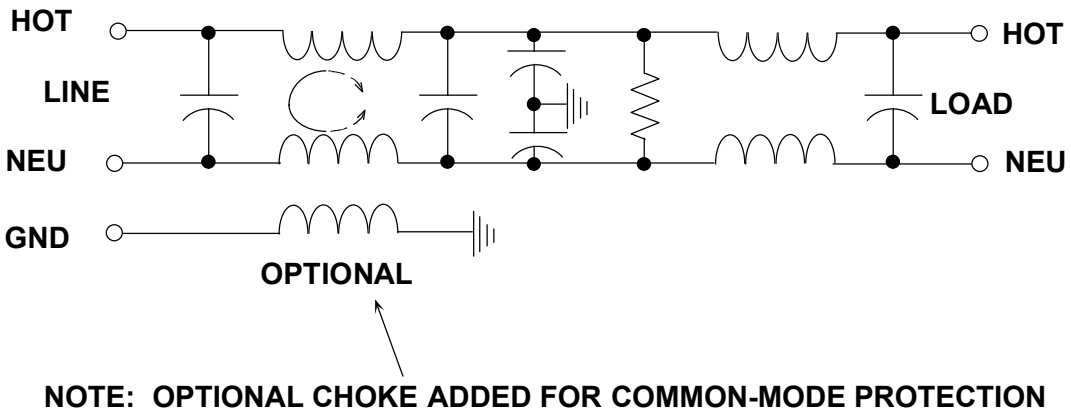


Figure 10.30

Transformers provide the best common-mode power line isolation. They provide good protection at low frequencies (<1MHz), and for transients with rise and fall times greater than 300ns. Most motor noise and lightning transients are in this range, so isolation transformers work well for these types of disturbances. Although the isolation between input and output is galvanic, isolation transformers do not provide sufficient protection against extremely fast transients (<10ns) or those caused by high-amplitude electrostatic discharge (1 to 3ns). Isolation transformers can be designed for various levels of differential- or common-mode protection. For differential-mode noise rejection, the Faraday shield is connected to the neutral, and for common-mode noise rejection, the shield is connected to the safety ground.

It is important to remember that AC line power can potentially be lethal! Do not experiment without proper equipment and training! All components used in power line filters should be UL approved, and the best way to provide this is to specify a packaged UL approved filter. It should be installed in such a manner that it is the first circuit the AC line sees upon entering the equipment. Standard three wire IEC style line cords are designed to mate with three terminal male connectors integral to many line filters. This is the best way to achieve this function, as it automatically grounds the third wire to the shell of the filter and equipment chassis via a low inductance path.

Commercial power line filters are quite effective in reducing AC power-line noise. This noise generally has both common-mode and differential-mode components. Common-mode noise is noise that is found on any two of the three power connections (black, white, or green) with the same amplitude and polarity. In contrast, differential-mode noise is noise found only between two lines. By design, most commercially available filters address both noise modes (see Reference 16).

REFERENCES: NOISE REDUCTION AND FILTERING

1. **EMC Design Workshop Notes**, Kimmel-Gerke Associates, Ltd., St. Paul, MN. 55108, (612) 330-3728.

2. Walt Jung, Dick Marsh, *Picking Capacitors, Parts 1 & 2*, **Audio,** February, March, 1980.

3. Tantalum Electrolytic and Ceramic Capacitor Families, Kemet Electronics, Box 5928, Greenville, SC, 29606, (803) 963-6300.

4. Type HFQ Aluminum Electrolytic Capacitor and type V Stacked Polyester Film Capacitor, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, (201) 348-7000.

5. OS-CON Aluminum Electrolytic Capacitor 93/94 Technical Book, Sanyo, 3333 Sanyo Road, Forrest City, AK, 72335, (501) 633-6634.

6. Ian Clelland, *Metalized Polyester Film Capacitor Fills High Frequency Switcher Needs*, **PCIM**, June 1992.

7. Type 5MC Metallized Polycarbonate Capacitor, Electronic Concepts, Inc., Box 1278, Eatontown, NJ, 07724, (908) 542-7880.

8. Walt Jung, *Regulators for High-Performance Audio, Parts 1 and 2*, **The Audio Amateur,** issues 1 and 2, 1995.

9. Henry Ott, **Noise Reduction Techniques in Electronic Systems, 2d Ed.,** 1988, Wiley.

10. Fair-Rite Linear Ferrites Catalog, Fair-Rite Products, Box J, Wallkill, NY, 12886, (914) 895-2055, http://www.fair-rite.com.

11. Type EXCEL leaded ferrite bead EMI filter, and type EXC L leadless ferrite bead, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, (201) 348-7000.

12. Steve Hageman, *Use Ferrite Bead Models to Analyze EMI Suppression*, **The Design Center Source,** MicroSim Newsletter**,** January, 1995.

13. Type 5250 and 6000-101K chokes, J. W. Miller, 306 E. Alondra Blvd., Gardena, CA, 90247, (310) 515-1720.

14. DIGI-KEY, PO Box 677, Thief River Falls, MN, 56701-0677, (800) 344-4539.

15. Tantalum Electrolytic Capacitor SPICE Models, Kemet Electronics, Box 5928, Greenville, SC, 29606, (803) 963-6300.

16. Eichhoff Electronics, Inc., 205 Hallene Road, Warwick, RI., 02886, (401) 738-1440, http://www.eichhoff.com.

17. Practical Design Techniques for Power and Thermal Management, Analog Devices, 1998, Chapter 8.

PREVENTING RFI RECTIFICATION
Walt Kester, Walt Jung, Chuck Kitchin

High frequency radio frequency interference (RFI) can seriously affect the DC performance of high accuracy circuits. Because of their relatively low bandwidth, precision operational amplifiers and instrumentation amplifiers will not accurately amplify RF signals in the MHz range. However, if these out-of-band signals are allowed to couple into the precision amplifier through either its input, output, or power supply pins, they can be rectified by various junctions in the amplifier and ultimately cause an unexplained and unwanted DC offset at the output. An excellent analysis of the phenomenon is found in Reference 1, but the purpose here is to show how proper filtering can be used to minimize or prevent these errors.

We have previously discussed how proper power supply decoupling techniques will minimize RFI on the IC power pins. Further discussion is required with respect to the amplifier inputs and outputs.

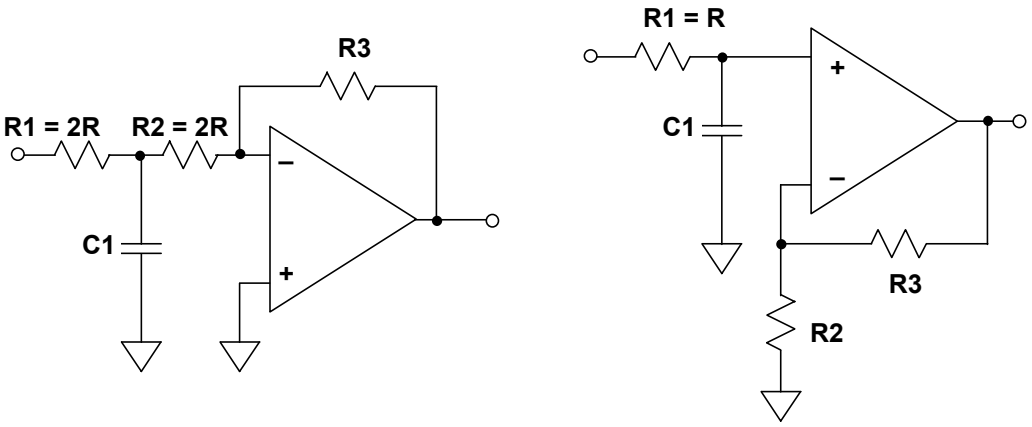
The best way to prevent rectification due to input RFI is to use a filter located close to the op amp input as shown in Figure 10.31. In the case of the inverting op amp, the filter capacitor C1 is placed between R1 and R2. The DC closed loop gain of the circuit is –R3/(R1+R2). C1 is not connected directly to the inverting input of the op amp because that would result in instability. The filter bandwidth is chosen to be at least 100 times larger than the actual signal bandwidth to prevent signal attenuation. For the non-inverting configuration, the filter capacitor can be connected directly to the op amp input as shown.

It should be noted that a ferrite bead can be used instead of R1, however ferrite bead impedance is not well controlled and is generally no greater than 100Ω at 10MHz to 100MHz. This requires a large value capacitor to attenuate the lower frequencies.

Precision instrumentation amplifiers are particularly sensitive to common-mode RFI. Proper filtering is shown in Figure 10.32. Note that there is both common-mode filtering (R1/C1, R2/C2) and differential mode filtering (R1+R2, and C3). If R1/R2 and C1/C2 are not well matched, some of the input common-mode signal at V_{IN} will be converted to a differential one at the in-amp inputs. For this reason, C1 and C2 should be matched to within at least 5% of each other. R1 and R2 should be 1% metal film resistors to insure matching. Capacitor C3 attenuates the differential signal which can result from imperfect matching of the common-mode filters. In this type of filter, C3 should be much larger than C1 or C2 in order to ensure that any differential signal due to mismatching of the common-mode signals is sufficiently attenuated.

The overall filter bandwidth should be chosen to be at least 100 times the input signal bandwidth. The components should be symmetrically mounted on a PC board with a large area ground plane and placed very close to the in-amp input for optimum performance of the filter.

FILTERING AMPLIFIER INPUTS TO PREVENT RFI RECTIFICATION

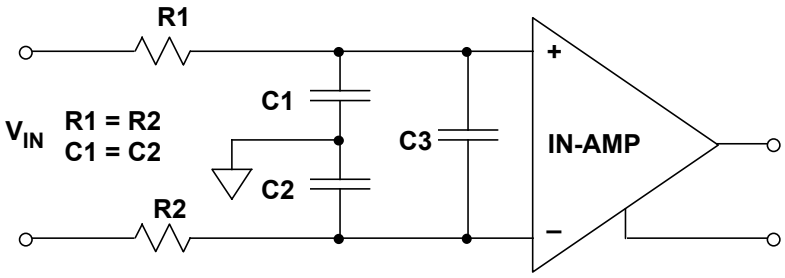


$$\text{FILTER BANDWIDTH} = \frac{1}{2\pi R\, C1}$$

> 100 × SIGNAL BANDWIDTH

Figure 10.31

FILTERING IN-AMP INPUTS



$\tau_{DIFF} = (R1 + R2)\, C3$

$\tau_{CM} = R1 \cdot C1 = R2 \cdot C2$ $\qquad \tau_{DIFF} >> \tau_{CM}$

R1·C1 SHOULD MATCH R2·C2

R1 = R2 SHOULD BE 1% RESISTORS
C1 = C2 SHOULD BE 5% CAPACITORS

$$\text{DIFFERENTIAL FILTER BANDWIDTH} = \frac{1}{2\pi (R1 + R2)\left[\frac{C1 \cdot C2}{C1 + C2} + C3\right]}$$

Figure 10.32

Figure 10.33 shows an actual filter for use with the AD620 in-amp. The common-mode rejection was tested by applying a 1V p-p common-mode signal to the input resistors. The AD620 gain was 1000. The RTI offset voltage of the in-amp was measured as the frequency of the sinewave source was varied from DC to 20MHz. The maximum RTI input offset voltage shift was 1.5µV. The filter bandwidth was approximately 400Hz.

Common-mode chokes offer a simple, one component alternative to RC passive filters. Selecting the proper common-mode choke is critical, however. The choke used in the circuit of Figure 10.34 was a Pulse Engineering B4001 designed for XDSL data receivers (through-hole mount). The B4003 is an equivalent surface mount choke. The maximum RTI offset shift measured from DC to 20MHz was 4.5µV. Unlike the RC filter of Figure 10.32, the choke-based filter offers no differential mode filtration, as shown.

COMMON AND DIFFERENTIAL MODE FILTER WITH AD620

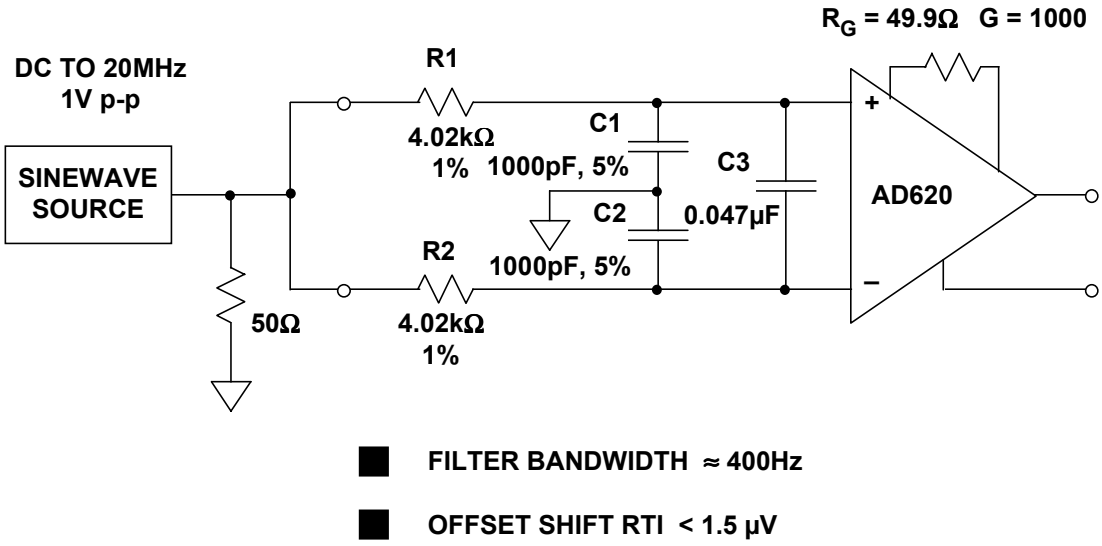
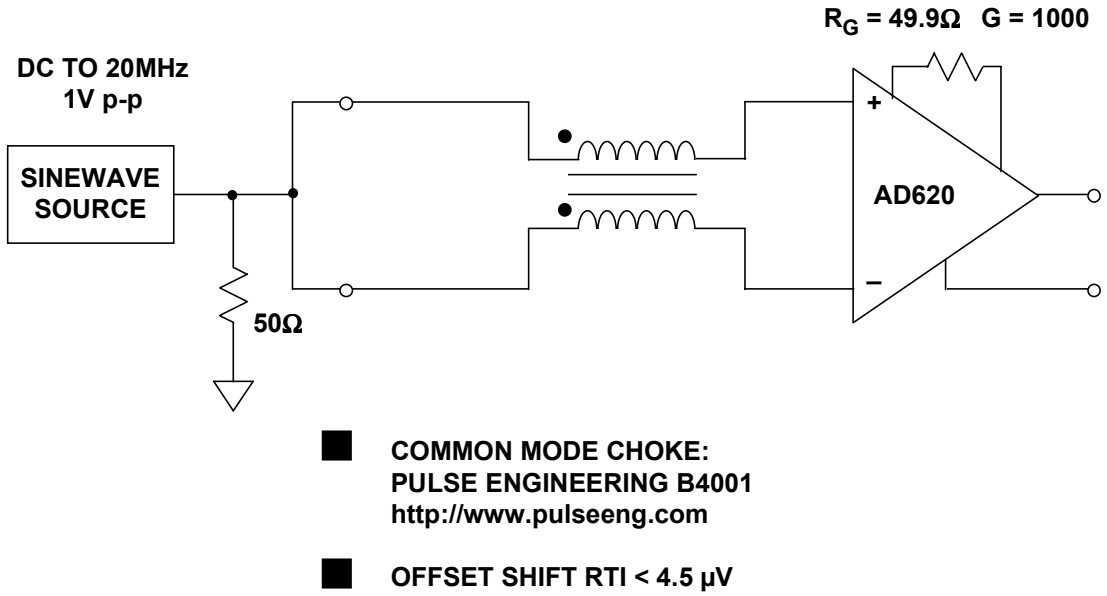


Figure 10.33

In addition to filtering the inputs and the power pins, amplifier outputs need to be protected from RFI, especially if they must drive long lengths of cable. RFI on the output can couple into the amplifier where it is rectified and appears again on the output as a DC offset shift. A resistor or ferrite bead in series with the output is the simplest output filter. Adding a capacitor as shown in Figure 10.35 improves this filter, but the capacitor should not be connected to the op-amp side of the resistor because it may cause the amplifier to become unstable. Many amplifiers are sensitive to direct output capacitive loads, so this condition should be avoided unless the amplifier data sheet clearly specifies that the output is insensitive to capacitive loading.

COMMON MODE CHOKE WITH AD620



- COMMON MODE CHOKE:
  PULSE ENGINEERING B4001
  http://www.pulseeng.com
- OFFSET SHIFT RTI < 4.5 µV

Figure 10.34

FILTERING AMPLIFIER OUTPUTS PROTECTS AGAINST EMI/RFI EMISSION AND SUSCEPTIBILITY

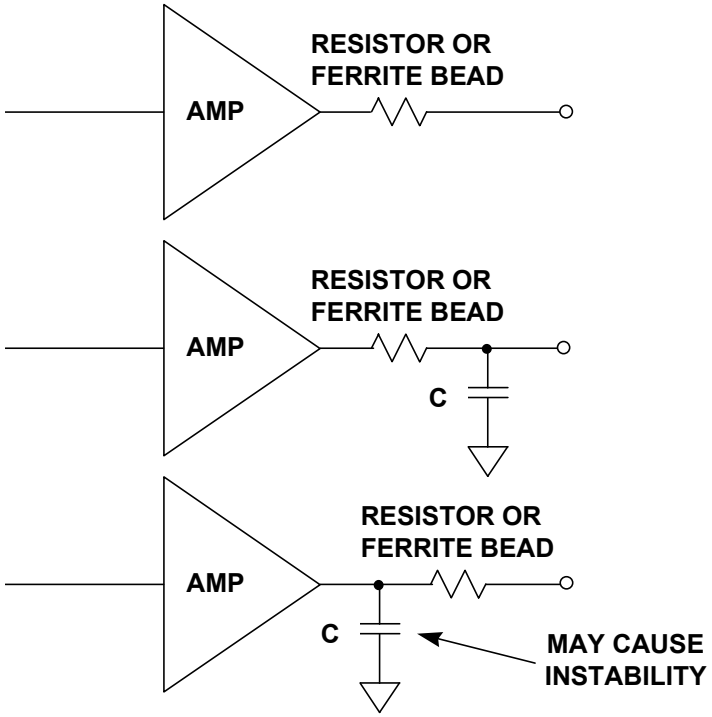


Figure 10.35

REFERENCES ON RFI RECTIFICATION

1. **System Applications Guide**, Analog Devices, Inc., 1993, Section 1, pp. 1.37-1.55.

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DEALING WITH HIGH SPEED LOGIC

Much has been written about terminating printed circuit board traces in their characteristic impedance to avoid reflections. A good rule-of-thumb to determine when this is necessary is as follows: *Terminate the line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster).* A conservative approach is to use a 2 inch (PCB track length)/nanosecond (rise-, fall-time) criterion. For example, PCB tracks for high-speed logic with rise/fall time of 5ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (including any meanders). The 2 inch/nanosecond track length criterion is summarized in Figure 10.36 for a number of logic families.

LINE TERMINATION SHOULD BE USED WHEN LENGTH OF PCB TRACK EXCEEDS 2 inches/ns

DIGITAL IC FAMILY	t_r, t_s (ns)	PCB TRACK LENGTH (inches)	PCB TRACK LENGTH (cm)
GaAs	0.1	0.2	0.5
ECL	0.75	1.5	3.8
Schottky	3	6	15
FAST	3	6	15
AS	3	6	15
AC	4	8	20
ALS	6	12	30
LS	8	16	40
TTL	10	20	50
HC	18	36	90

t_r = rise time of signal in ns
t_f = fall time of signal in ns
For analog signals @ f_{max}, calculate $t_r = t_f = 0.35 / fmax$

Figure 10.36

This same 2 inch/nanosecond rule of thumb should be used with analog circuits in determining the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime, t_r, can be calculated using the equation $t_r = 0.35/f_{max}$.

The maximum PCB track length is then calculated by multiplying the risetime by 2 inch/nanosecond. For example, a maximum output frequency of 100MHz corresponds to a risetime of 3.5ns, and a track carrying this signal greater than 7 inches should be treated as a transmission line.

Equation 10.1 can be used to determine the characteristic impedance of a PCB track separated from a power/ground plane by the board's dielectric (microstrip transmission line):

$$Z_o(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98d}{0.89w + t}\right] \qquad \text{Eq. 10.1}$$

where ε_r = dielectric constant of printed circuit board material;
d = thickness of the board between metal layers, in mils;
w = width of metal trace, in mils; and
t = thickness of metal trace, in mils.

The one-way transit time for a single metal trace over a power/ground plane can be determined from Eq.10.2:

$$t_{pd}(ns/ft) = 1.017\sqrt{0.475\varepsilon_r + 0.67} \qquad \text{Eq. 10.2}$$

For example, a standard 4-layer PCB board might use 8-mil wide, 1 ounce (1.4 mils) copper traces separated by 0.021" FR-4 (ε_r=4.7) dielectric material. The characteristic impedance and one-way transit time of such a signal trace would be 88Ω and 1.7ns/ft (7"/ns), respectively.

The best ways to keep sensitive analog circuits from being affected by fast logic are to physically separate the two and to use no faster logic family than is dictated by system requirements. In some cases, this may require the use of several logic families in a system. An alternative is to use series resistance or ferrite beads to slow down the logic transitions where the speed is not required. Figure 10.37 shows two methods. In the first, the series resistance and the input capacitance of the gate form a lowpass filter. Typical CMOS input capacitance is 10pF. Locate the series resistor close to the driving gate. The resistor minimizes transient currents and may eliminate the necessity of using transmission line techniques. The value of the resistor should be chosen such that the rise and fall times at the receiving gate are fast enough to meet system requirement, but no faster. Also, make sure that the resistor is not so large that the logic levels at the receiver are out of specification because of the source and sink current which must flow through the resistor.

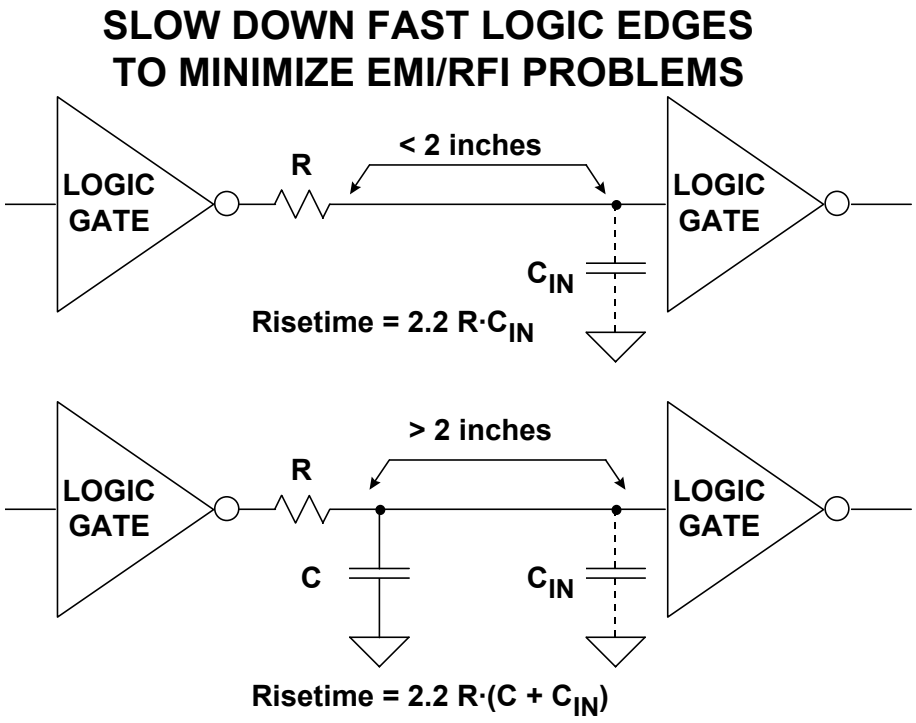
SLOW DOWN FAST LOGIC EDGES
TO MINIMIZE EMI/RFI PROBLEMS
LOGIC GATE
R
< 2 inches
LOGIC GATE
C_{IN}
Risetime = 2.2 R·C_{IN}
LOGIC GATE
R
> 2 inches
LOGIC GATE
C
C_{IN}
Risetime = 2.2 R·(C + C_{IN})

Figure 10.37

A REVIEW OF SHIELDING CONCEPTS

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 1,3, and 4 cited at the end of the section for more detailed information.

Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2π, or $\lambda/2\pi$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1ns pulse edge has an upper bandwidth of approximately 350MHz. The wavelength of a 350MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_0 = 377\Omega$. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377Ω. If the source is low-current and high-voltage (for example, a rod antenna or a high-speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377Ω.

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an impedance mismatch to the incident interference because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. Both concepts are illustrated in Figure 10.38. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

REFLECTION AND ABSORPTION ARE THE TWO PRINCIPAL SHIELDING MECHANISMS

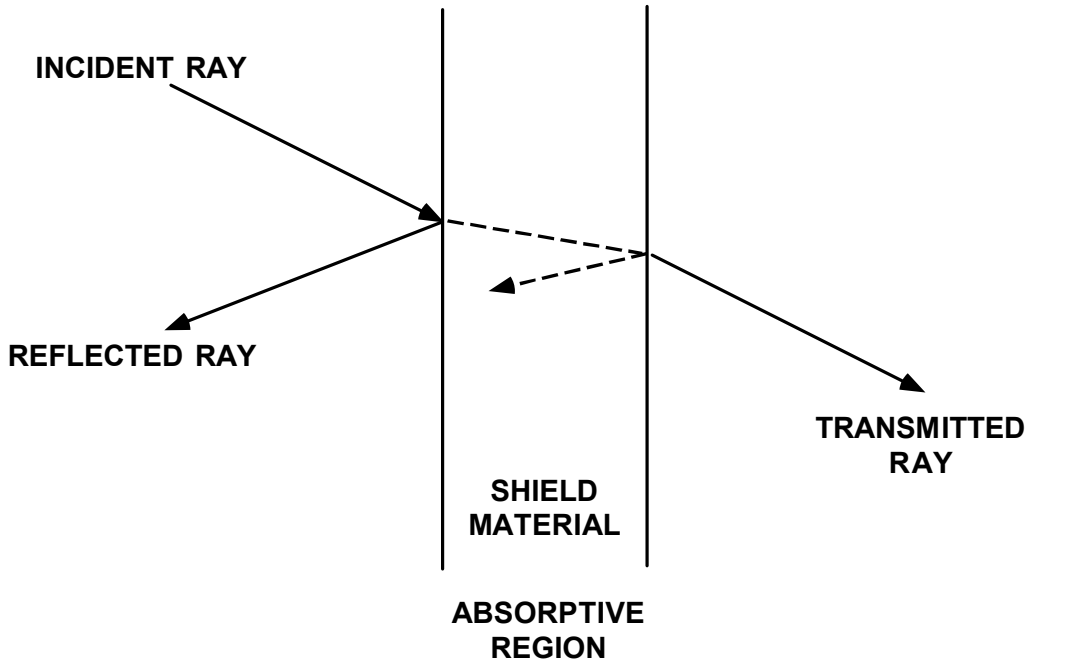

Figure 10.38

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e(\text{dB}) = 322 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f^3 r^2}\right] \qquad \text{Eq. 10.3}$$

where σ_r = relative conductivity of the shielding material, in Siemens per meter;
μ_r = relative permeability of the shielding material, in Henries per meter;
f = frequency of the interference, and
r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m(\text{dB}) = 14.6 + 10\log_{10}\left[\frac{f r^2 \sigma_r}{\mu_r}\right] \qquad \text{Eq. 10.4}$$

and, for plane waves ($r > \lambda/2\pi$), the reflection loss is given by:

$$R_{pw}(dB) = 168 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f}\right] \qquad \text{Eq. 10.5}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A(dB) = 3.34\ t\sqrt{\sigma_r \mu_r f} \qquad \text{Eq. 10.6}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (δ) thick is 9dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_S, increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate shielding. At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low-reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit. Some characteristics of metallic materials commonly used for shielded enclosures are shown in Figure 10.39.

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation. Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

CONDUCTIVITY AND PERMEABILITY FOR VARIOUS SHIELDING MATERIALS

MATERIAL	RELATIVE CONDUCTIVITY	RELATIVE PERMEABILITY
Copper	1	1
Aluminum	1	0.61
Steel	0.1	1,000
Mu-Metal	0.03	20,000

Conductivity: Ability to Conduct Electricity

Permeability: Ability to Absorb Magnetic Energy

Figure 10.39

The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation 10.7 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness } (\text{dB}) = 20 \log_{10}\left(\frac{\lambda}{2 \cdot \text{L}}\right) \qquad \text{Eq. 10.7}$$

where λ = wavelength of the interference and
L = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0dB shielding effectiveness). A rule-of-thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20dB shielding effectiveness. Furthermore, a few small openings on each side of an enclosure is preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the point of shield entry.

General Points on Cables and Shields

Although covered in more detail later, the improper use of cables and their shields is a significant contributor to both radiated and conducted interference. Rather than developing an entire treatise on these issues, the interested reader should consult References 1,2, 4, and 5. As illustrated in Figure 10.40, effective cable and enclosure shielding confines sensitive circuitry and signals within the entire shield without compromising shielding effectiveness. As shown in the diagram, the enclosures and the shield must be grounded properly, otherwise they will act as an antenna and make the radiated and conducted interference problem worse.

"ELECTRICALLY LONG" OR "ELECTRICALLY SHORT" APPLICATION

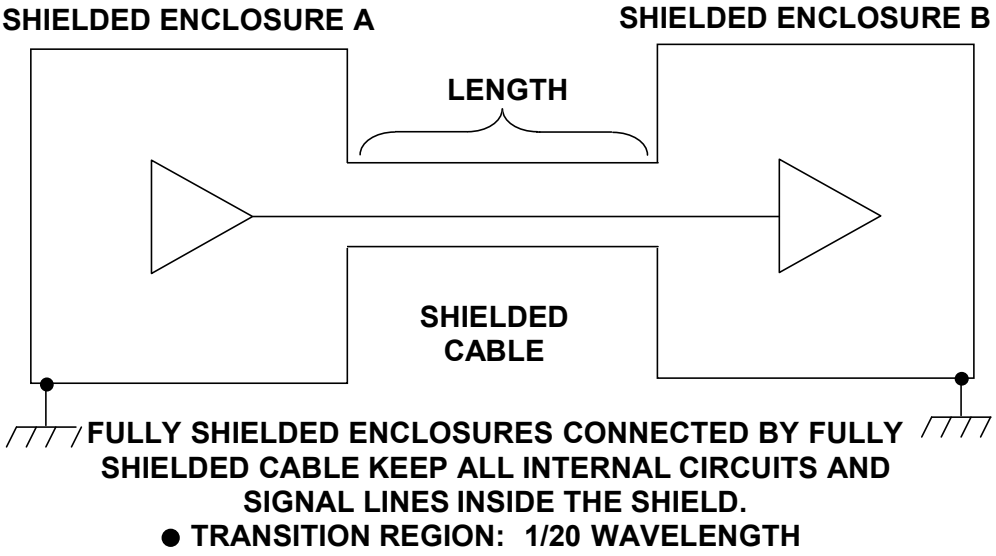

Figure 10.40

Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered *electrically short* if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference, otherwise it is *electrically long*. For example, at 50/60Hz, an *electrically short* cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable.

In those applications where the length of the cable is *electrically long*, or protection against high-frequency interference is required, then the preferred method is to connect the cable shield to low-impedance points at both ends (direct connection at the driving end, and capacitive connection at the receiver). Otherwise, unterminated

transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low-frequency (<1MHz), electric-field interference, grounding the shield at one end is acceptable. For high-frequency interference (>1MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure.

Grounding the shield at both ends, however, can create a low frequency ground loop in a practical situation as shown in Figure 10.41.

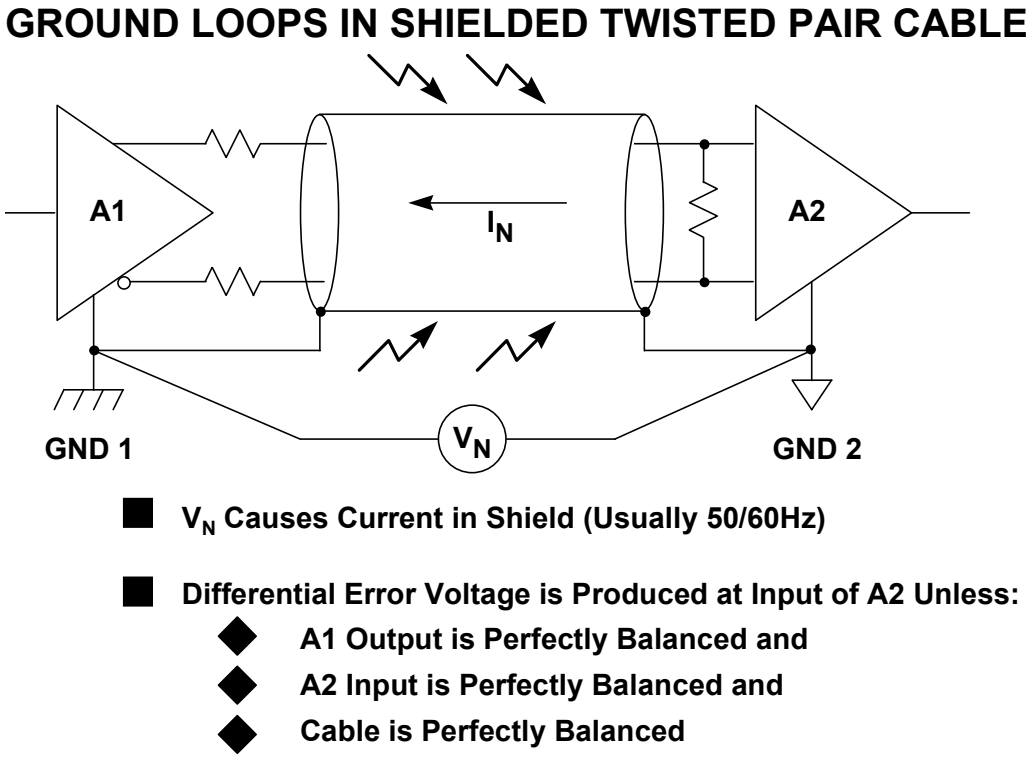

Figure 10.41

As discussed above, cable shields can be subjected to both low and high frequency interference. Good design practice requires that the shield be grounded at both ends if the cable is electrically long to the interference frequency, as is usually the case with RF interference.

When two systems A1 and A2 are remote from each other, however, there is usually a difference in the ground potentials at each system. The frequency of this potential difference is generally the line frequency (50Hz or 60Hz) and multiples thereof. If the shield is grounded at both ends as shown, however, a noise current flows through the shield. In a perfectly balanced system, the common-mode rejection of the system is infinite, and this current produces no differential error at the receiver A2. However, perfect balance is never achieved in the driver, its impedance, the cable, or the receiver, so a certain portion of the shield current will appear as a

differential signal at the input of A2. The following examples illustrate the correct way to ground the shield under various conditions.

Figure 10.42 shows a remote passive RTD sensor connected to a bridge and conditioning circuit by a shielded cable. The proper grounding method is shown in the upper part of the figure, where the shield is grounded at the receiving end. However, safety considerations may require that the remote end of the shield be grounded. If this is the case, the receiving end can be grounded with a low inductance ceramic capacitor (0.01µF to 0.1µF) . The capacitor acts as a ground to RF signals on the shield but blocks line frequency current to flow in the shield. This technique is often referred to as a *hybrid ground*.

In the case of an active remote sensor (Figure 10.43), the hybrid ground is also appropriate, either for a balanced or single-ended driver. The capacitor breaks the DC ground loop in both cases. In both cases, the line is driven from an impedance of R_S, split between legs. In the case of the bottom diagram, the $R_S/2$ resistor in the return leg can only be used for applications with a balanced receiver, as shown.

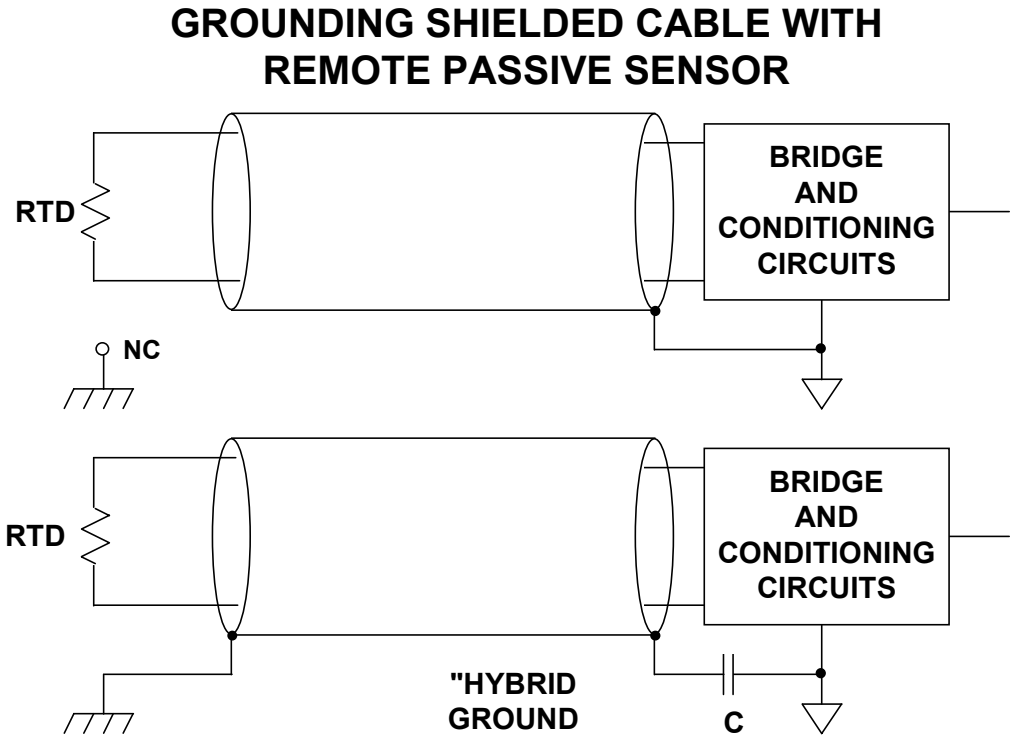

Figure 10.42

Coaxial cables are different from shielded twisted pair cables in that the signal return current path is through the shield. For this reason, the ideal situation is to ground the shield at the driving end and allow the shield to float at the differential receiver (A2) as shown in Figure 10.44. For this technique to work, however, the receiver must be differential and have good high frequency common mode rejection. If the receiver is a single-ended type, there is no choice but to ground the coaxial cable shield at both ends.

GROUNDING SHIELDED CABLE WITH REMOTE ACTIVE SENSOR

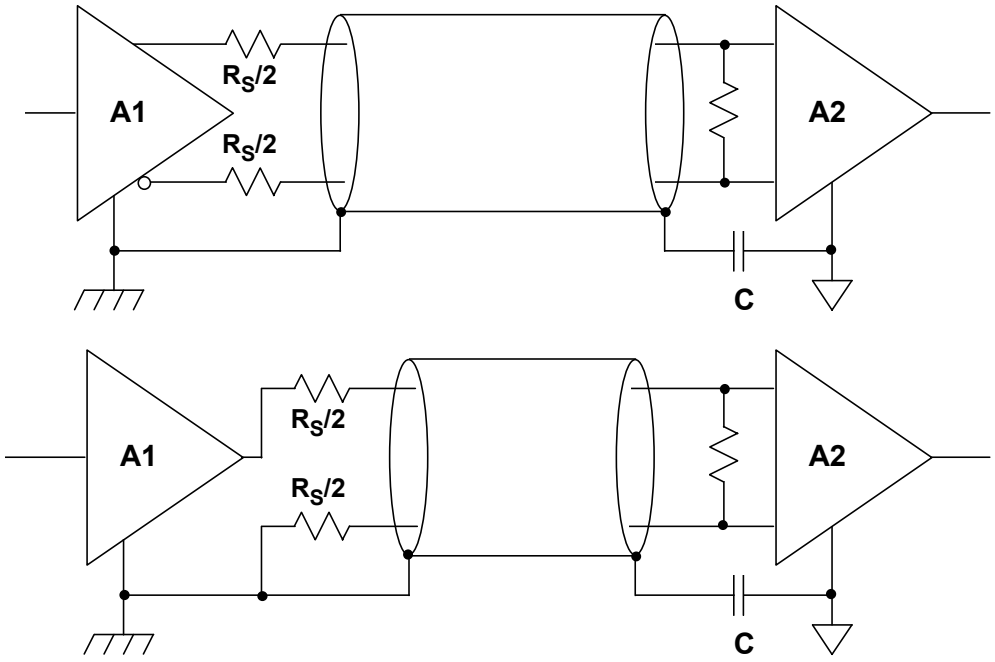

Figure 10.43

COAXIAL CABLE GROUNDING

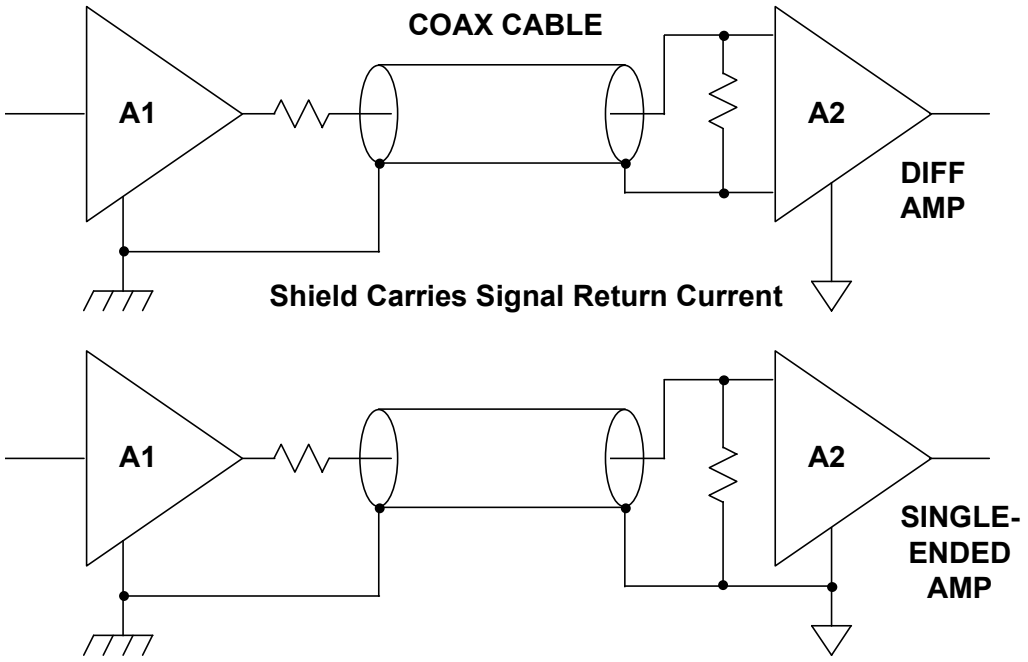

Figure 10.44

Digital Isolation Techniques

Another way to break ground loops is to use isolation techniques. Analog isolation amplifiers find many applications where a high degree of isolation is required, such as in medical instrumentation. Digital isolation techniques offer a reliable method of transmitting digital signals over interfaces without introducing ground noise.

Optoisolators are useful and available in a wide variety of styles and packages. Current is applied to an LED transmitter as shown in Figure 10.45. The light output is received by a phototransistor. Isolation voltages range from 5000V to 7000V. In the circuit, the LED is driven with a current of approximately 10mA. This produces a light output sufficient to saturate the phototransistor. Although excellent for digital signals, optoisolators are too nonlinear for most analog applications. One should realize that since the phototransistor is operated in a saturated mode, rise and fall-times can range from 10µs to 20µs in some slower devices, so the proper optoisolator for the application must be selected.

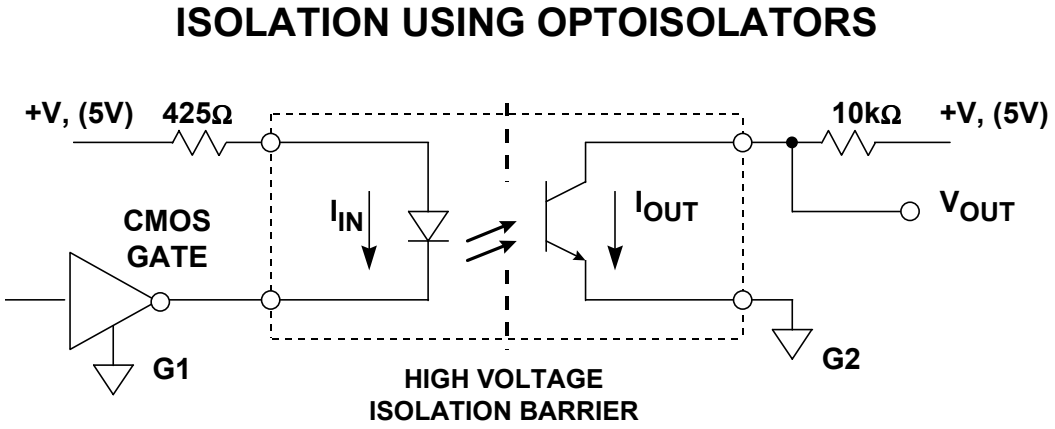

Figure 10.45

The AD260/AD261 family of digital isolators isolates five digital control signals to/from high speed DSPs, microcontrollers, or microprocessors. The AD260 also has a 1.5W transformer for a 3.5kV isolated external DC/DC power supply circuit.

Each line of the AD260 can handle digital signals up to 20MHz with a propagation delay of only 14ns which allows for extremely fast data transmission. Output waveform symmetry is maintained to within ±1ns of the input so the AD260 can be used to accurately isolate time-based pulse width modulator (PWM) signals.

A simplified schematic of one channel of the AD260/AD261 is shown in Figure 10.46. The data input is passed through a schmitt trigger circuit, through a latch, and a special transmitter circuit which differentiates the edges of the digital input signal and drives the primary winding of a proprietary transformer with a "set-high/set-low" signal. The secondary of the isolation transformer drives a receiver with the same "set-hi/set-low" data which regenerates the original logic waveform. An internal circuit operates in the background which interrogates all inputs about every 5µs and in the absence of logic transitions, sends appropriate "set-hi/set-low" data across the interface. Recovery time from a fault condition or at power-up is thus between 5µs and 10µs.

The power transformer (available on the AD260) is designed to operate between 150kHz and 250kHz and will easily deliver more than 1W of isolated power when driven push-pull (5V) on the transmitter side. Different transformer taps, rectifier and regulator schemes will provide combinations of ±5V, 15V, 24V, or even 30V or higher. The output voltage when driven with a low voltage-drop drive will be 37V p-p across the entire secondary with a 5V push-pull drive.

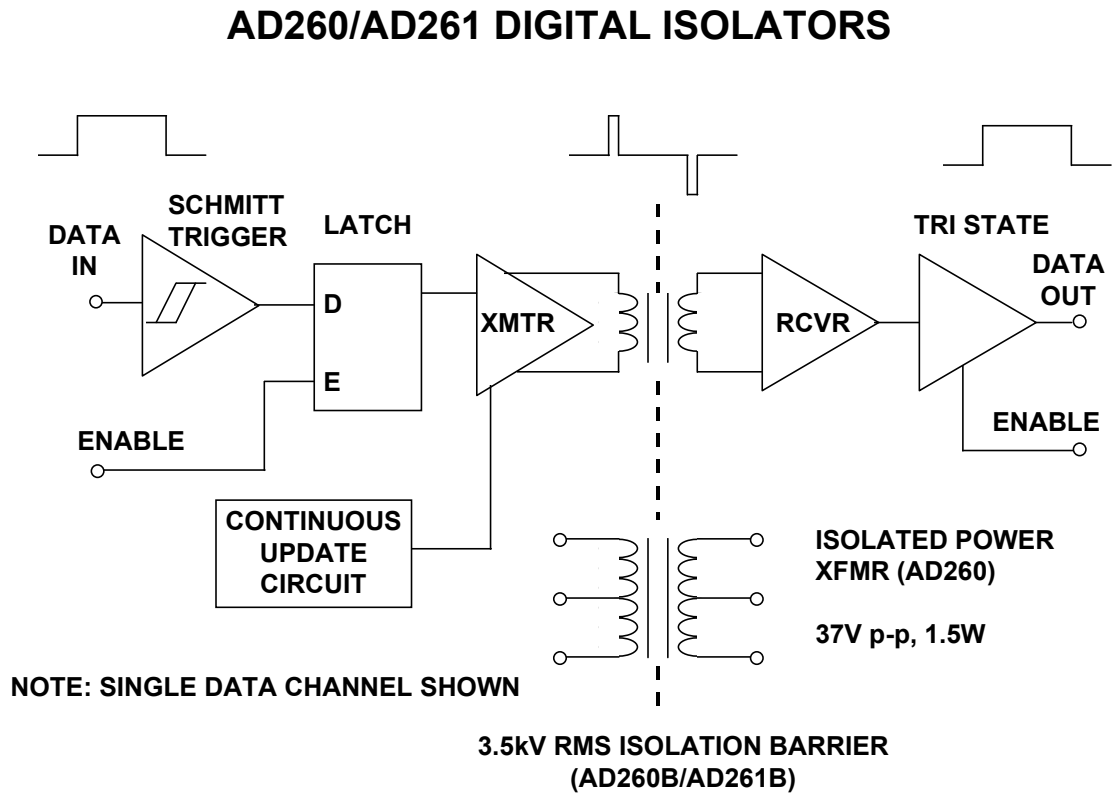

Figure 10.46

AD260/AD261 DIGITAL ISOLATOR KEY SPECIFICATIONS

- **Isolation Test Voltage to 3.5kV RMS (AD260B/AD261B)**
- **Five Isolated Digital Lines Available in 6 Input/Output Configurations**
- **Logic Signal Frequency: 20MHz Max.**
- **Isolated Power Transformer: 37V p-p, 1.5W (AD260)**
- **Waveform Edge Transmission Symmetry: ±1ns**
- **Propagation Delay: 14ns**
- **Rise and Fall-Times < 5ns**

Figure 10.47

REFERENCES ON EMI/RFI AND SHIELDING

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OVERVOLTAGE PROTECTION

Walt Kester, Wes Freeman, Joe Buxton

Op amps and instrumentation amplifiers must often interface to the outside world, which may entail handling voltages that exceed their absolute maximum ratings. Sensors are often placed in an environment where a fault may connect the sensor to high voltages: if the sensor is connected to an amplifier, the amplifier inputs may see voltages exceeding its power supplies. Whenever its input voltage goes outside its supply range, an op amp may be damaged, even when they are turned off. Almost all op amps' input absolute maximum ratings limit the maximum allowable input voltage to the positive and negative supplies or possibly 0.3V outside these supplies. A few exceptions to this rule do exist, which can be identified from individual data sheets, but the vast majority of amplifiers require input protection if over-voltage can possibly occur.

Any op amp input will break down to the positive rail or the negative rail if it encounters sufficient over-voltages. The breakdown voltage is entirely dependent on the structure of the input stage. It may be equivalent to a diode drop of 0.7V or to a process breakdown voltage of 50V or more. The danger of an over-voltage is that when conduction occurs large currents may flow, which can destroy the device. In many cases, over-voltage results in current well in over 100mA, which can destroy a part almost instantly.

To avoid damage, input current should be limited to less than 5mA unless otherwise stated on the relevant data sheet. This value is a conservative rule of thumb based on metal trace widths in a typical op amp input stage. Higher levels of current can cause metal migration, which will eventually lead to an open trace. Migration is a cumulative effect that may not result in a failure for a long period of time. Failure may occur due to multiple over-voltages, which is a difficult failure mode to identify. Thus, even though an amplifier may appear to withstand over-voltage currents well above 5mA for a short period of time, it is important to limit the current to guarantee long term reliability.

Two types of conduction occur in over-voltage conditions, forward biasing of PN junctions inherent in the structure of the input stage or, given enough voltage, reverse junction breakdown. The danger of forward biasing a PN-junction is that excessive current will flow and damage the part. As long as the current is limited no damage should occur. However, when the conduction is due to the reverse breakdown of a PN junction, the problem can be more serious. In the case of a base-emitter junction break down, even small amounts of current can cause degradation in the beta of the transistor. After a breakdown occurs, input parameters such as offset and bias current may be well out of specification. Diode protection is needed to prevent base-emitter junction breakdown. Other junctions, such as base-collector junctions and JFET gate-source junctions do not exhibit the same degradation in performance on break down, and for these the input current should be limited to 5mA, unless the data sheet specifies a larger value.

INPUT OVERVOLTAGE

- **INPUT SHOULD NOT EXCEED ABSOLUTE MAXIMUM RATINGS (Usually Specified With Respect to Supply Voltages)**
- **A Common Specification Requires the Input Signal Remain Within 0.3V of the Supply Rails**
- **Input Stage Conduction Current Should Be Limited (Rule of Thumb: ≤ 5mA Unless Otherwise Specified)**
- **Avoid Reverse Bias Junction Breakdown in Input Stage Junctions**
- **Differential and Common Mode Ratings May Differ**
- **No Two Amplifiers are Exactly the Same**
- **Some ICs Contain Input Protection (Voltage Clamps, Current Limits, or Both), but Absolute Maximum Ratings Must Still Be Observed**

Figure 10.48

A generalized external protection circuit using two Schottky diodes and an external current limiting resistor can be used to ensure input protection as shown in Figure 10.49. If the op amp has internal protection diodes to the supplies, they will conduct at about 0.6V forward drop above or below the supply rails. The external current limit resistor must be chosen so that the maximum amount of input current is limited to 5mA. This can result in large values of R_{LIMIT}, and the resulting increase in noise and offset voltage may not be acceptable. For instance, to protect against a 100V input at V_{IN}, R_{LIMIT} must be greater than 20kΩ (assuming a worst case condition where the supply voltages are at zero volts). The external Schottky protection diodes will begin to conduct at about 0.3V, and overvoltage current is shunted through them to the supply rails rather than through the internal ones. This allows R_{LIMIT} to be set by the maximum allowable diode current, which can be much larger than the internal limit of 5mA. For instance, a 500Ω R_{LIMIT} resistor would limit the diode current to 200mA for a V_{IN} of 100V.
A protection resistor in series with an amplifier input will also produce a voltage drop due to the amplifier bias current flowing through it. This drop appears as an increase in the circuit offset voltage (and, if the bias current changes with temperature, offset drift). In amplifiers where bias currents are approximately equal, a resistor in series with each input will tend to balance the effect and reduce the error.

When using external Schottky clamp diodes to protect operational amplifier inputs, the effects of diode junction capacitance and leakage current should be evaluated in the application. Diode junction capacitance and R_{LIMIT} will add an additional pole in the signal path, and diode leakage currents will double for every 10°C rise in ambient temperature. Therefore, low leakage diodes should be used such that, at the highest ambient temperature for the application, the total diode leakage current is less than one-tenth of the input bias current for the device at that temperature. Another issue with regard to the use of Schottky diodes is the change in their

forward voltage drop as a function of temperature. These diodes do not, in fact, limit the signal to ±0.3V at all ambient temperatures, but if the Schottky diodes are at the same temperature as the op amp, they will limit the voltage to a safe level, even if they do not limit it at all times to within the data sheet rating. This is true if over-voltage is only possible at turn-on, when the diodes and the op amp will always be at the same temperature. If the op amp is warm when it is repowered, however, steps must be taken to ensure that diodes and op amp are at the same temperature.

GENERALIZED EXTERNAL OVERVOLTAGE PROTECTION CIRCUIT FOR OP AMPS

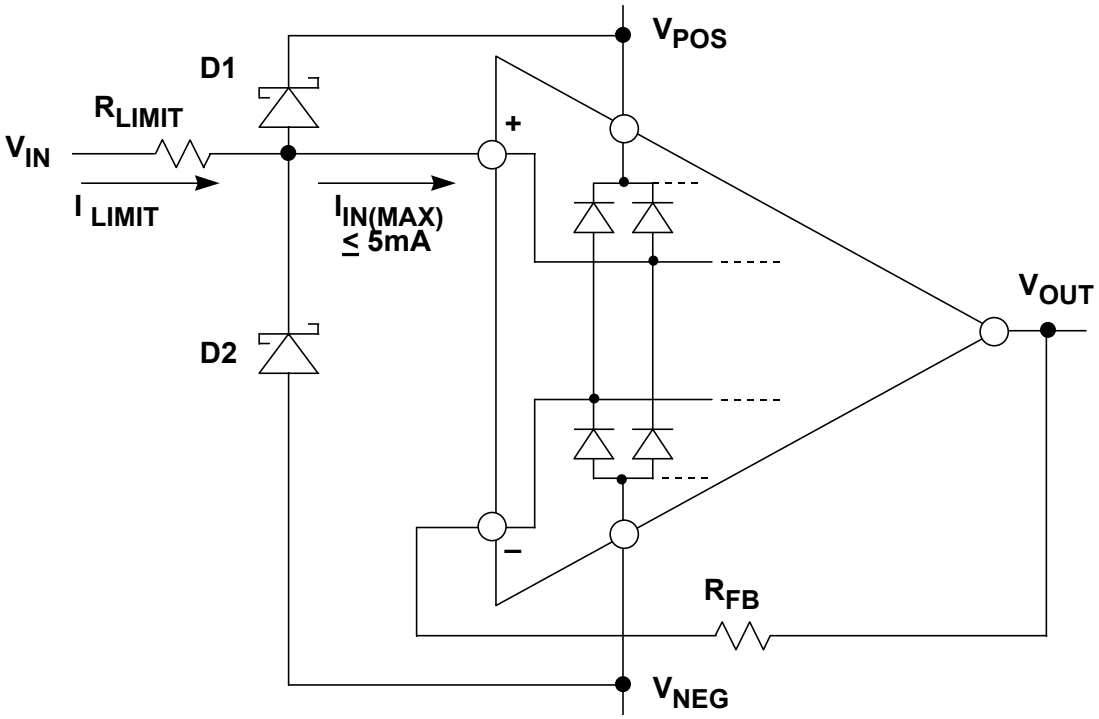


Figure 10.49

A simplified schematic of the AD620 instrumentation amplifier is shown in Figure 10.50. The 400Ω input resistors are thin-film, and therefore do not behave as junctions, as would be the case with diffused resistors. The input transistors Q1 and Q2 have diodes D1 and D2 across their base-emitter junctions to prevent reverse breakdown. Figure 10.51 shows an equivalent input circuit for an overvoltage condition. The common-mode voltage at $+V_{IN}$ or $-V_{IN}$ should be limited to 0.3V above V_{POS} and 0.3V below V_{NEG}. In addition, the differential input voltage should be limited to a value which limits the input current to 10mA maximum. The equivalent circuit shows that the input current flows through the two external R_{LIMIT} resistors, the two internal R_S resistors, the gain-setting resistor R_G, and two diode drops (Q2 and D1). For a given differential input voltage, the input current is a function of R_G and hence the gain. For a gain of 1000, R_G = 49.9Ω, and therefore has more of an impact on the input current than for a gain of 10, where R_G = 5.49kΩ.

AD620 SIMPLIFIED SCHEMATIC

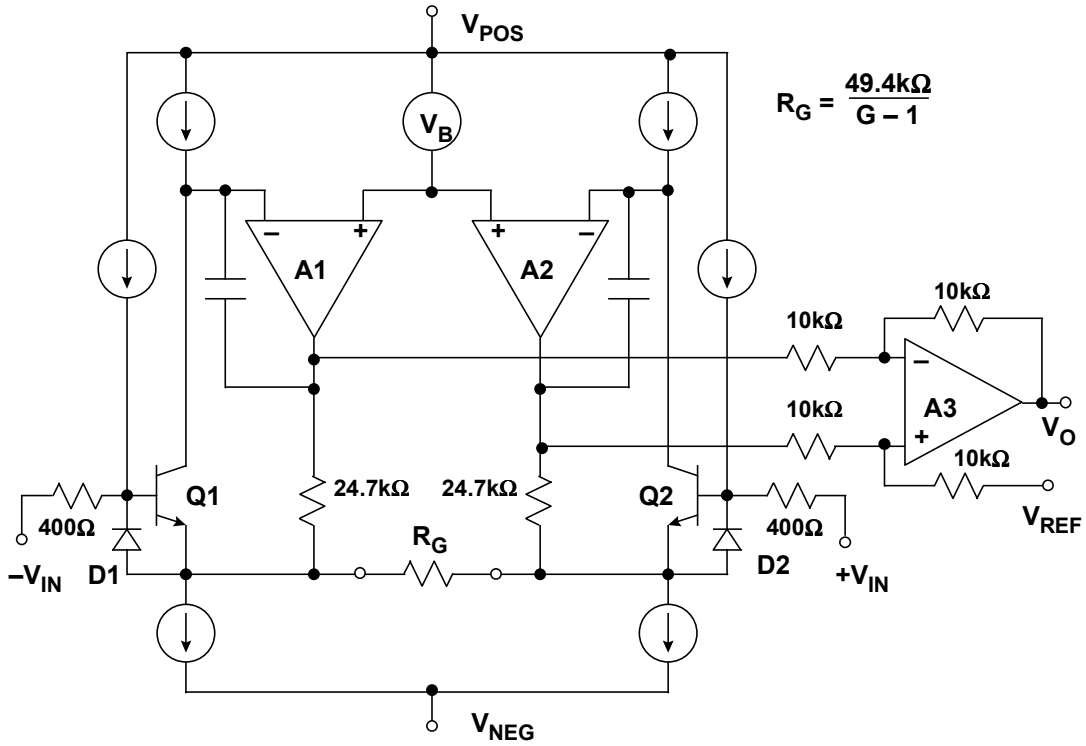
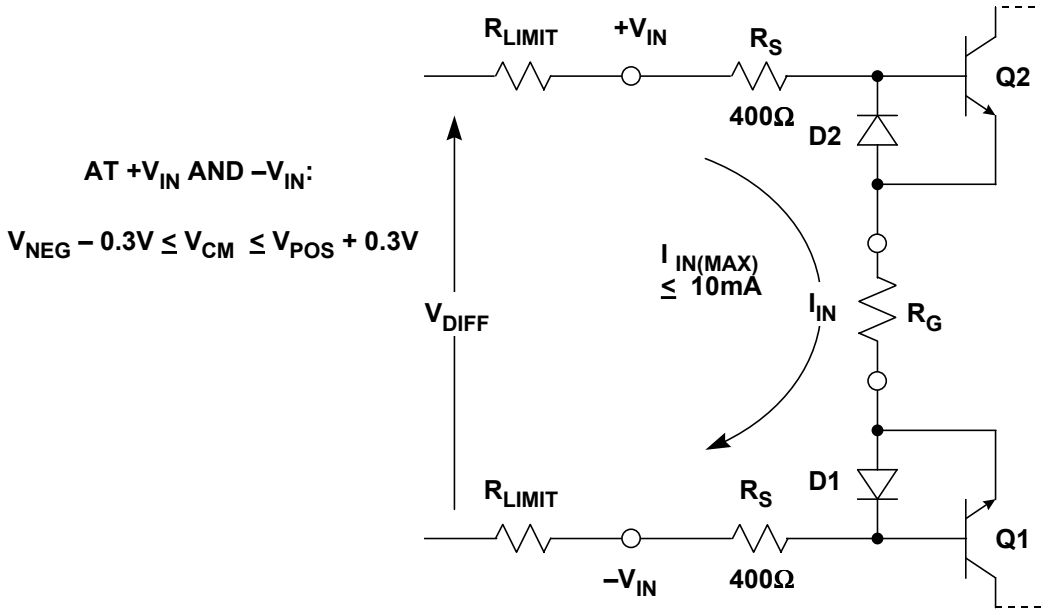


Figure 10.50

AD620 EQUIVALENT INPUT CIRCUIT WITH OVERVOLTAGE



$V_{DIFF} = I_{IN}(2R_S + 2R_{LIMIT} + R_G) + 1.2V$

$V_{DIFF(MAX)} \le I_{IN(MAX)}(2R_S + 2R_{LIMIT} + R_G) + 1.2V$

Figure 10.51

A generalized external voltage protection circuit for an in-amp is shown in Figure 10.52. The R_{LIMIT} resistors are chosen to limit the maximum current through the diodes connected to V_{POS} and V_{NEG}. The Zener diodes or Transient Voltage Suppressers (TVSs, or TransZorbs™) are selected to limit the maximum differential input voltage to less than $|V_{POS} - V_{NEG}|$ if required.

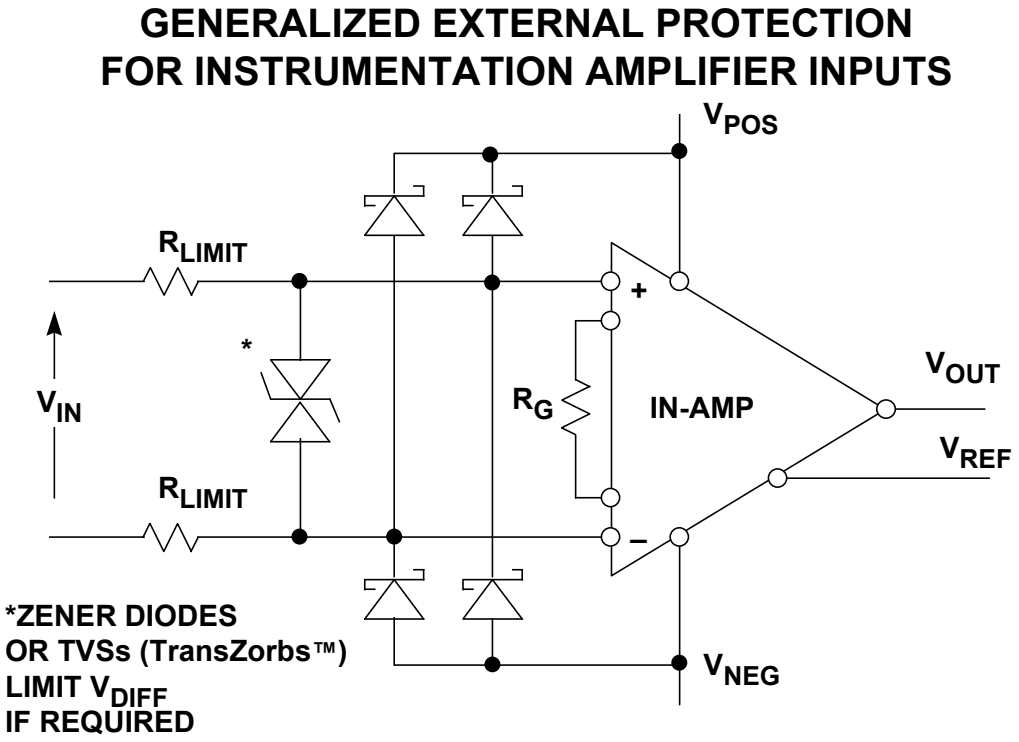


Figure 10.52

The two op amp instrumentation (see Figure 10.53) can generally be protected with external Schottky diodes to the supplies and current limit resistors. The input current is not a function of the gain-setting resistor as in the case of the three op amp in-amp configuration.

ADCs whose input range falls between the supply rails can generally be protected with external Schottky diodes and a current limit resistor as shown in Figure 10.54. Even if internal ESD protection diodes are provided, the use of the external ones allows smaller values of R_{LIMIT} and lower noise and offset errors. ADCs with thin-film input attenuators, such as the AD7890-10 (see Figure 10.55), can be protected with Zener diodes on TVSs with an R_{LIMIT} resistor to limit the current through them.

INPUT PROTECTION FOR TWO OP AMP IN-AMP (AD627)

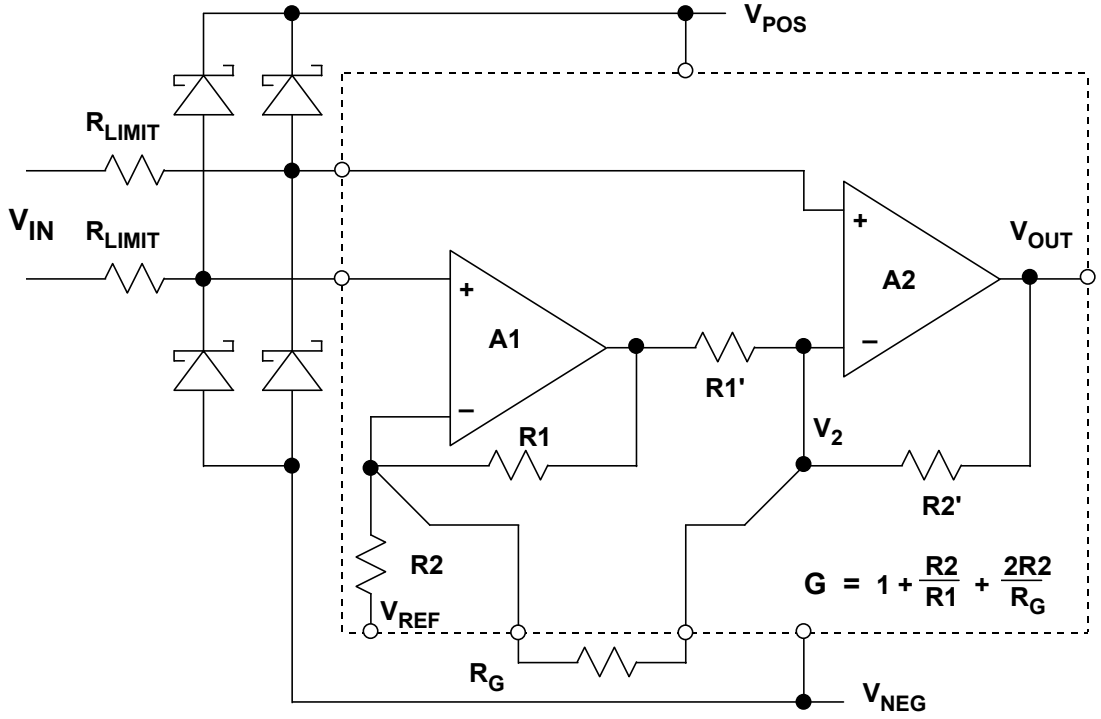
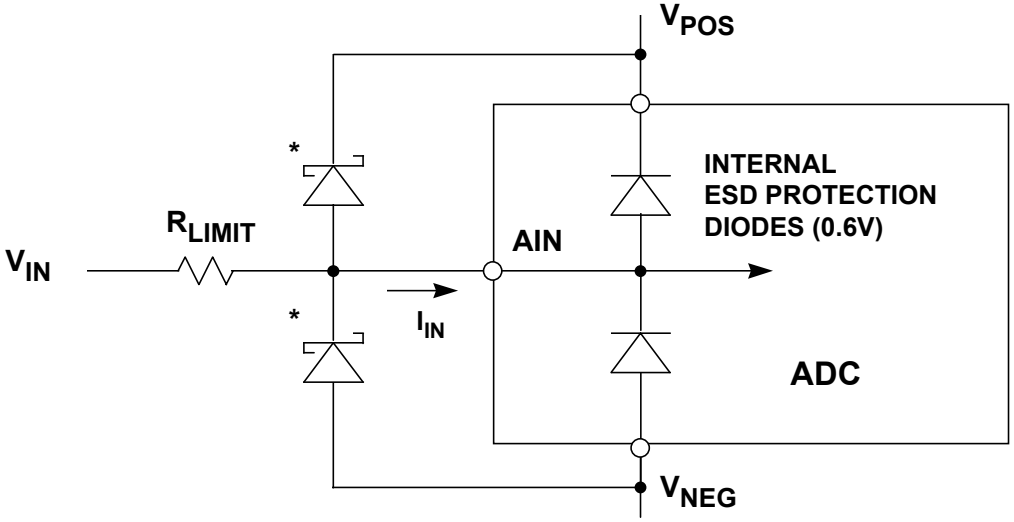


Figure 10.53

INPUT PROTECTION FOR ADCs WITH INPUT RANGES WITHIN SUPPLY VOLTAGES



- Choose R_{LIMIT} to Limit I_{IN} Current to 5mA
- *Additional External Schottky Diodes Allow Lower Values of R_{LIMIT}

Figure 10.54

INPUT PROTECTION FOR SINGLE-SUPPLY ADCs WITH THIN FILM RESISTOR INPUT ATTENUATORS

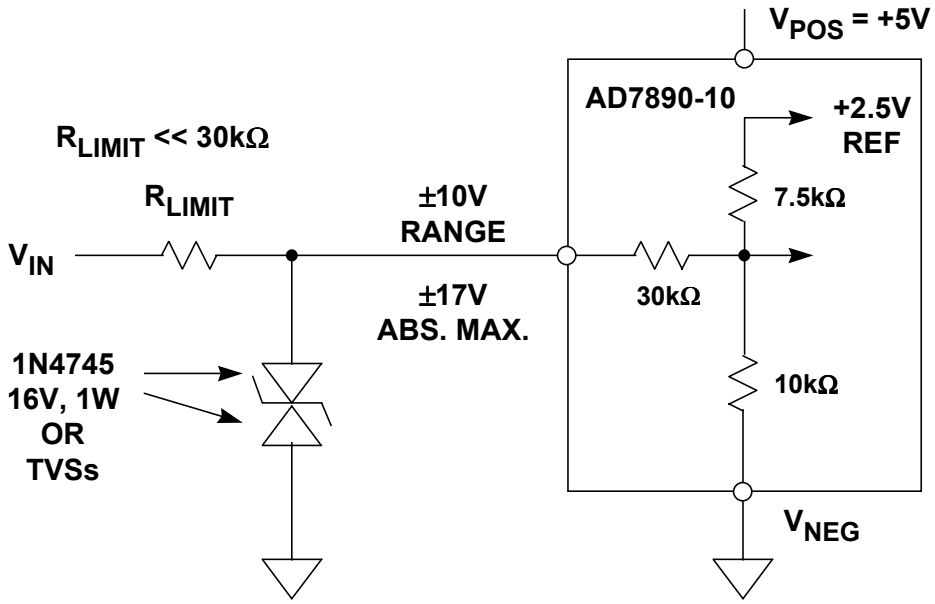


Figure 10.55

Overvoltage Protection Using CMOS Channel Protectors

The ADG465/ADG466/ADG467 are CMOS channel protectors which are placed in series with the signal path. The channel protector will protect sensitive components from voltage transients whether the power supplies are present or not. Because the channel protection works whether the supplies are present or not, the channel protectors are ideal for use in applications where correct power sequencing cannot always be guaranteed (e.g., hot-insertion rack systems) to protect analog inputs.

Each channel protector (see Figure 10.56) has an independent operation and consists of four MOS transistors - two NMOS and two PMOS. One of the PMOS devices does not lie directly in the signal path but is used to connect the source of the second PMOS device to its backgate. This has the effect of lowering the threshold voltage and so increasing the input signal range of the channel for normal operation. The source and backgate of the NMOS devices are connected for the same reason.

The channel protector behaves just like a series resistor (60Ω to 80Ω) during normal operation, i.e., $(V_{SS} + 2V) < V_D < (V_{DD} – 1.5V)$. When a channel's analog input voltage exceeds this range, one of the MOSFETs will switch off, clamping the output at either V_{SS} + 2V or V_{DD} – 1.5V. Circuitry and signal source protection is provided in the event of an overvoltage or power loss. The channel protectors can withstand overvoltage inputs from V_{SS} – 20V to V_{DD} + 20V with power on (V_{DD} – V_{SS} = 44V maximum). With power off ($V_{DD} = V_{SS} = 0V$), maximum input voltage is ±35V. The channel protectors are very low power devices, and even under fault conditions, the supply current is limited to sub microampere levels. All transistors

are dielectrically isolated from each other using a trench isolation method thereby ensuring that the channel protectors cannot latch up.

Figure 10.58 shows a typical application that requires overvoltage and power supply sequencing protection. The application shows a hot-insertion rack system. This involves plugging a circuit board or module into a live rack via an edge connector. In this type of application it is not possible to guarantee correct power supply sequencing. Correct power supply sequencing means that the power supplies should be connected before any external signals. Incorrect power sequencing can cause a CMOS device to latch up. This is true of most CMOS devices regardless of the functionality. RC networks are used on the supplies of the channel protector to ensure that the rest of the circuit is powered up before the channel protectors. In this way, the outputs of the channel protectors are clamped well below V_{DD} and V_{SS} until the capacitors are charged. The diodes ensure that the supplies on the channel protector never exceed the supply rails when it is being disconnected. Again this ensures that signals on the inputs of the CMOS devices never exceed the supplies.

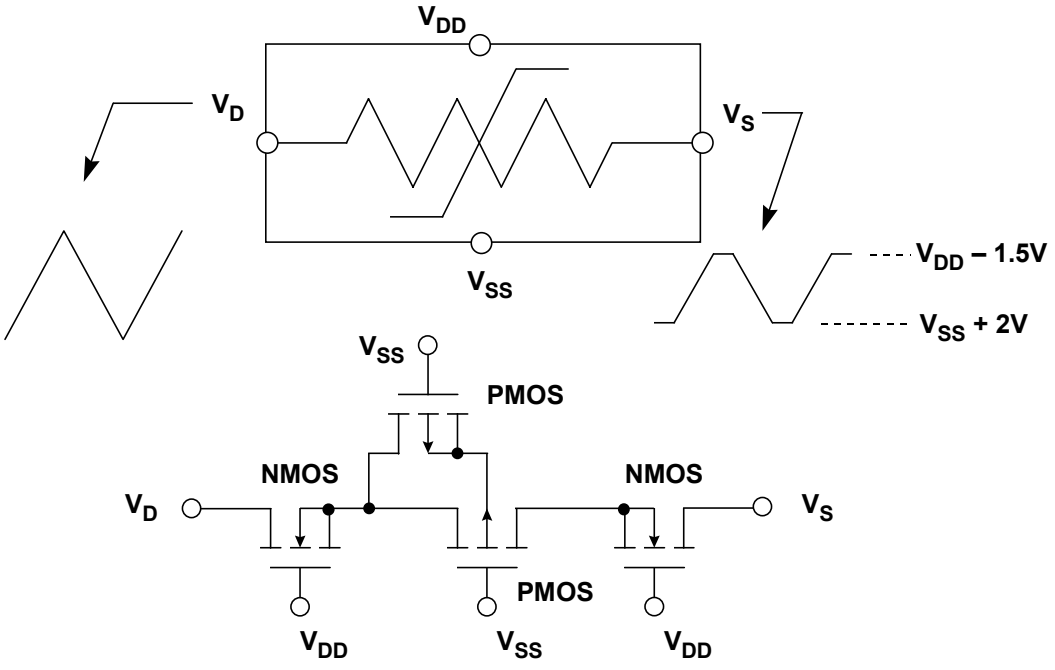


Figure 10.56

ADG465, ADG466, and ADG467 CHANNEL PROTECTORS KEY SPECIFICATIONS

- Low On-Resistance (50Ω for ADG465, 80Ω for ADG466/467)
- On-Resistance Match: 3%
- 44V Maximum Supply Voltage, $V_{DD} - V_{SS}$
- Fault and Overvoltage Protection up to ±40V
- Positive Overvoltages Clamped at $V_{DD} - 1.5V$
- Negative Overvoltages Clamped at $V_{SS} + 2V$
- Signal Paths Open-Circuit with Power Off
- Latch-Up Proof Construction

Figure 10.57

OVERVOLTAGE AND POWER SUPPLY SEQUENCING PROTECTION USING THE ADG466

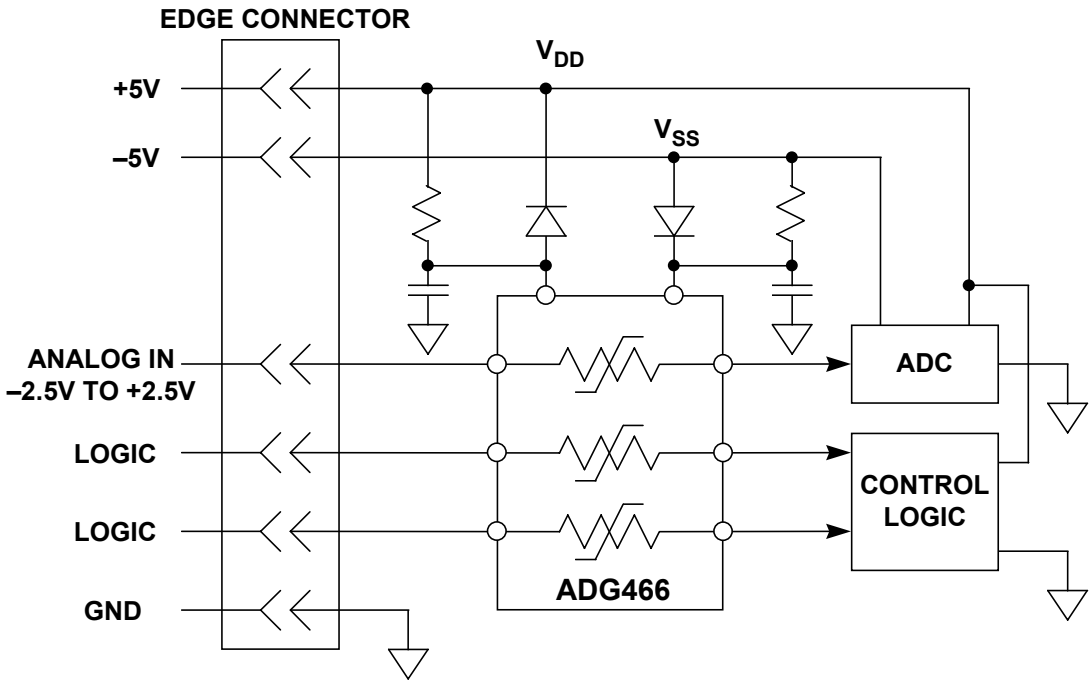


Figure 10.58

ELECTROSTATIC DISCHARGE
Walt Kester, Wes Freeman, James Bryant

Electrostatic discharge is a single, fast, high current transfer of electrostatic charge that results from:

(1) Direct contact transfer between two objects at different potentials (sometimes called contact discharge), or
(2) A high electrostatic field between two objects when they are in close proximity (sometimes called air discharge)

The prime sources of static electricity are mostly insulators and are typically synthetic materials, e.g., vinyl or plastic work surfaces, insulated shoes, finished wood chairs, Scotch tape, bubble pack, soldering irons with ungrounded tips, etc. Voltage levels generated by these sources can be extremely high since their charge is not readily distributed over their surfaces or conducted to other objects.

The generation of static electricity caused by rubbing two substances together is called the *triboelectric* effect. Examples are shown in Figure 10.59.

EXAMPLES OF ELECTROSTATIC CHARGE GENERATION

- **Walking Across a Carpet**
  - **1000V - 1500V Generated**
- **Walking Across a Vinyl Floor**
  - **150V - 250V Generated**
- **Handling Material Protected by Clear Plastic Covers**
  - **400V - 600V Generated**
- **Handling Polyethylene Bags**
  - **1000V - 2000V Generated**
- **Pouring Polyurethane Foam Into a Box**
  - **1200V - 1500V Generated**

- **Note: Assume 60% RH. For Low RH (30%), Generated Voltages Can Be >10 Times Those Listed Above**

Figure 10.59

Integrated circuits can be damaged by the high voltages and high peak currents that can be generated by electrostatic discharge. Precision analog circuits, which often feature very low bias currents, are more susceptible to damage than common digital circuits, because the traditional input-protection structures which protect against ESD damage also increase input leakage.

For the design engineer or technician, the most common manifestation of ESD damage is a catastrophic failure of the IC. However, exposure to ESD can also cause increased leakage or degrade other parameters. If a device appears to not meet a data sheet specification during evaluation, the possibility of ESD damage should be considered.

UNDERSTANDING ESD DAMAGE

- **ESD Failure Mechanisms:**
  - **Dielectric or junction damage**
  - **Surface charge accumulation**
  - **Conductor fusing**
- **ESD Damage Can Cause:**
  - **Increased leakage**
  - **Degradation in performance**
  - **Functional failures of ICs.**
- **ESD Damage is often Cumulative:**
  - **For example, each ESD "zap" may increase junction damage until, finally, the device fails.**

Figure 10.60

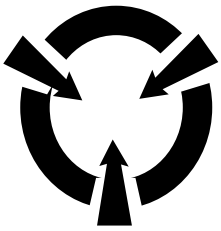
All ESD sensitive devices are shipped in protective packaging. ICs are usually contained in either conductive foam or antistatic tubes. Either way, the container is then sealed in a static-dissipative plastic bag. The sealed bag is marked with a distinctive sticker, such as that shown in Figure 10.61, which outlines the appropriate handling procedures. In addition, the data sheets for ESD sensitive ICs generally have a statement to that effect (see Figure 10.62).

Once ESD-sensitive devices are identified, protection is relatively easy. Obviously, keeping ICs in their original protective packaging as long as possible is the first step. The second step is to discharge potential ESD sources before damage to the IC can occur. Discharging a potentially dangerous voltage can be done quickly and safely through a high impedance.

The key component required for safe ESD handling is a workbench with a static-dissipative surface, as shown in Figure 10.63. This surface is connected to ground through a 1MΩ resistor, which dissipates static charge while protecting the user from electrical shock hazards caused by ground faults. If existing bench tops are nonconductive, a static-dissipative mat should be added, along with a discharge resistor.

RECOGNIZING ESD SENSITIVE DEVICES

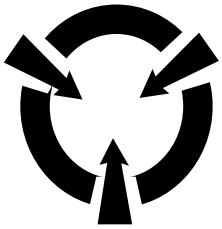
All static sensitive devices are sealed in protective packaging and marked with special handling instructions



CAUTION

SENSITIVE ELECTRONIC DEVICES

DO NOT SHIP OR STORE NEAR STRONG ELECTROSTATIC, ELECTROMAGNETIC, MAGNETIC, OR RADIOACTIVE FIELDS



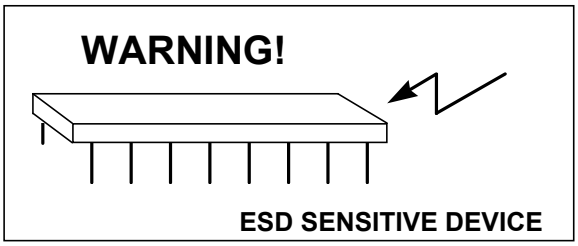
CAUTION

SENSITIVE ELECTRONIC DEVICES

DO NOT OPEN EXCEPT AT APPROVED FIELD FORCE PROTECTIVE WORK STATION

Figure 10.61

ESD STATEMENT ON DATA SHEETS OF MOST LINEAR AND MIXED-SIGNAL ICs



CAUTION

ESD (Electrostatic Discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADXXX features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Figure 10.62

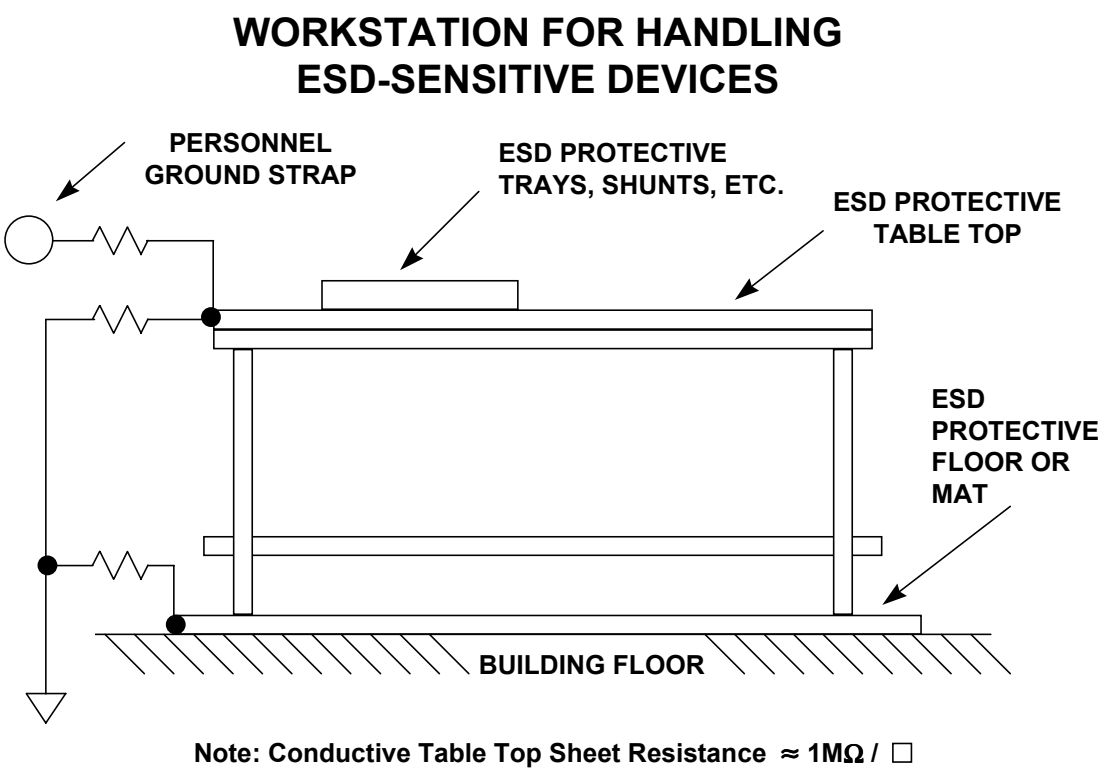


Figure 10.63

Notice that the surface of the workbench has a moderately high sheet resistance. It is neither necessary nor desirable to use a low-resistance surface (such as a sheet of copper-clad PC board) for the work surface. Remember, a high peak current may flow if a charged IC is discharged through a low impedance. This is precisely what happens when a charged IC contacts a grounded copper clad board. When the same charged IC is placed on the surface shown in Figure 10.63, however, the peak current is not high enough to damage the device.

A conductive wrist strap is also recommended while handling ESD-sensitive devices. The wrist strap ensures that normal tasks, such as peeling tape off of packages, will not cause damage to ICs. Again, a 1MΩ resistor, from the wrist strap to ground, is required for safety.

When building prototype breadboards or assembling PC boards which contain ESD-sensitive devices, all passive components should be inserted and soldered before the ICs. This procedure minimizes the ESD exposure of the sensitive devices. The soldering iron must, of course, have a grounded tip.

Protecting ICs from ESD requires the participation of both the IC manufacturer and the customer. IC manufacturers have a vested interest in providing the highest possible level of ESD protection for their products. IC circuit designers, process engineers, packaging specialists and others are constantly looking for new and improved circuit designs, processes, and packaging methods to withstand or shunt ESD energy.

A complete ESD protection plan, however, requires more than building-ESD protection into ICs. Users of ICs must also provide their employees with the necessary knowledge of and training in ESD handling procedures (Figure 10.64).

ESD PROTECTION REQUIRES A PARTNERSHIP BETWEEN THE IC SUPPLIER AND THE CUSTOMER

ANALOG DEVICES:

- **Circuit Design and Fabrication -**
  - **Design and manufacture products with the highest level of ESD protection consistent with required analog and digital performance.**
- **Pack and Ship -**
  - **Pack in static dissipative material. Mark packages with ESD warning.**

CUSTOMERS:

- **Incoming Inspection -**
  - **Inspect at grounded workstation. Minimize handling.**
- **Inventory Control -**
  - **Store in original ESD-safe packaging. Minimize handling.**
- **Manufacturing -**
  - **Deliver to work area in original ESD-safe packaging. Open packages only at grounded workstation. Package subassemblies in static dissipative packaging.**
- **Pack and Ship -**

  Pack in static dissipative material if required. Replacement or optional boards may require special attention.

Figure 10.64

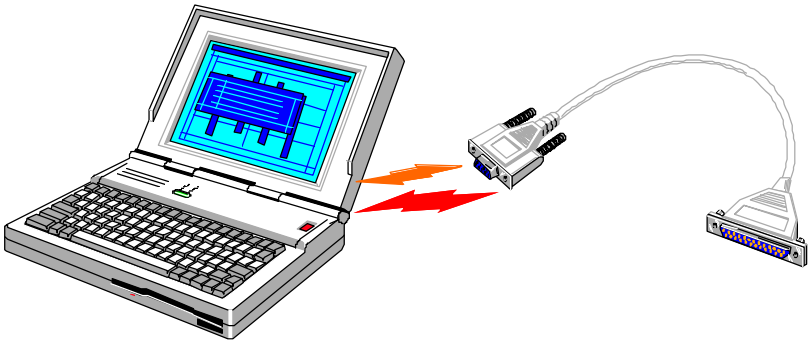
Special care should be taken when breadboarding and evaluating ICs. The effects of ESD damage can be cumulative, so repeated mishandling of a device can eventually cause a failure. Inserting and removing ICs from a test socket, storing devices during evaluation, and adding or removing external components on the breadboard should all be done while observing proper ESD precautions. Again, if a device fails during a prototype system development, repeated ESD stress may be the cause.

The key word to remember with respect to ESD is *prevention*. There is no way to undo ESD damage, or to compensate for its effects.

ESD Models and Testing

Some applications have higher ESD sensitivity than others. ICs which are located on a PC board surrounded by other circuits are generally much less susceptible to ESD damage than circuits which must interface with other PC boards or the outside world. These ICs are generally not specified or guaranteed to meet any particular ESD specification (with the exception of MIL-STD-883 Method 3015 classified devices). A good example of an ESD-sensitive interface is the RS-232 port on a computer (see Figure 10.65). The RS-232 driver and receiver ICs are directly in the firing line for voltage transients as well as ESD. In order to guarantee ESD performance for such devices, the test methods and limits must be specified.

RS-232 PORT IS VERY SUSCEPTIBLE TO ESD



- **I-O Transceiver Is Directly in the Firing Line for Transients - RS-232 Port Is Particularly Vulnerable**
- **I-O Port Is an Open Gateway in the Enclosure**
- **Harmonised Standards Are Now Mandatory Requirements in European Community**

Figure 10.65

A host of test waveforms and specifications have been developed to evaluate the susceptibility of devices to ESD. The three most prominent of these waveforms currently in use for semiconductor or discrete devices are: The Human Body Model (HBM), the Machine Model (MM), and the Charged Device Model (CDM). Each of these models represents a fundamentally different ESD event, consequently, correlation between the test results for these models is minimal.

Since 1996, all electronic equipment sold to or within the European Community must meet Electromechanical Compatibility (EMC) levels as defined in specification IEC1000-4-x. This does not apply to individual ICs, but to the end equipment. These standards are defined along with test methods in the various IEC1000 specifications shown in Figure 10.66.

IEC1000-4-2 specifies compliance testing using two coupling methods, *contact discharge* and *air-gap discharge*. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage, but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, hence the term air discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method, while less realistic, is more repeatable and is gaining acceptance in preference to the air-gap method.

IEC 1000-4-x BASIC IMMUNITY STANDARDS FOR ELECTRONIC EQUIPMENT (NOT ICs!)

- **IEC1000-4 Electromagnetic Compatibility EMC**
- **IEC1000-4-1 Overview of Immunity Tests**
- **IEC1000-4-2 Electrostatic Discharge Immunity (ESD)**
- **IEC1000-4-3 Radiated Radio-Frequency Electromagnetic Field Immunity**
- **IEC1000-4-4 Electrical Fast Transients (EFT)**
- **IEC1000-4-5 Lightening Surges**
- **IEC1000-4-6 Conducted Radio Frequency Disturbances above 9kHz**
- **Compliance Marking:** CE

Figure 10.66

Although very little energy is contained within an ESD pulse, the extremely fast risetime coupled with high voltages can cause failures in unprotected ICs. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation, which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

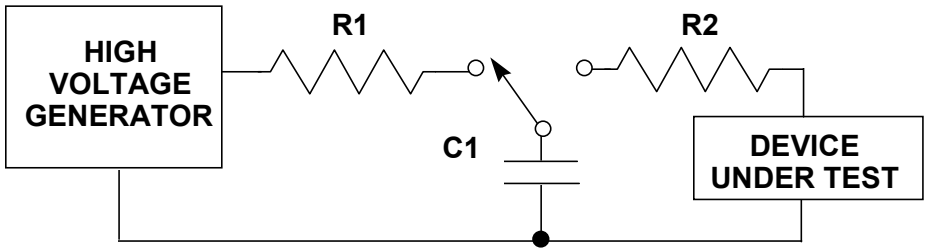
I-O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I-O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I-O port (such as RS-232 line drivers and receivers). Traditional ESD test methods such as MIL-STD-883B Method 3015.7 do not fully test a product's susceptibility to this type of discharge. This test was intended to test a product's susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the MIL-STD-883B Method 3015.7 test and the IEC test:

(1) The IEC test is much more stringent in terms of discharge energy. The peak current injected is over four times greater.
(2) The current risetime is significantly faster in the IEC test.
(3) The IEC test is carried out while power is applied to the device.

It is possible that ESD discharge could induce latch-up in the device under test. This test is therefore more representative of a real-world I-O discharge where the equipment is operating normally with power applied. For maximum confidence, however, both tests should be performed on interface devices, thus ensuring maximum protection both during handling, and later, during field service.

A comparison of the test circuit values for the IEC1000-4-2 model versus the MIL-STD-883B Method 3015.7 Human Body Model is shown in Figure 10.67, and the ESD waveforms are compared in Figure 10.68.

MIL STD 883B METHOD 3015.7 HUMAN BODY MODEL VERSUS IEC 1000-4-2 ESD TESTING



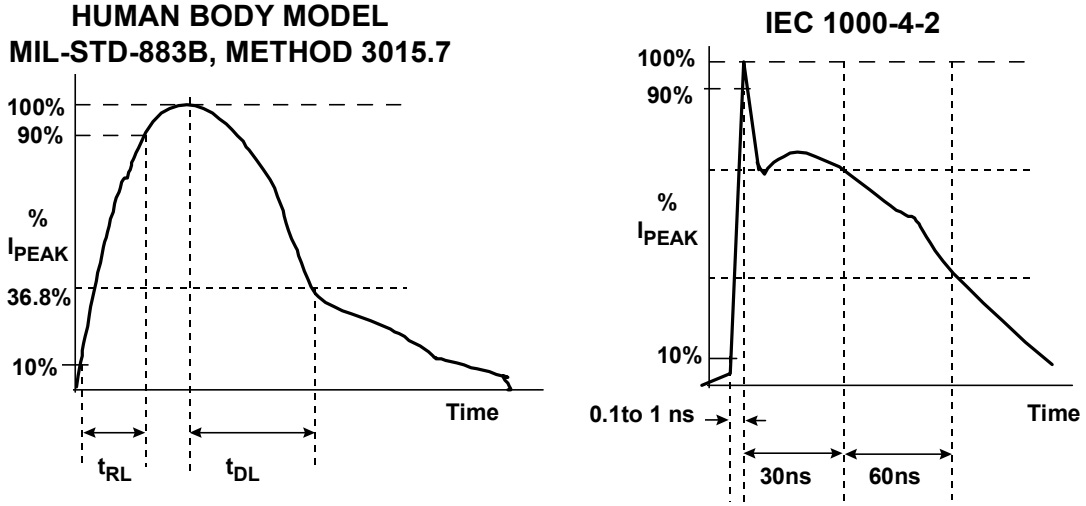
ESD TEST METHOD	R2	C1
Human Body Model MIL STD 883B Method 3015.7	1.5kΩ	100pF
IEC 1000-4-2	330Ω	150pF

NOTE: CONTACT DISCHARGE VOLTAGE SPEC FOR IEC 1000-4-2 IS ±8kV

Figure 10.67

Suitable ESD-protection design measures are relatively easy to incorporate, and most of the over-voltage protection methods previously discussed in this section will help. Additional protection can be obtained by the addition of TransZorbs at appropriate places in the system. For RS-232 and RS-485 line drivers and receivers, the ADMXXX-E series is supplied with guaranteed 15kV (HBM) ESD specifications.

MIL-STD-883B, METHOD 3015.7 HUMAN BODY MODEL AND IEC 1000-4-2 ESD WAVEFORMS



- Voltage : 8 kV
- Peak Current :
  - MIL-883B, Method 3015.7 HBM : 5 A
  - IEC 1000-4-2 : 25 A

Figure 10.68

CUSTOMER DESIGN PRECAUTIONS FOR ICs WHICH MUST OPERATE AT ESD-SUSCEPTIBLE INTERFACES

- Observe all Absolute Maximum Ratings on Data Sheet!
- Follow General Overvoltage Protection Recommendations
  - Add Series Resistance to Limit Currents
  - Add Zeners or Transient Voltage Supressors (TVS) TransZorbs™ for Extra Protection (http://www.gensemi.com)
- Purchase ESD-Specified Digital Interface Devices Such as
  - ADMXXX-E Series of RS-232 / RS-485 Drivers / Receivers (MIL-883B, Method 3015.7: 15kV, IEC 1000-4-2: 8kV)
- Read AN-397, "Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Reocurrence," by Niall Lyne - Available from Analog Devices, http://www.analog.com

Figure 10.69

REFERENCES ON ESD AND OVERVOLTAGE:

1. **Amplifier Applications Guide**, Section XI, pp. 1-10, Analog Devices, Incorporated, Norwood, MA, 1992.

2. **Systems Applications Guide**, Section 1, pp. 56-72, Analog Devices, Incorporated, Norwood, MA, 1993.

3. **Linear Design Seminar**, Section 1, pp. 19-22, Analog Devices, Incorporated, Norwood, MA, 1994.

4. **ESD Prevention Manual**, Analog Devices, Inc.

5. *MIL-STD-883 Method 3015, Electrostatic Discharge Sensitivity Classification*. Available from Standardization Document Order Desk, 700 Robbins Ave., Building #4, Section D, Philadelphia, PA 19111-5094.

6. *EIAJ ED-4701 Test Method C-111, Electrostatic Discharges*. Available from the Japan Electronics Bureau, 250 W 34th St., New York NY 10119, Attn.: Tomoko.

7. *ESD Association Standard S5.2 for Electrostatic Discharge (ESD) Sensitivity Testing -Machine Model (MM)- Component Level*. Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.

8. *ESD Association Draft Standard DS5.3 for Electrostatic Discharge (ESD) Sensitivity Testing - Charged Device Model (CDM) Component Testing*. Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.

9. Niall Lyne, *Electrical Overstress Damage to CMOS Converters*, **Application Note AN-397**, Analog Devices, 1995, http://www.analog.com.

10. *How to Reliably Protect CMOS Circuits Against Power Supply Overvoltaging*, **Application Note AN-311**, Analog Devices, http://www.analog.com

11. ADM3311E RS-232 Port Transceiver Data Sheet, Analog Devices, Inc., http://www.analog.com.

12. TransZorbs Available from General Semiconductor, Inc., 10 Melville Park Road, Melville, NY, 11747-3113, 516-847-3000, http://www.gensemi.com.

Subject Index

Analog Devices Parts Index