

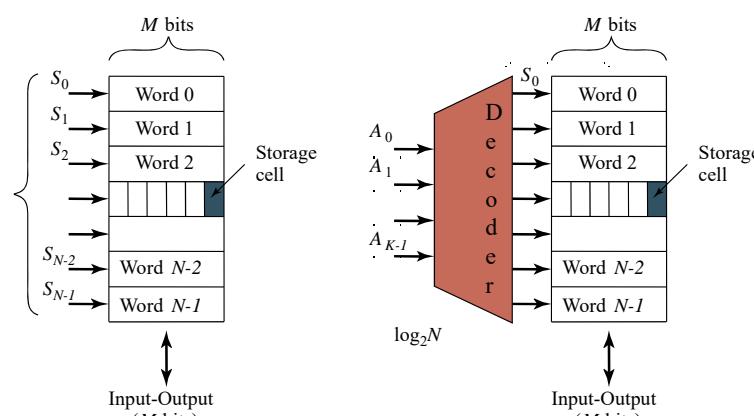
Digitalna elektronika
RAM memorije

RWM Read-Write Memory		Non-Volatile Read-Write Memory	ROM Read-Only Memory
Random Access	Non-Random Access	EPROM E ² PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

NV RWM = NV RAM

Ne gube sadržaj kada se isključi napajanje

Digitalna elektronika
RAM memorije

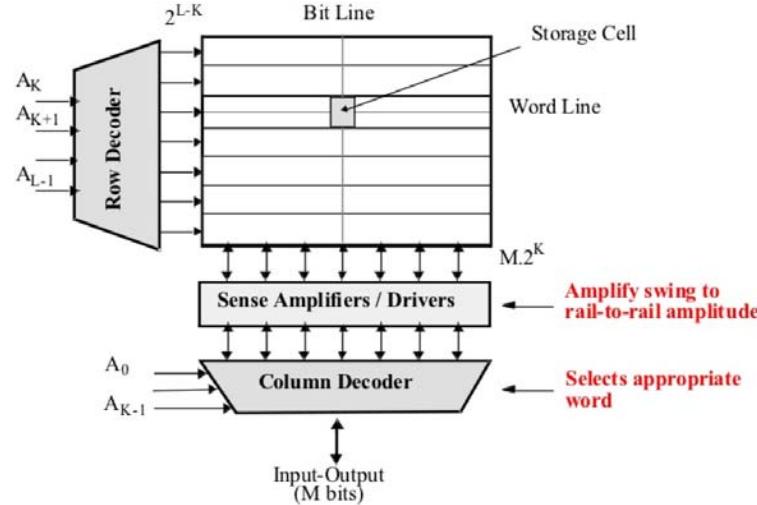


$N \times M$ memorija
 N reči == N selekcionih signala

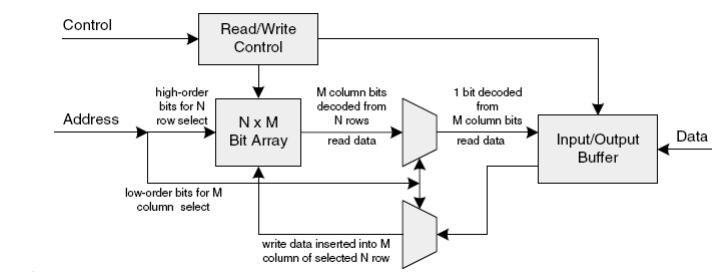
Dekoder smanjuje broj selekcionih signala
 $K = \log_2 N$

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RAM memorije

Problem: broj reči >> broja bita po reči



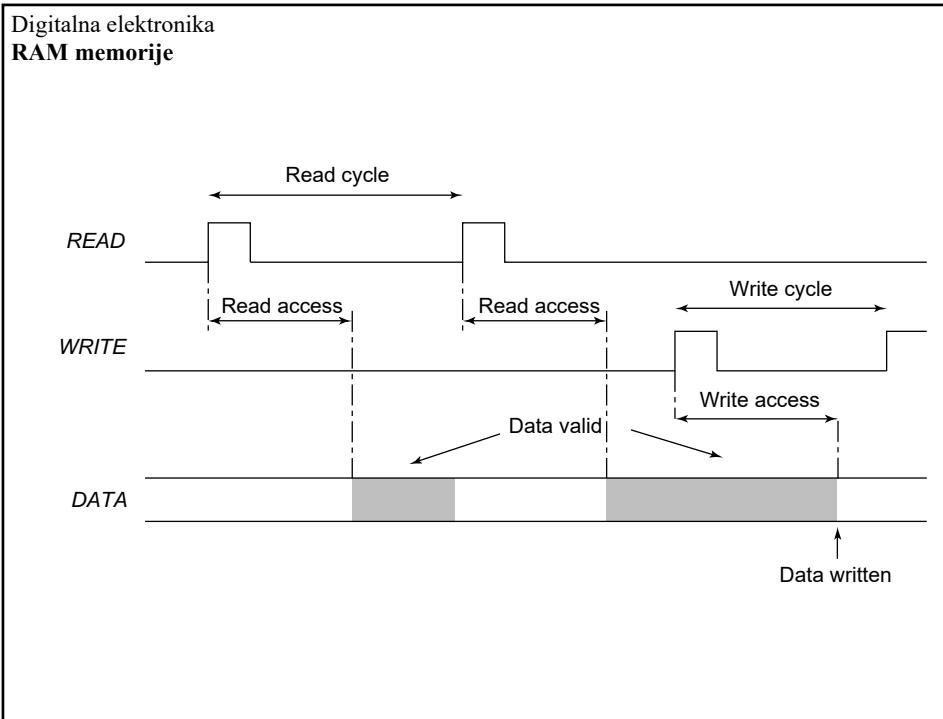
Digitalna elektronika
RAM memorije



Adresa

Podatak

Kontrolni signali



Digitalna elektronika
RAM memorije

STATIC (SRAM)

Podaci se pamte dok postoji napajanje

Velika memorijska čelija – 6 tranzistora

Brze

Memorijska čelija ima diferencijalni izlaz

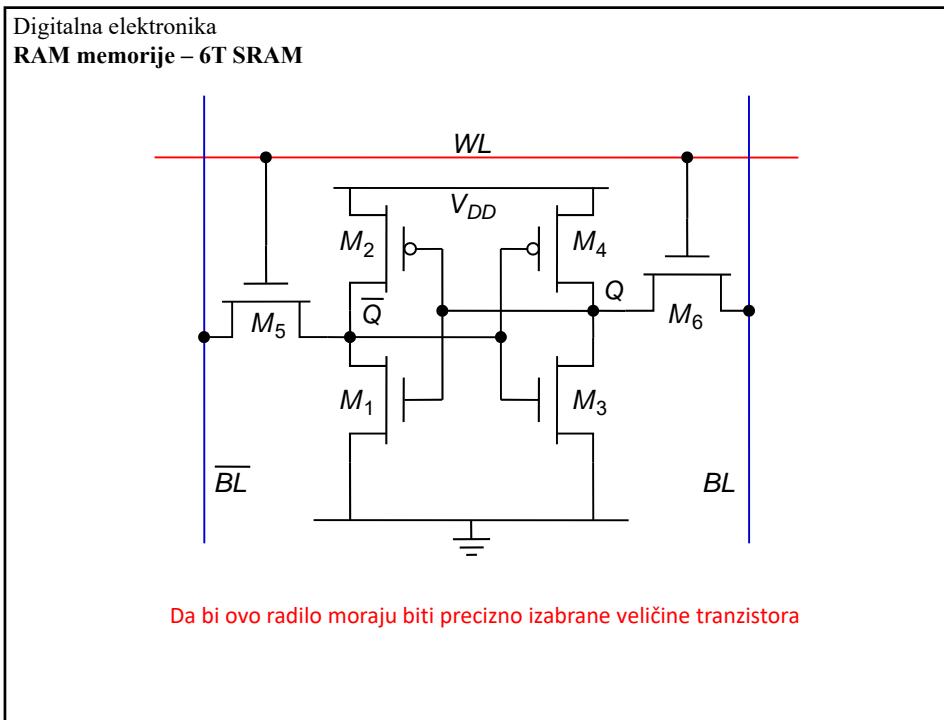
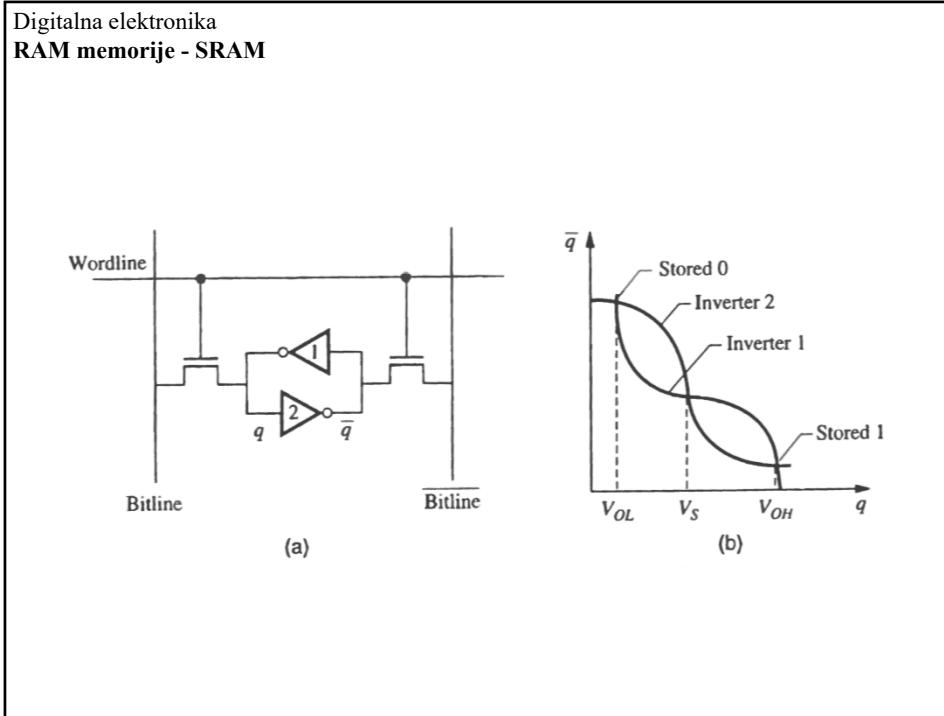
DYNAMIC (DRAM)

Da bi podatak ostao sačuvan potrebno "osvežavanje"

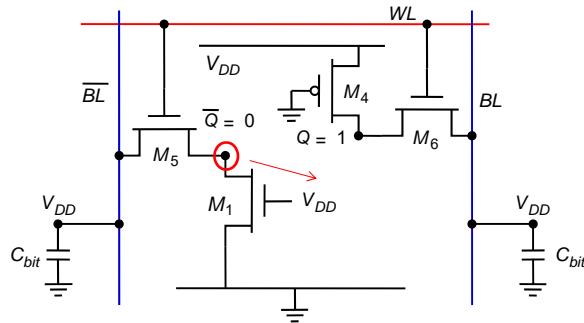
Mala memorijska čelija – 1 do 3 tranzistora

Sporije

Memorijska čelija ima jednostruki izlaz



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RAM memorije – 6T SRAM - Read



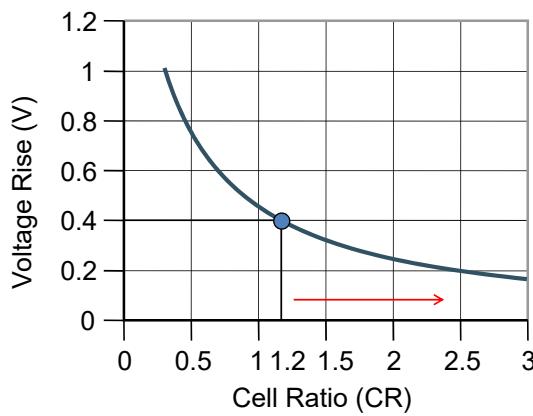
Pre aktiviranja čitanja, bitske linije na V_{DD}
 V_{DS1} ne sme da uključi M3, V_{GS3}

$$I_{D5} = \frac{B_5}{2} (V_{GS5} - V_{Th})^2 = I_{D1} = \frac{B_1}{2} (2V_{DS1}(V_{GS1} - V_{Th}) - V_{DS1}^2)$$

$$(V_{DD} - V_{DS1} - V_{Th})^2 = \frac{B_1}{B_5} (2V_{DS1}(V_{DD} - V_{Th}) - V_{DS1}^2)$$

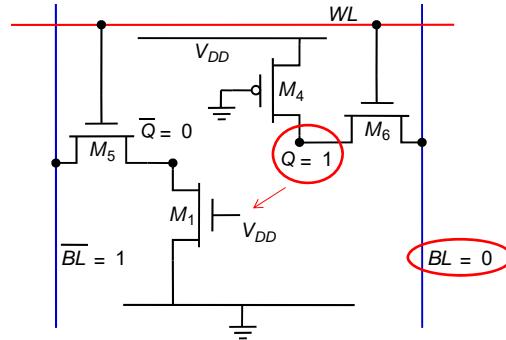
$$V_{DS1} = (V_{DD} - V_{Th}) - \sqrt{(V_{DD} - V_{Th})^2 - \frac{(V_{DD} - V_{Th})^2}{(1+CR)}}$$

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RAM memorije – 6T SRAM - Read



$$CR = \frac{W_1/L_1}{W_5/L_5}$$

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RAM memorije – 6T SRAM - Write

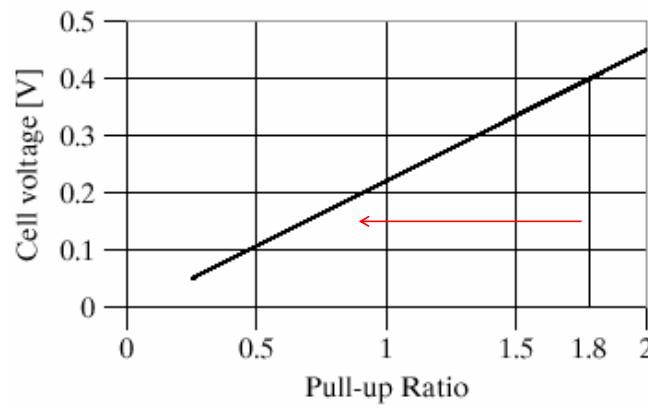


$$I_{D4} = \frac{B_4}{2} (V_{GS4} - V_{Tp})^2 = I_{D6} = \frac{B_6}{2} (2V_{DS6}(V_{GS6} - V_{Tn}) - V_{DS6}^2)$$

$$(-V_{DD} - V_{Tp})^2 = \frac{B_6}{B_4} (2V_{DS6}(V_{DD} - V_{Tn}) - V_{DS6}^2)$$

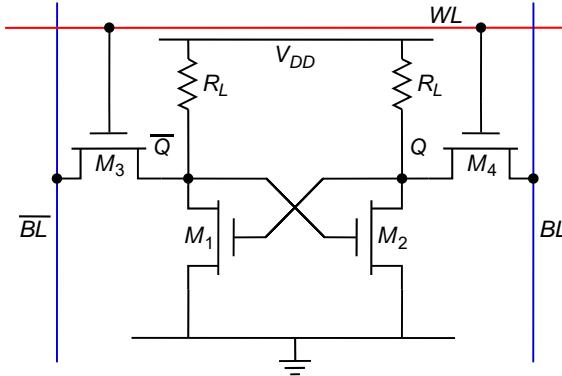
$$V_{DS6} = (V_{DD} - V_{Tn}) - \sqrt{(V_{DD} - V_{Tn})^2 - \frac{\mu_p}{\mu_n} PU (-V_{DD} - V_{Tp})^2}$$

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RAM memorije – 6T SRAM - Write



$$PU = \frac{W_4 / L_4}{W_6 / L_6}$$

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RAM memorije – Resistance load SRAM



R_L veliko da bi se smanjila struja u statičkom režimu

Koliko veliko?

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RAM memorije – TFT load SRAM

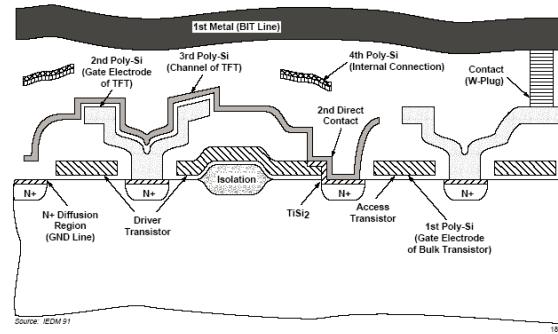
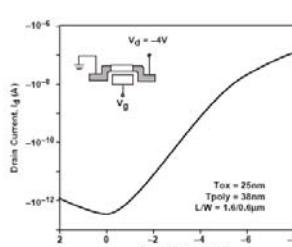


Figure 8-7. Cross Section of TFT SRAM Cell

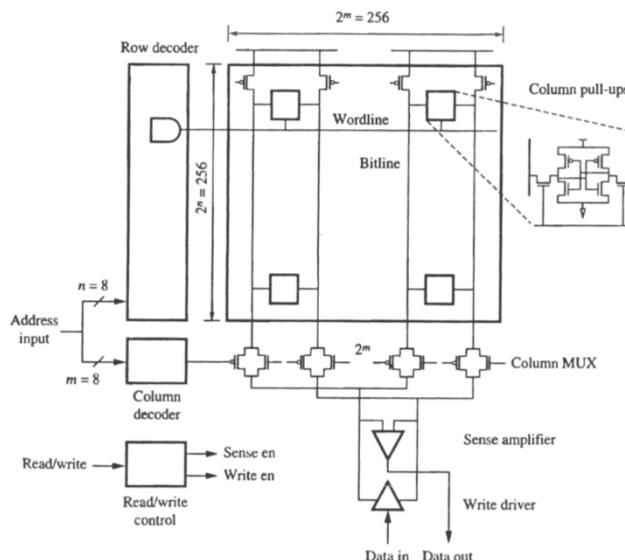
TFT - Thin Film Transistors - kao opterećenje

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RAM memorije – SRAM

Table 12-2 Comparison of CMOS SRAM cells used in 1-Mbit memory
(from [Takada91])

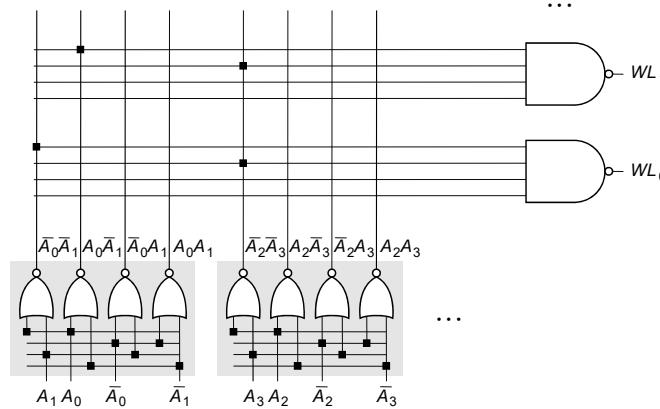
	Complementary CMOS	Resistive Load	TFT Cell
Number of transistors	6	4	4 (+2 TFT)
Cell size	$58.2 \mu\text{m}^2$ (0.7- μm rule)	$40.8 \mu\text{m}^2$ (0.7- μm rule)	$41.1 \mu\text{m}^2$ (0.8- μm rule)
Standby current (per cell)	10^{-15} A	10^{-12} A	10^{-13} A

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RAM memorije – SRAM

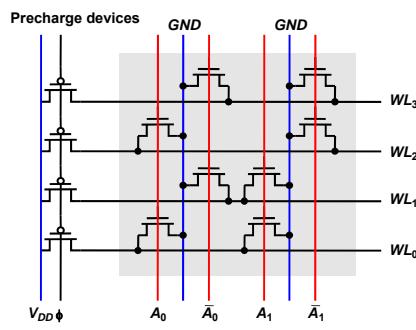


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RAM memorije – SRAM - dekoderi

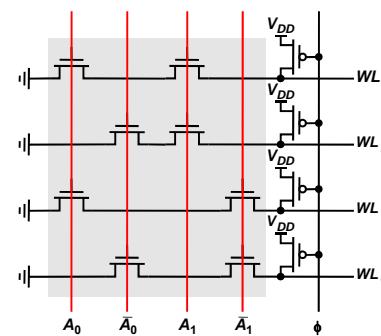
U više nivoa



Digitalna elektronika
RAM memorije – SRAM - dekoderi

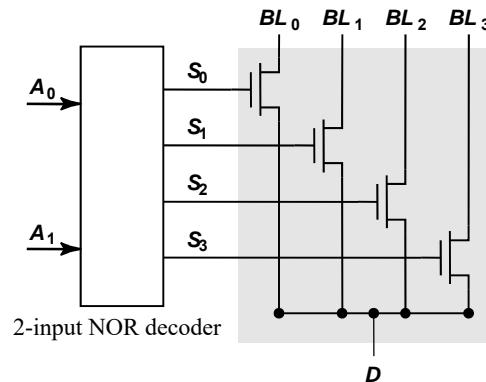


2-input NOR decoder



2-input NAND decoder

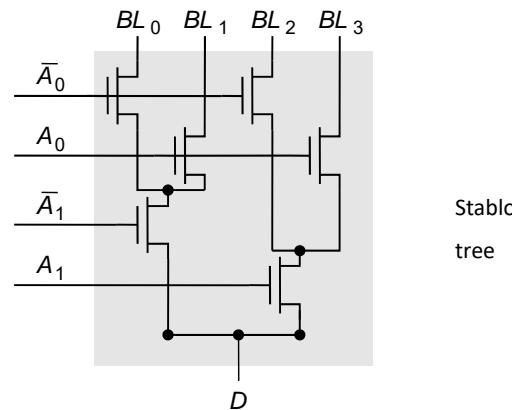
Digitalna elektronika
RAM memorije – SRAM - dekoderi



Prednost: brzina - samo jedan tranzistor na putanji podatka

Manja: Veliki broj tranzistora

Digitalna elektronika
RAM memorije – SRAM - dekoderi

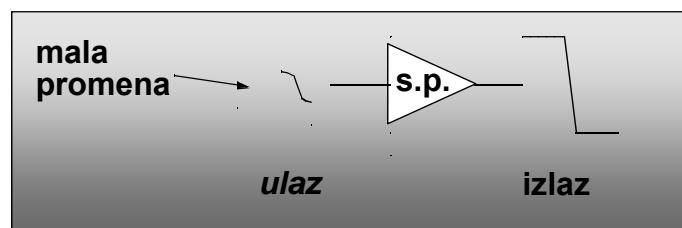


Broj tranzistora znatno manji, ali raste vreme propagacije

Rešenje je kombinacija prethodnih slučajeva, arhitektura memorije, baferi

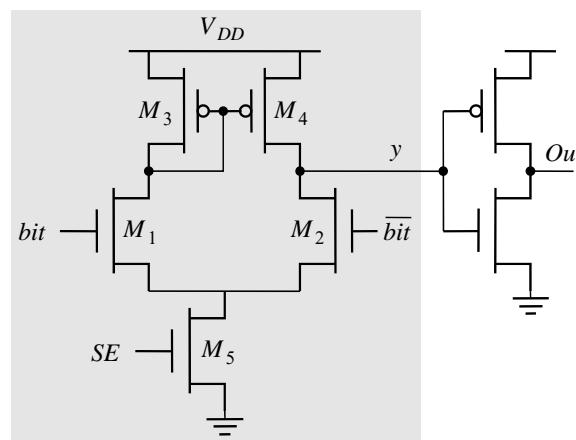
Digitalna elektronika
RAM memorije – SRAM – senzorski pojačavači

$$t_p = \frac{C \cdot \Delta V}{I_{av}}$$

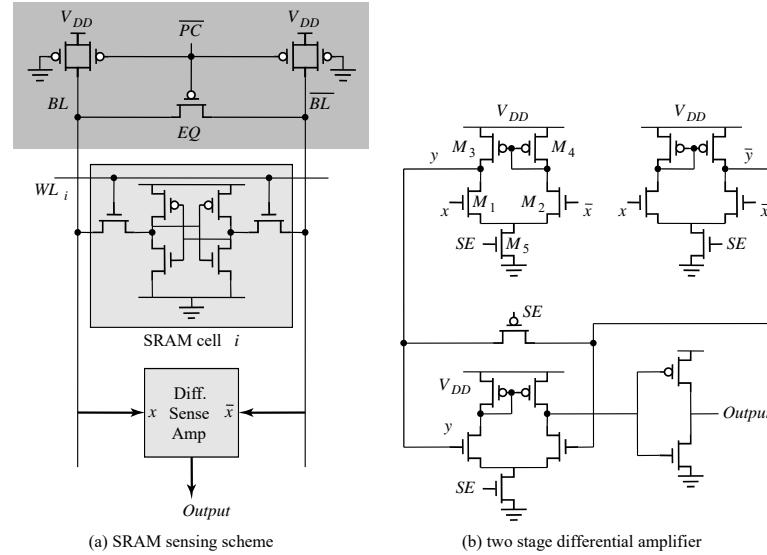


Digitalna elektronika

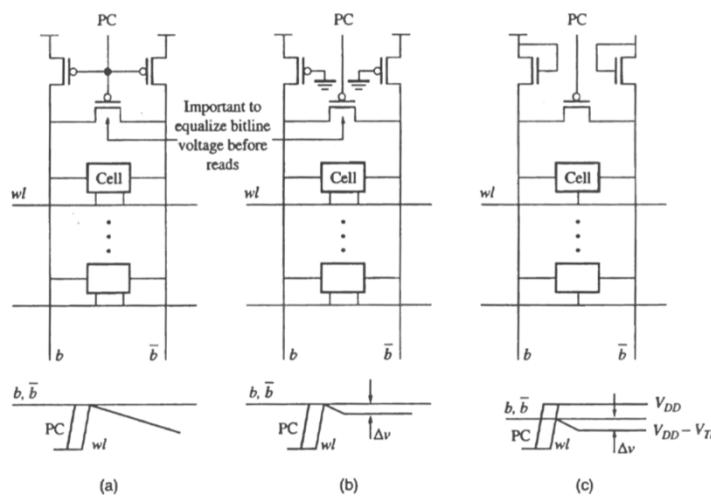
RAM memorije – SRAM – senzorski pojačavači



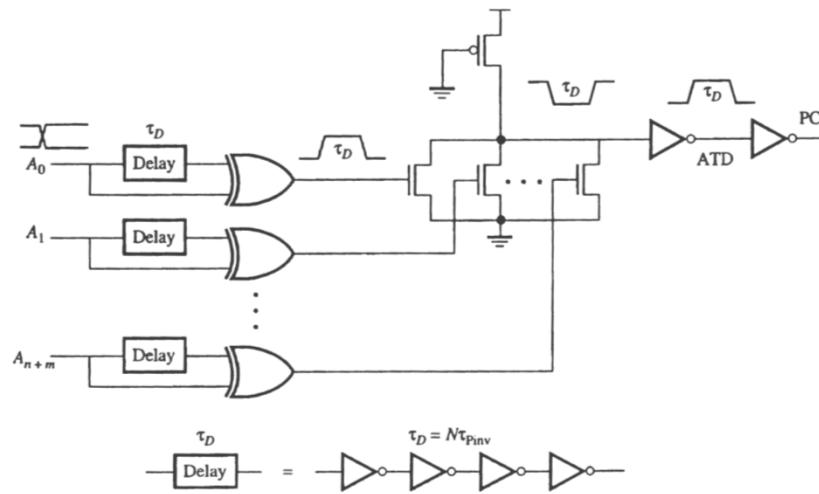
Digitalna elektronika
RAM memorije – SRAM – senzorski pojačavači



Digitalna elektronika
RAM memorije – SRAM – precharge

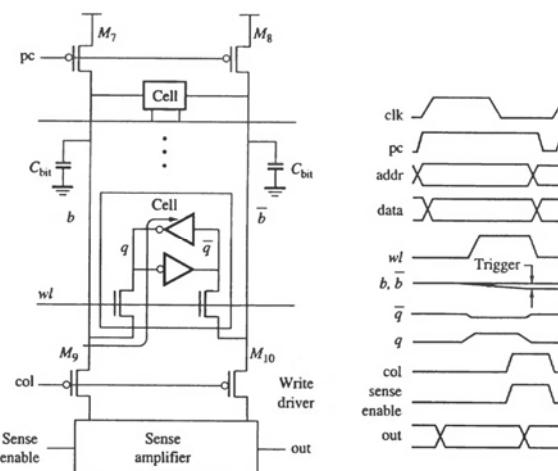


Digitalna elektronika
RAM memorije – SRAM – precharge



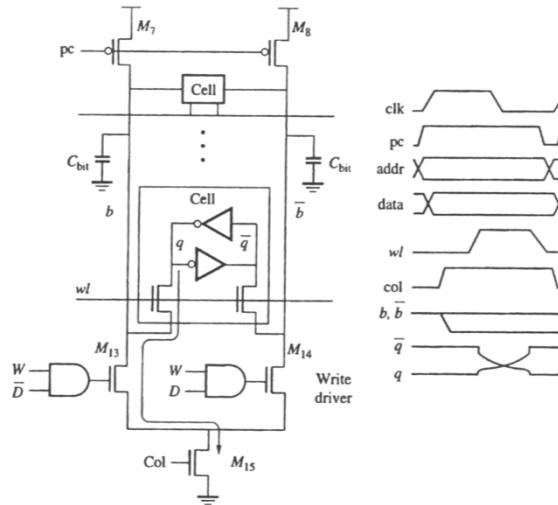
Detekcija promene adrese

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RAM memorije – SRAM – Read



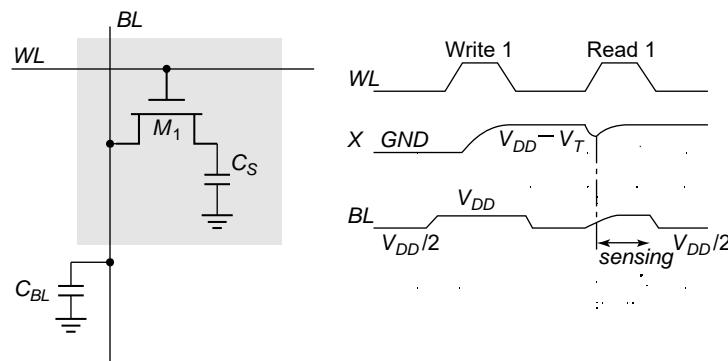
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RAM memorije – SRAM – Write



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RAM memorije – 1T DRAM



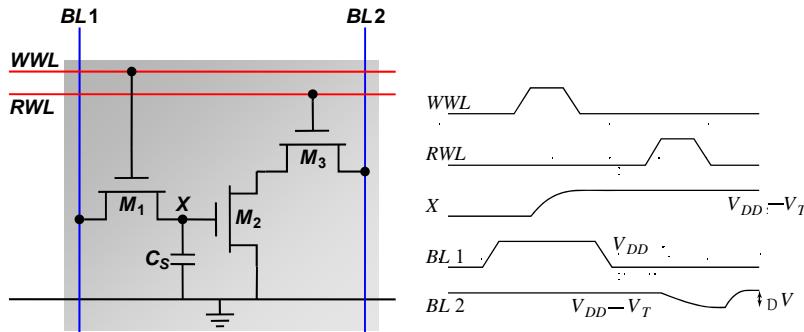
Write: C_S se puni i prazni aktiviranjem WL and BL.
Read: razmena nanelektrisanja C_S i C_{BL}

$$\Delta V = V_{BL} - V_{PRE} = (V_{BIT} - V_{PRE}) \frac{C_S}{C_S + C_{BL}}$$

Promena napona 250 mV.

Destruktivno!!!

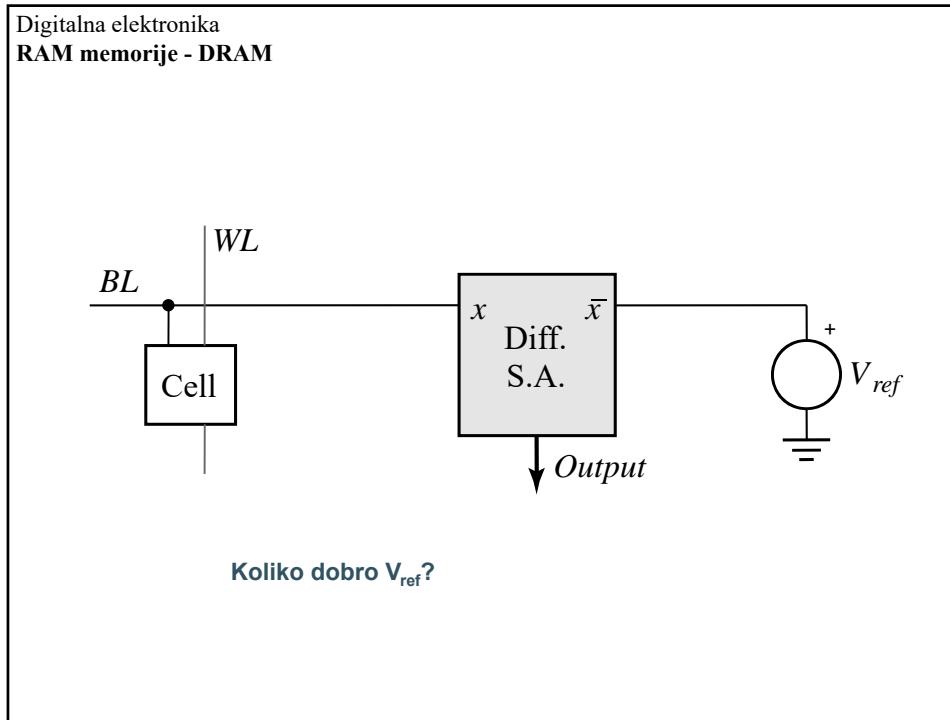
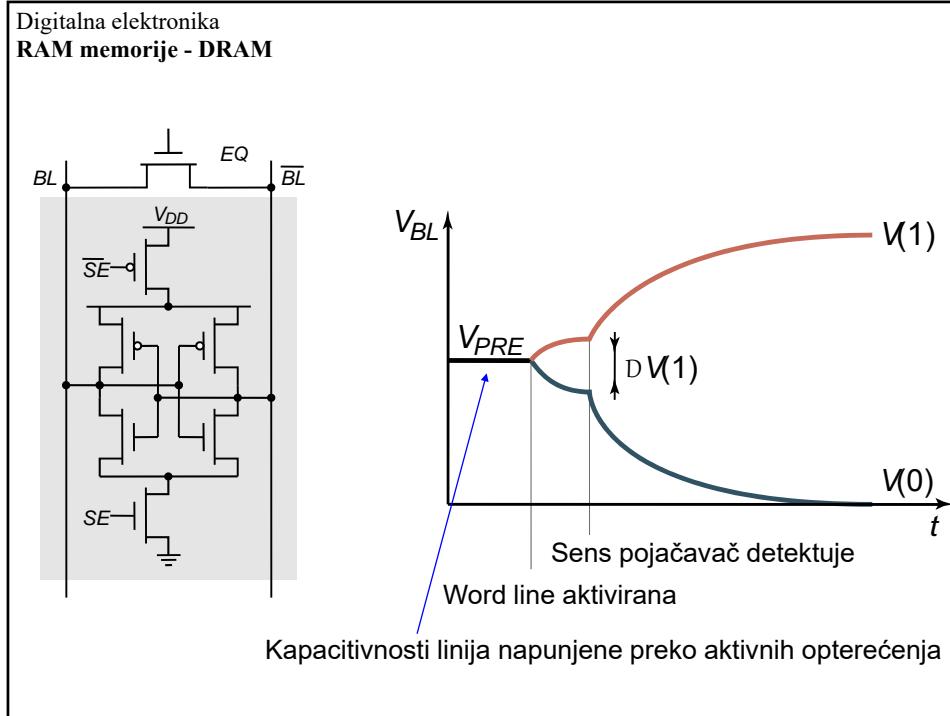
Digitalna elektronika
RAM memorije – 3T DRAM



NEDestruktivno!!!

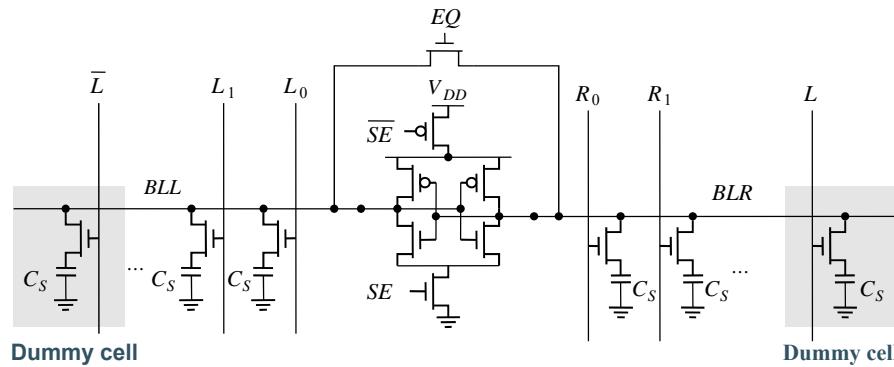
Digitalna elektronika
RAM memorije – DRAM

- 1T DRAM zahteva senzorski pojačavač
- DRAM memorijska čelija je sa jednostrukim izlazom - single ended.
- SRAM čelija je sa diferencijalnim izlazom.
- Čitanje 1T DRAM čelije je destruktivno; čitanje odnosno osvežavanje je neophodno.
- Za razliku od 3T čelije, 1T čelija zahteva dodatnu kapacitivnost.
- Kada se upisuje “1” u DRAM čeliju napona na kondenzatoru je manji za napon praga MOS tranzistora, manje nanelektrisanja, $V_{wl} > VDD$



Digitalna elektronika

RAM memorije – DRAM – open bitline



Digitalna elektronika

RAM memorije – DRAM – open bitline

