Digitalna elektronika
Programabilne logičke komponente

Logičke komponente se mogu klasifikovati u dve velike grupe

- fiksne
- programabilne

Fiksne – kada su proizvedene određena im je logička funkcija i ne može se menjati

Programabilne – korisnik može da ih prilagodi, programira, za određenu logičku finkciju

Digitalna elektronika
Programabilne logičke komponente

Šta je ideja?

Bilo koja logička funkcija može da se predstavi u obliku sume proizvoda!

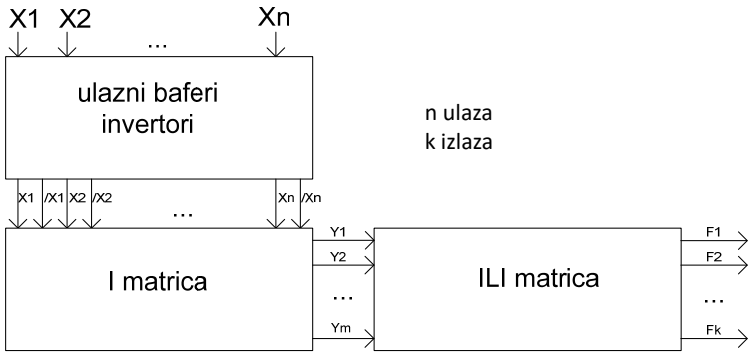
I + ILI (ako ima NE)

Šta treba?

Dovoljan broj ulaza.
Dovoljan broj izlaza.

Mogućnost programiranja I-ILI povezanosti.

Digitalna elektronika
Programabilne logičke komponente



Šta i koliko može da se programira zavisi od tipa komponente.

Da li su obe matrice programabilne?
Da li je samo I odnosno ILI matrica programabilna?
Koliko su programabilne?
Šta može da učestvuje u Y i koliko ih ima (m?)? Koliko ulaza u I kola.
Šta može da učestvuje u F i koliko? Koliko ulaza u ILI kola.

Digitalna elektronika
Programabilne logičke komponente

PLA – Programmable Logic Array
PAL – Programmable Array Logic
GAL – Generic Array Logic
} PLD

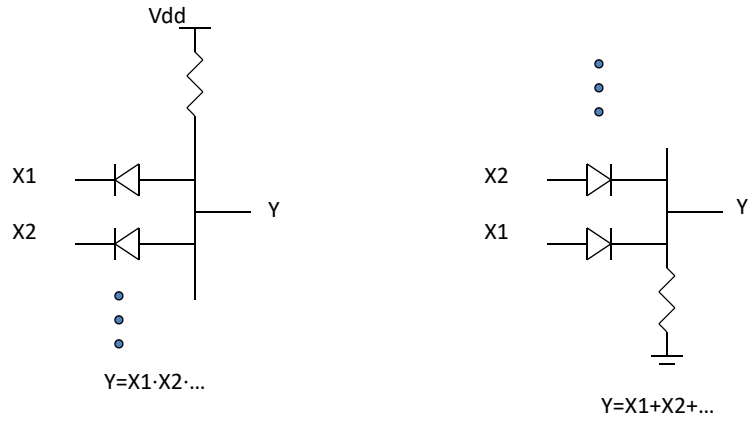
CPLD – Complex Programmable Logic Device
FPGA– Fild Programmable Gate Array
} CPLD

ROM – Read Only Memory
PROM – Programmable ROM
EPROM – Erasable PROM
EEPROM – Electrically EPROM
} Memory

ASIC– Application Specific Integrated Circuit } ASIC

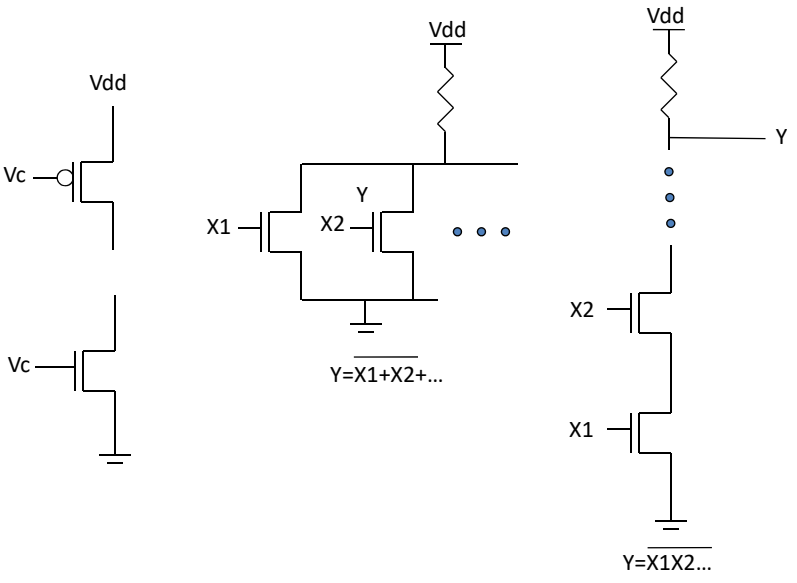
Digitalna elektronika
Programabilne logičke komponente

Kako realizovati kola sa puno ulaza?



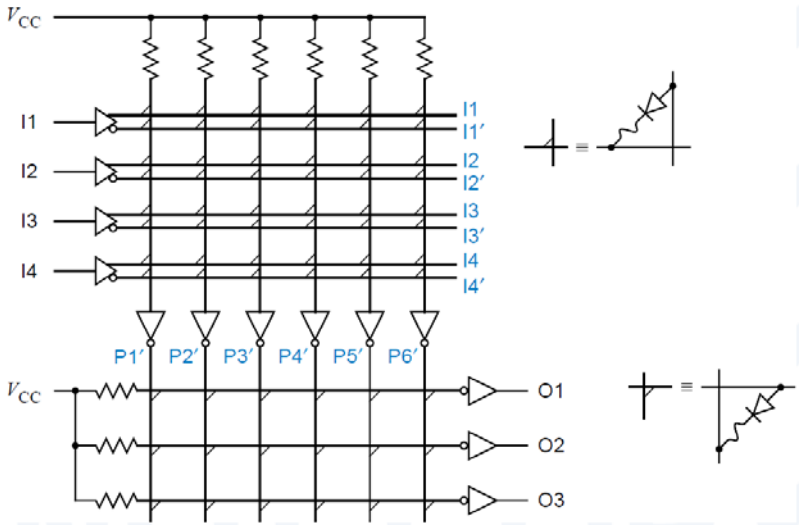
Digitalna elektronika
Programabilne logičke komponente

Kako realizovati kola sa puno ulaza?



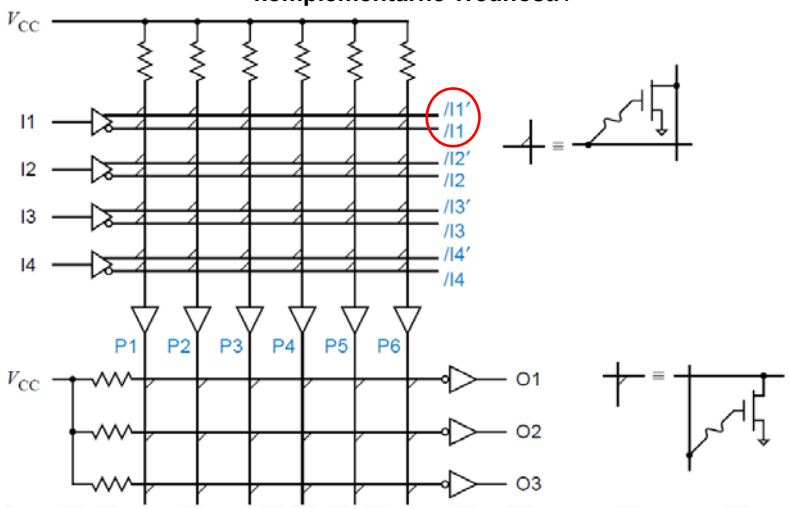
Digitalna elektronika
Programabilne logičke komponente

Kako lako realizovati logička kola sa puno ulaza a da imamo mogućnost programiranja?



Digitalna elektronika
Programabilne logičke komponente

Kako se u ovom slučaju dovode ulazi i komplementarne vrednosti?



Digitalna elektronika
Programabilne logičke komponente

U fazi predproizvodnje predvidimo svuda veze.

Ali za deo proizvodnje koji definiše veze

napravimo posebnu masku

IMA-NEMA veze

Nema veze -> ulaz ispada iz logičke funkcije

Ima veze -> ulaz formira logičke funkcije

MASK

Programmable

U fazi proizvodnje predvidimo i napravimo svuda veze.

U fazi programiranja Vcc -> Vpp Vpp > Vcc

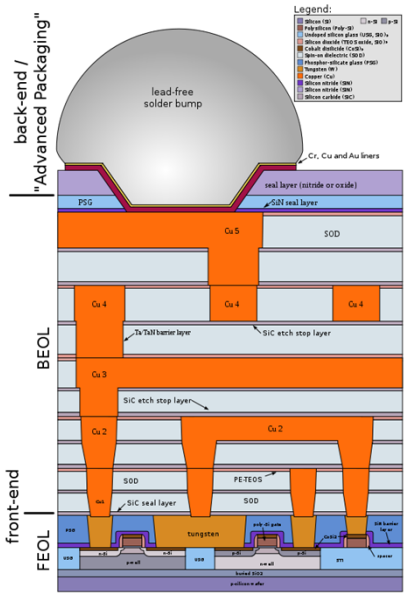
Spaljena veza, osigurač -> ulaz ispada iz logičke funkcije

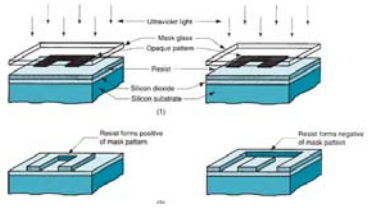
Ostala veza, osigurač -> ulaz formira logičke funkcije

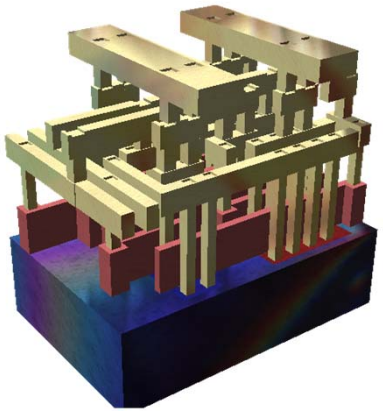
FUSE

Programmable

Digitalna elektronika
Programabilne logičke komponente

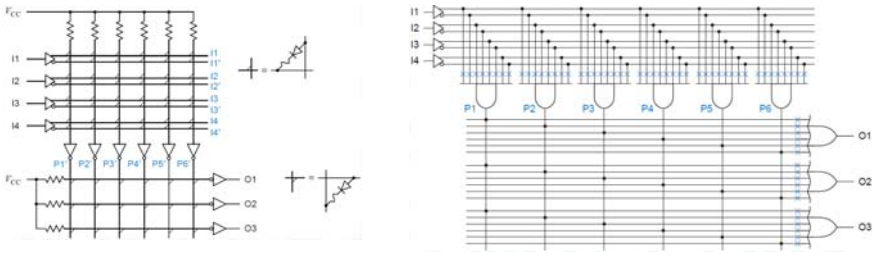


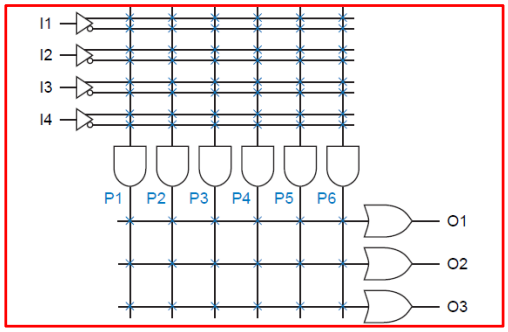




Digitalna elektronika
Programabilne logičke komponente

Kako simbolički crtati?





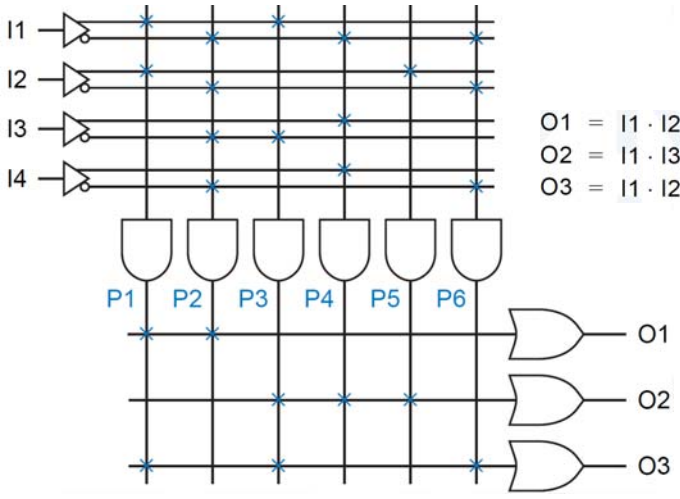
4 ulaza
3 izlaza

Programabilna I matrica
sa 6 izlaza

Programabilna ILI matrica
sa mogućnošću sabiranja
6 ulaza po izlazu

Digitalna elektronika
Programabilne logičke komponente

Primer realizacije logičkih funkcija



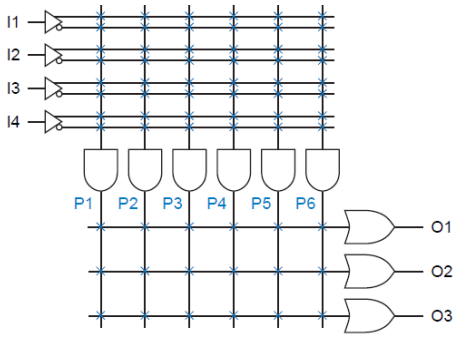
$$O1 = I1 \cdot I2 + I1' \cdot I2' \cdot I3' \cdot I4'$$
$$O2 = I1 \cdot I3' + I1' \cdot I3 \cdot I4 + I2$$
$$O3 = I1 \cdot I2 + I1 \cdot I3' + I1' \cdot I2' \cdot I4'$$

Digitalna elektronika

Programabilne logičke komponente - PLA

Programabilna I matrica

Programabilna ILI matrica



Broj ulaza

Broj izlaza

Broj mogućih logičkih proizvoda

Jedanput formiran logički proizvod

može se koristiti za realizaciju bilo koje izlazne logičke funkcije

Digitalna elektronika

Programabilne logičke komponente - PAL

Programabilna I matrica

Fiksna ILI matrica

Broj ulaza

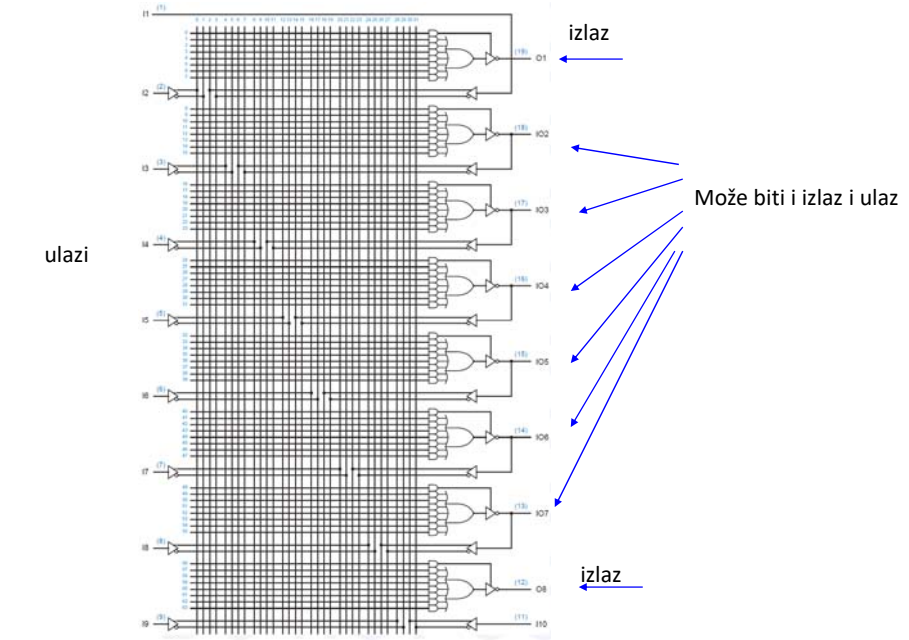
Broj izlaza

Broj mogućih logičkih proizvoda po izlazu

Jedanput formiran logički proizvod NE može se koristiti za realizaciju bilo koje izlazne logičke funkcije. Ako je potreban na više izlaza, mora se formirati po svakom izlazu.

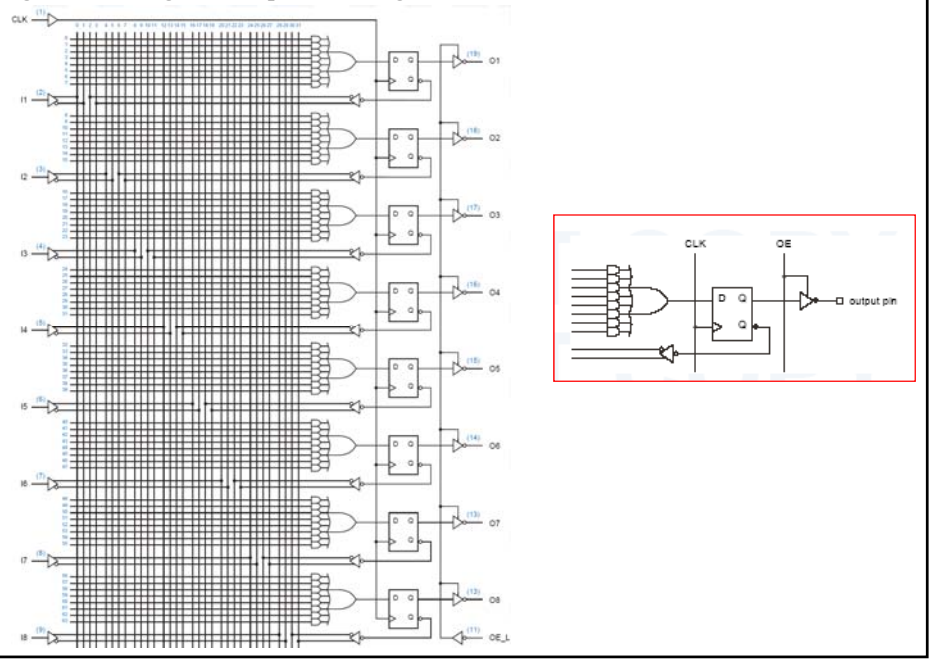
Digitalna elektronika

Programabilne logičke komponente – logički PAL



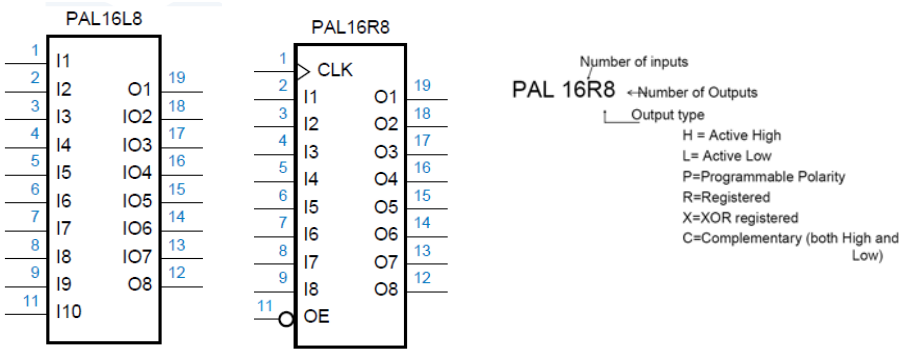
Digitalna elektronika

Programabilne logičke komponente – registarski PAL



Digitalna elektronika

Programabilne logičke komponente – oznake PAL komponenti



Ne može se sve saznati iz oznake !!!

16L8 (ne govori ništa o unutrašnjoj strukturi – npr koliko proizvoda može da se sabere po izlazu

Maksimalno 16 ulaza

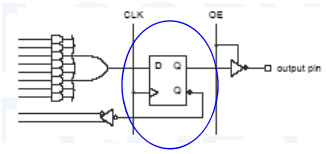
16R8?

Maksimalno 8 izlaza

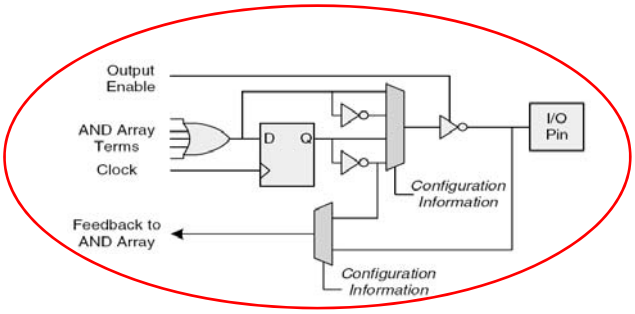
Izlazi su sa aktivnom logičkom nulom (invertor na izlazu)

Digitalna elektronika

Programabilne logičke komponente - GAL



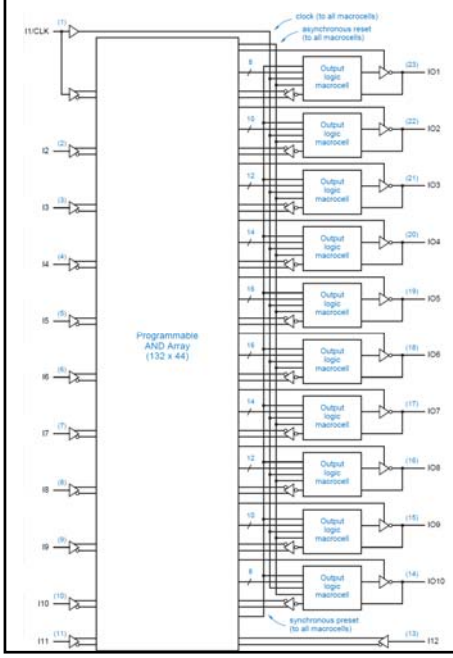
Na izlazu registarskog PALa

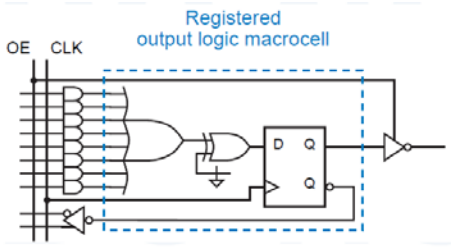


Na izlazu GALa

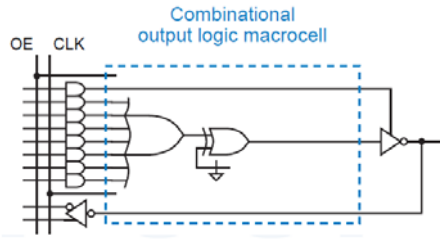
Makroćelija

Digitalna elektronika
Programabilne logičke komponente - GAL



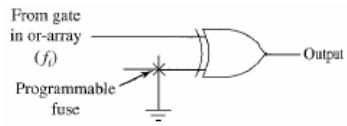


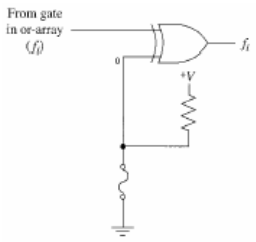
Konfigurisana makroćelija kao

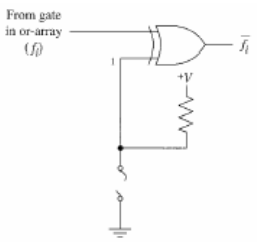


Digitalna elektronika
Programabilne logičke komponente - GAL

Inverted Non-Inverted Output

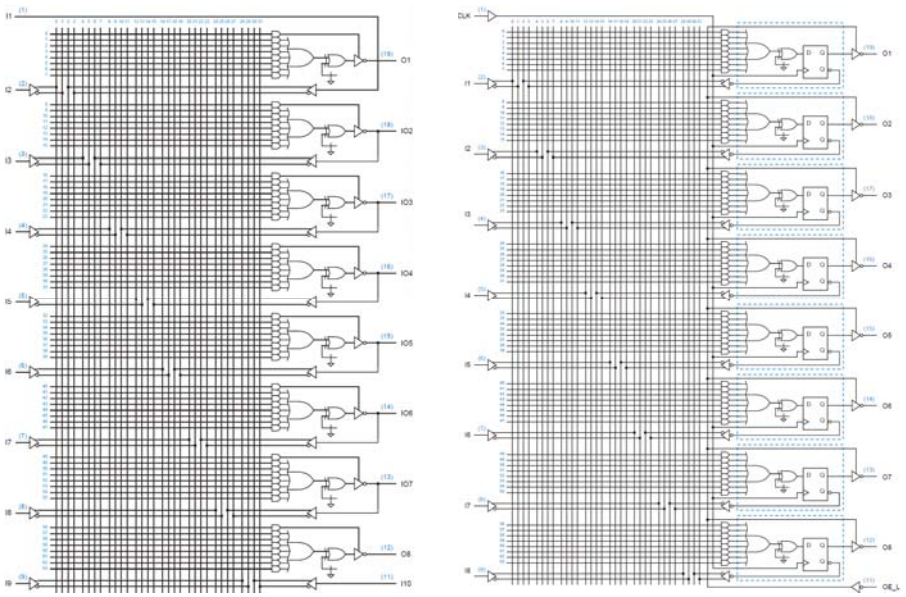






Digitalna elektronika

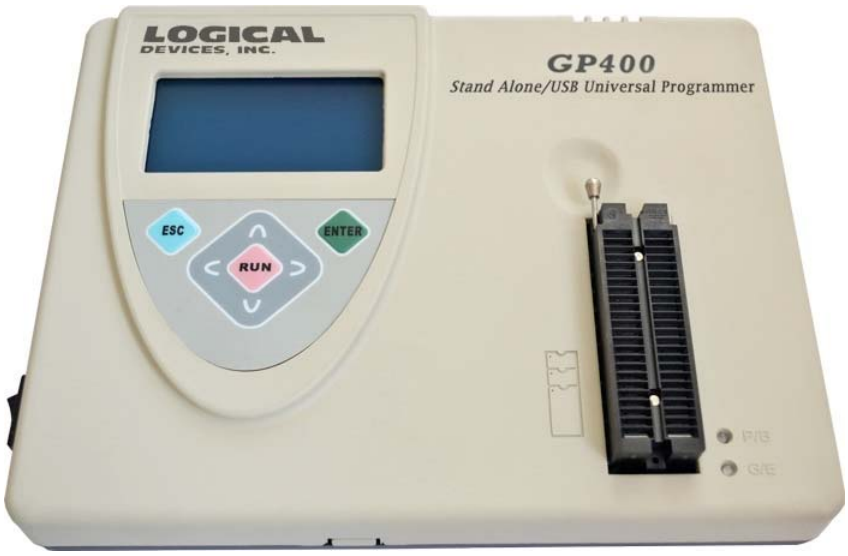
Programabilne logičke komponente - GAL



Svi izlazi logički | Međuvarijante | Svi izlazi registarski

Digitalna elektronika

Programabilne logičke komponente - Programiranje



Digitalna elektronika
Programabilne logičke komponente - Programiranje

JEDEC

- JEDEC files are used to specify the fuses that will be burned or connected to each AND gate.

```
□
CUPL(WM)        5.0a  Serial# 60000009
Device          g16v8as  Library DLIB-h-40-2
Created         Tue Sep 26 15:12:26 2006
Name            Decoder
Partno          00
Revision        01
Date            2/17/2005
Designer        F.Rios
Company         UMD
Assembly        None
Location
*QP20
*Q92194
*G0
*F0
*L00000 11011111111111111111111111111101
*L00032 01111111111111111111111111111101
*L00064 11110111111111111111111111111101
*L00096 11111111101111111111101111111101
*L00128 11111111101111101111111111111101
*L00160 11111111101101111111111111111101
*L00192 10101011011111111111111111111110
*L00224 10101011111110111011011111111110
*L00256 11101111111111111111111111111101
*L00288 01111111111111111111111111111101
*L00320 11110111111111111111111111111101
```

Number of total fuses

Number of fuse

1 = Blown fuse, no connection
0 = Intact fuse, connected

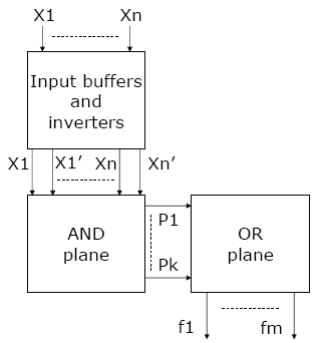
Digitalna elektronika
Programabilne logičke komponente - Programiranje

ABEL

```
module TIMEGEN6
title 'Six-phase Master Timing Generator'

" Input and Output pins
MCLK, RESET, RUN, RESTART                    pin;
T1, P1_L, P2_L, P3_L, P4_L, P5_L, P6_L       pin istype 'reg';

" State definitions
PHASES = [P1_L, P2_L, P3_L, P4_L, P5_L, P6_L];
NEXTPH = [P6_L, P1_L, P2_L, P3_L, P4_L, P5_L];
SRESET = [1, 1, 1, 1, 1, 1];
P1 =     [0, 1, 1, 1, 1, 1];

equations
T1.CLK = MCLK; PHASES.CLK = MCLK;

WHEN RESET THEN {T1 := 1; PHASES := SRESET;}
ELSE WHEN (PHASES==SRESET) # RESTART THEN {T1 := 1; PHASES := P1;}
ELSE WHEN RUN & T1 THEN {T1 := 0; PHASES := PHASES;}
ELSE WHEN RUN & !T1 THEN {T1 := 1; PHASES := NEXTPH;}
ELSE {T1 := T1; PHASES := PHASES;}

end TIMEGEN6
```

Digitalna elektronika

Programabilne logičke komponente - ROM



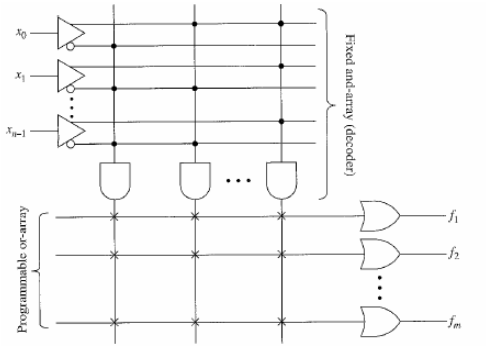
$k=2^n$

I matrica fiksna u obliku potpunog dekoder!!!

Zašto?

Imamo na raspolaganju sve moguće logičke proizvode od datih ulaznih promenljivih.

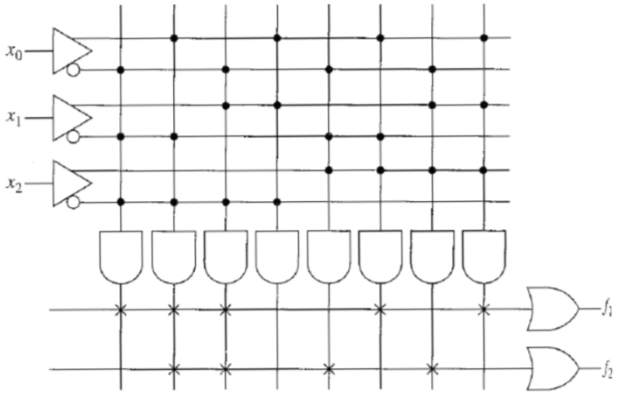
ILI matrica programabilna!!!



Digitalna elektronika

Programabilne logičke komponente - ROM

x_2	x_1	x_0	f_1	f_2
0	0	0	1	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

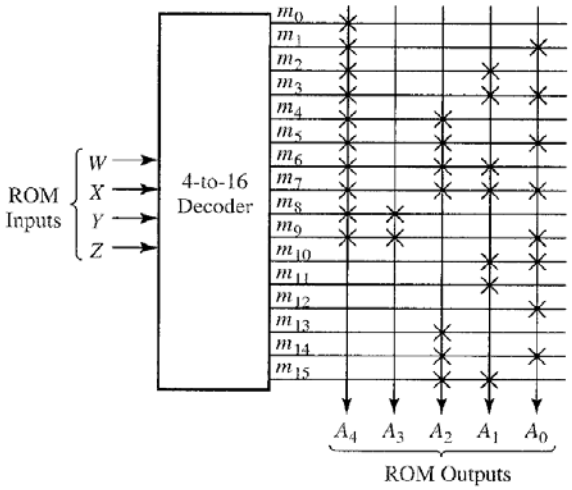


Logička komponenata
Ulazi $x_0\, x_1\, x_2$
Izlazi $f_1\, f_2$
....

Memorija
Ulazi $x_2\, x_1\, x_0$ =adresa
Izlazi $f_1\, f_2$ =podatak
svaka vrsta = memorijska lokacija
i podatak na toj memorisjkoj lokaciji

Digitalna elektronika
Programabilne logičke komponente - ROM

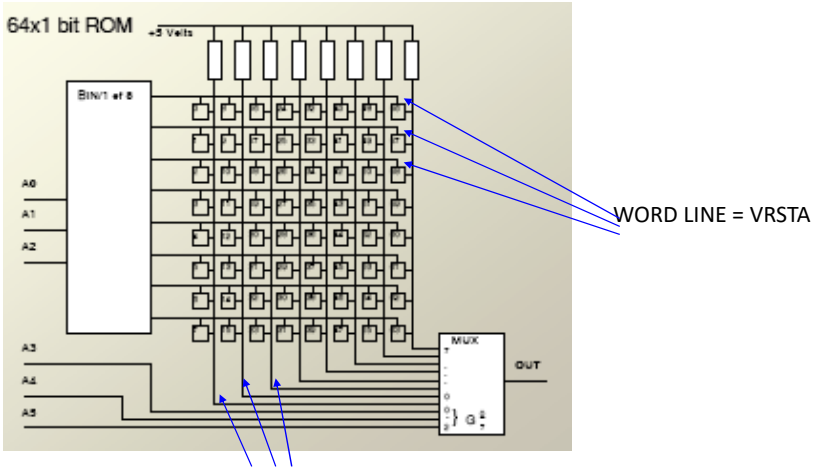
Primer sa isprogramiranim, memorisanim, sadržajem



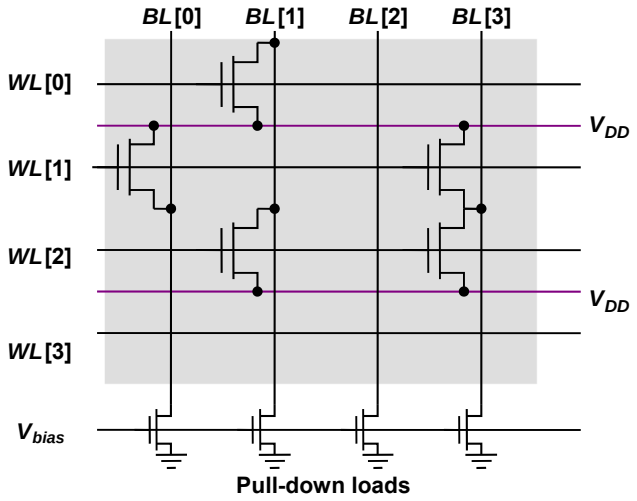
Digitalna elektronika
Programabilne logičke komponente - ROM

Da bi se što više iskoristio prostor "memorijska matrica" što približnije kvadratu

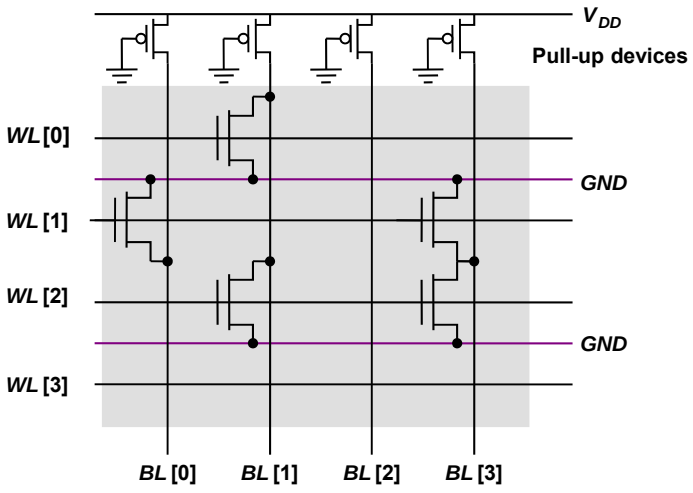
"memorijska matrica" deo koji se programira – ILI matrica



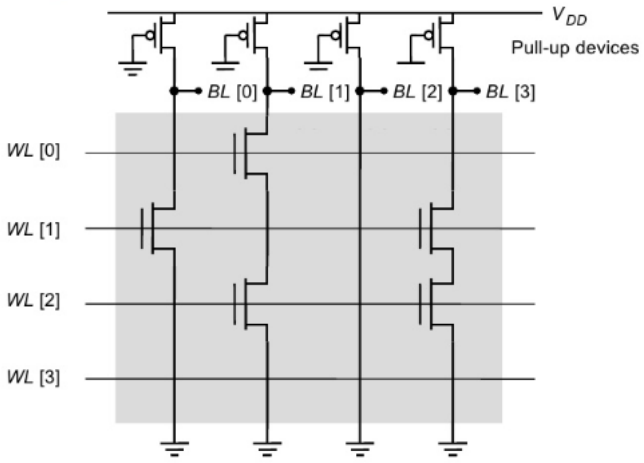
Digitalna elektronika
Programabilne logičke komponente – ROM



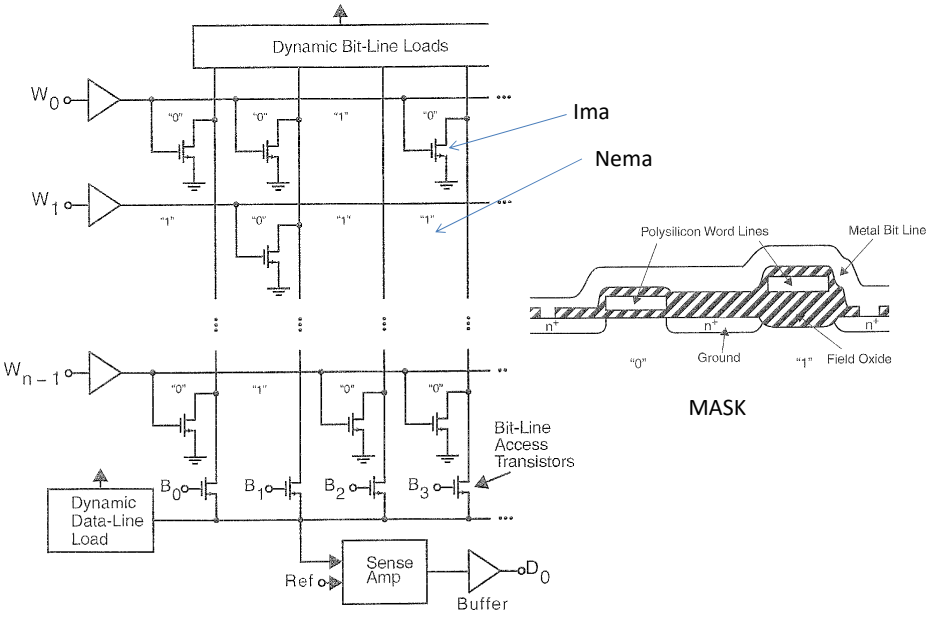
Digitalna elektronika
Programabilne logičke komponente – NOR ROM



Digitalna elektronika
Programabilne logičke komponente – NAND ROM

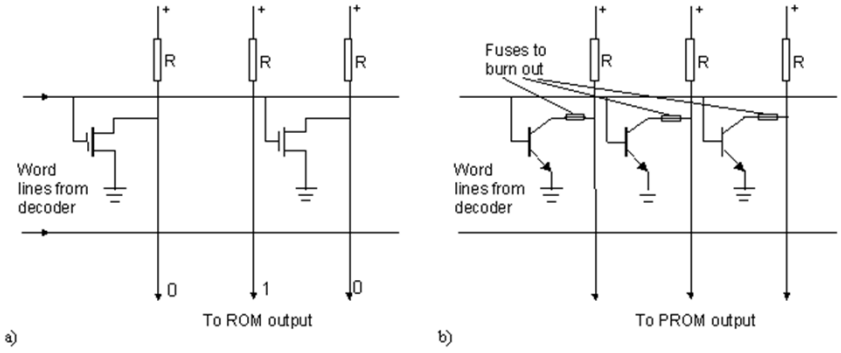


Digitalna elektronika
Programabilne logičke komponente - ROM



Digitalna elektronika

Programabilne logičke komponente – ROM programiranje

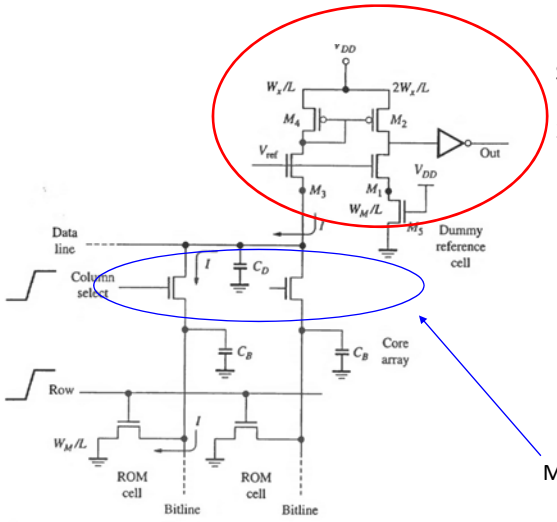


MASK ROM

FUSE PROM

Digitalna elektronika

Programabilne logičke komponente – ROM – senzorski pojačavač

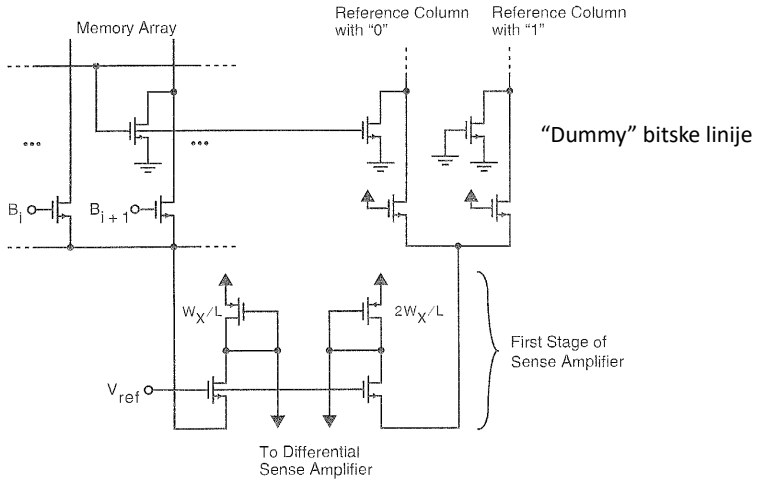


Senzorski pojačavač
1. Da ubrza očitavanje
2. Očitavanje pouzdano

Multiplekser?

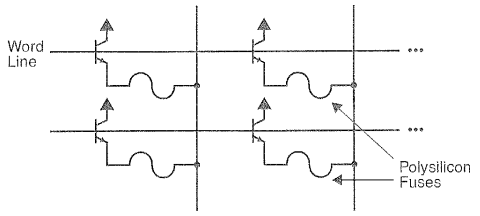
Digitalna elektronika

Programabilne logičke komponente – ROM – senzorski pojačavač

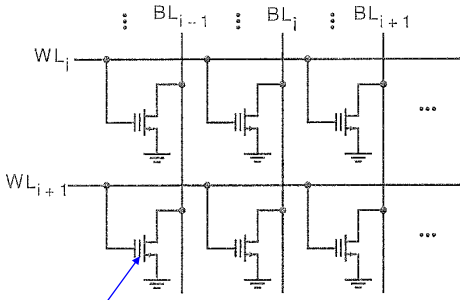


Digitalna elektronika

Programabilne logičke komponente – PROM



BIPOLARNI



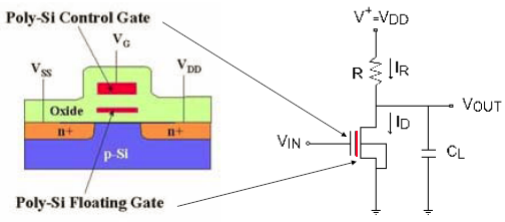
NMOS

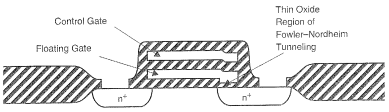
A šta su ove crtice, gde su osigurači?

Digitalna elektronika
Programabilne logičke komponente – PROM

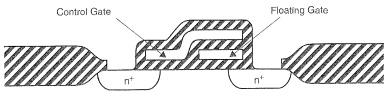
Floating Gate Inverter

FAMOS – Floating Gate Avalanche Injection MOS





FLOTOX – FLOating gate Tunneling Oxid



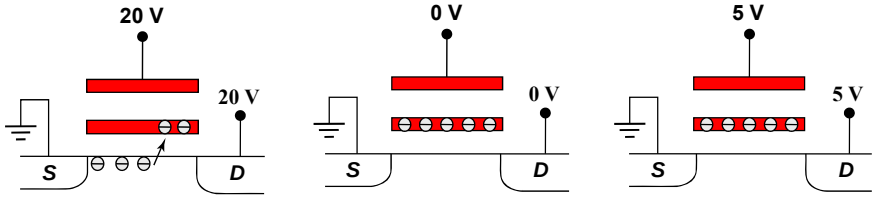
Kako ubaciti naelektrisanje na izolovani gejt?

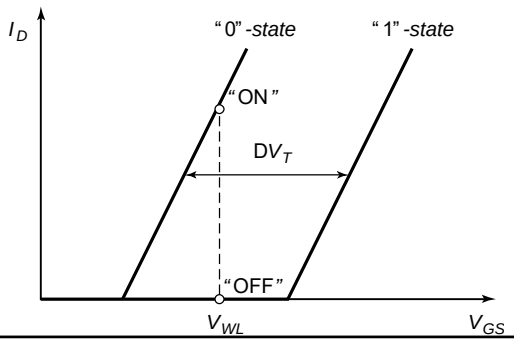
Channel hot electron current

Channel initiated secondary electron current

Fowler-Nordheim tunneling current

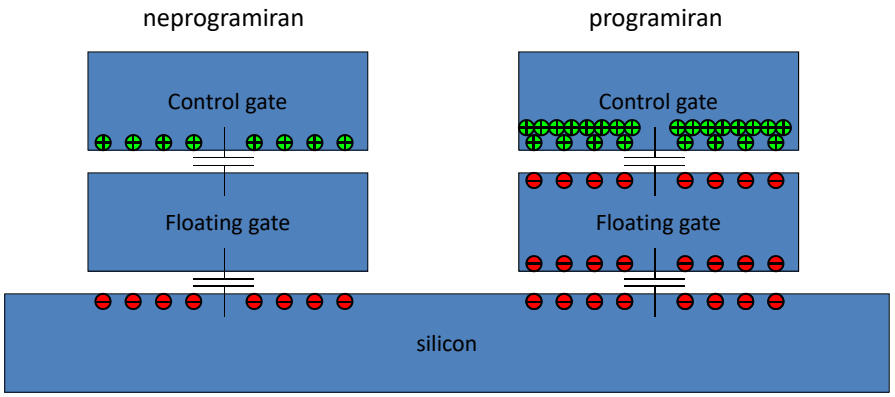
Digitalna elektronika
Programabilne logičke komponente – PROM - programiranje





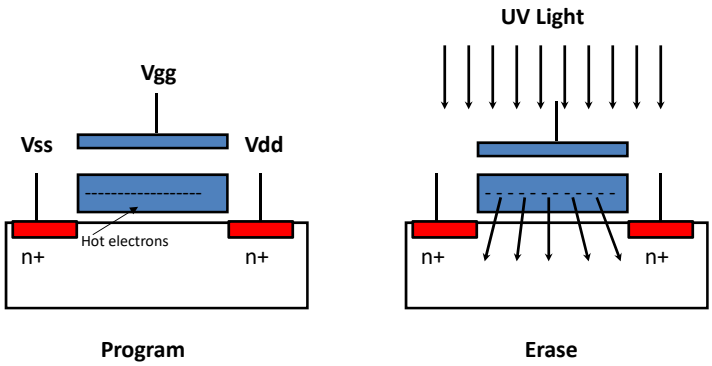
Digitalna elektronika

Programabilne logičke komponente – PROM - programiranje



Digitalna elektronika

Programabilne logičke komponente – EPROM - brisanje



Digitalna elektronika
Programabilne logičke komponente – EPROM - brisanje

EPROMs

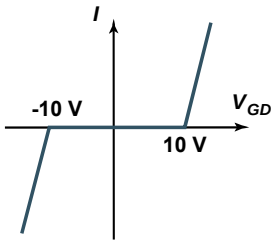
EPROM - ima staklo
OTPROM (One Time PROM) – nema staklo

Programiraju se u "istim" uređajima kao i PLD.
Brišu sa UV svetlošću.

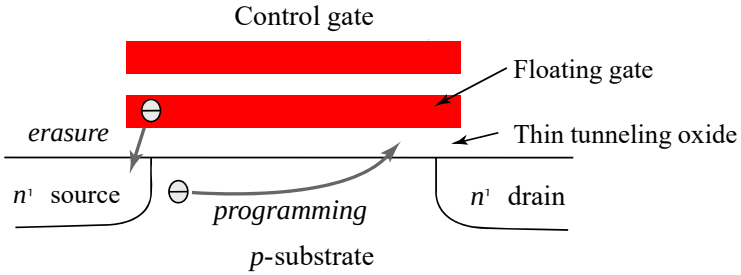
Digitalna elektronika
Programabilne logičke komponente – EEPROM

Elektroni na izolovanom gejtu.

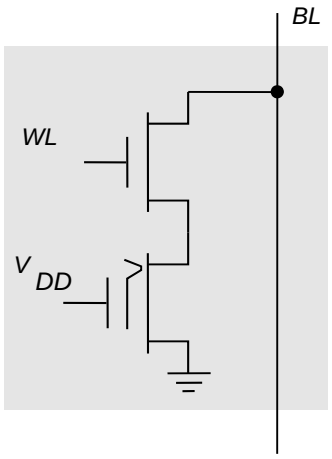
Kako su došli tako mogu i da odu

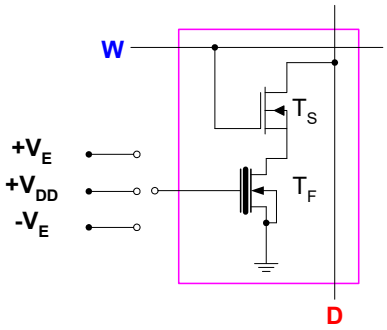


Fowler-Nordheim *I-V* characteristic



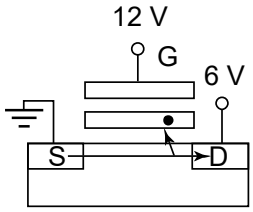
Digitalna elektronika
Programabilne logičke komponente – EEPROM

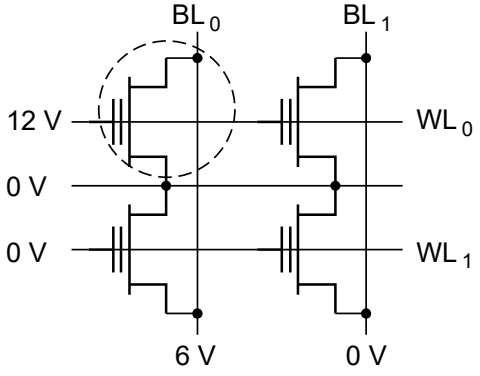




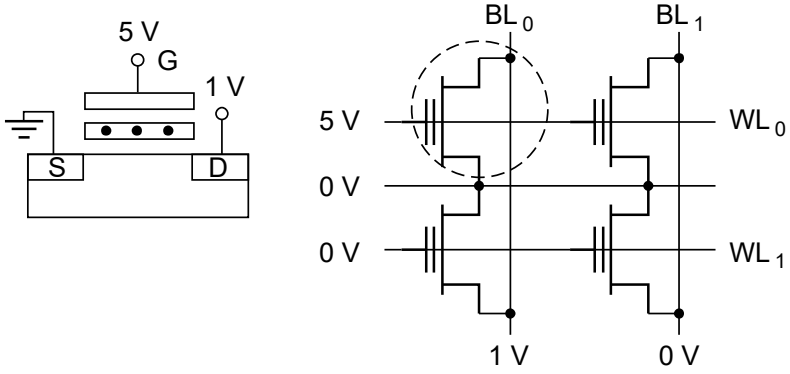
Kontrolu praga je teško ostvariti
“Neprogramiran” tranzistor?
Ako ga suviše izbrišemo.
⇨ **2 tranzistora**

Digitalna elektronika
Programabilne logičke komponente – Flash EPROM - UPIS

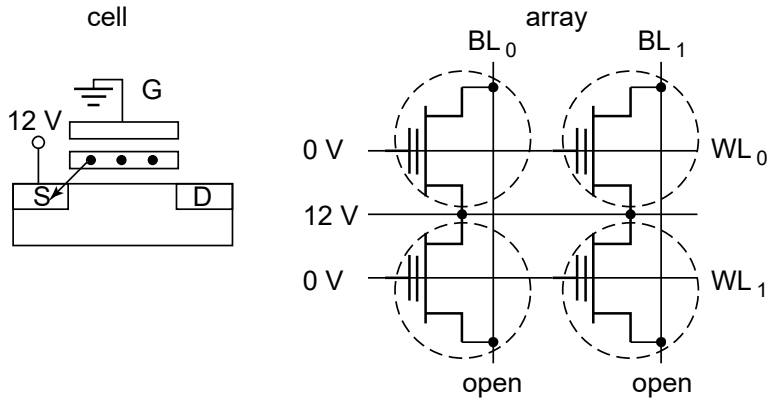




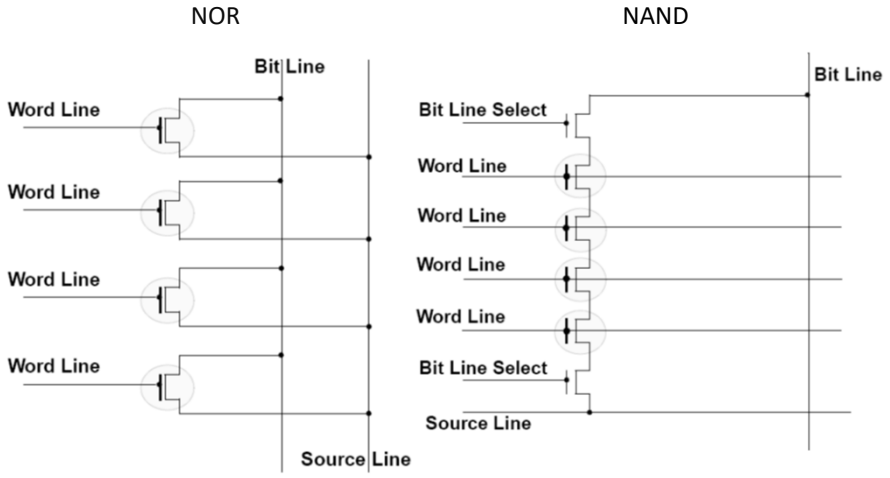
Digitalna elektronika
Programabilne logičke komponente – Flash EPROM - ČITANJE



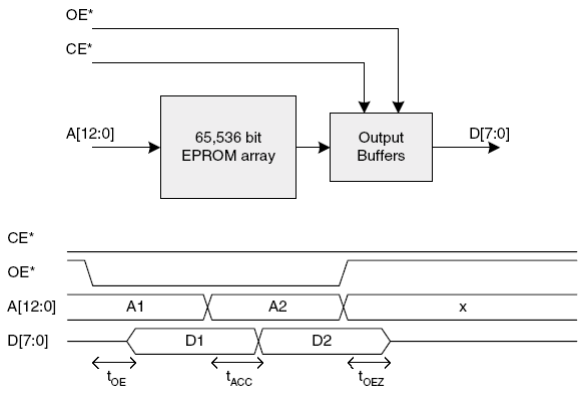
Digitalna elektronika
Programabilne logičke komponente – Flash EPROM - BRISANJE



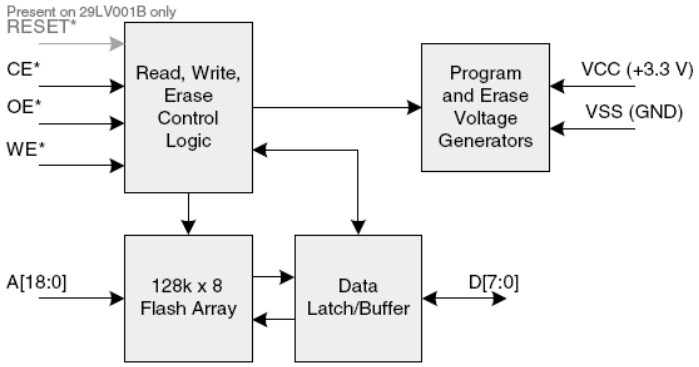
Digitalna elektronika
Programabilne logičke komponente – Flash EPROM



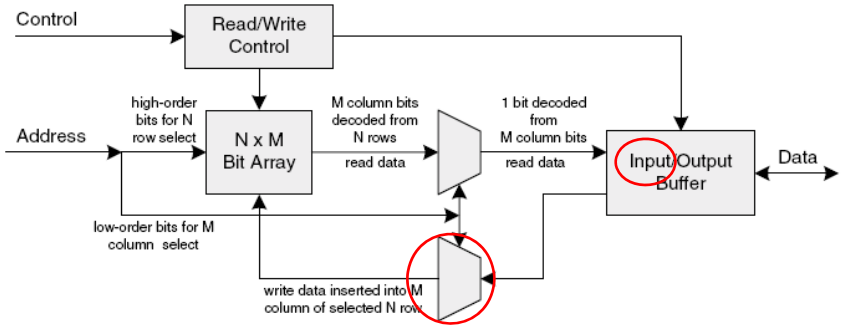
Digitalna elektronika
Programabilne logičke komponente – Memorije ROM



Digitalna elektronika
Programabilne logičke komponente – Memorije EEPROM FLASH



Digitalna elektronika
Programabilne logičke komponente – Memorije

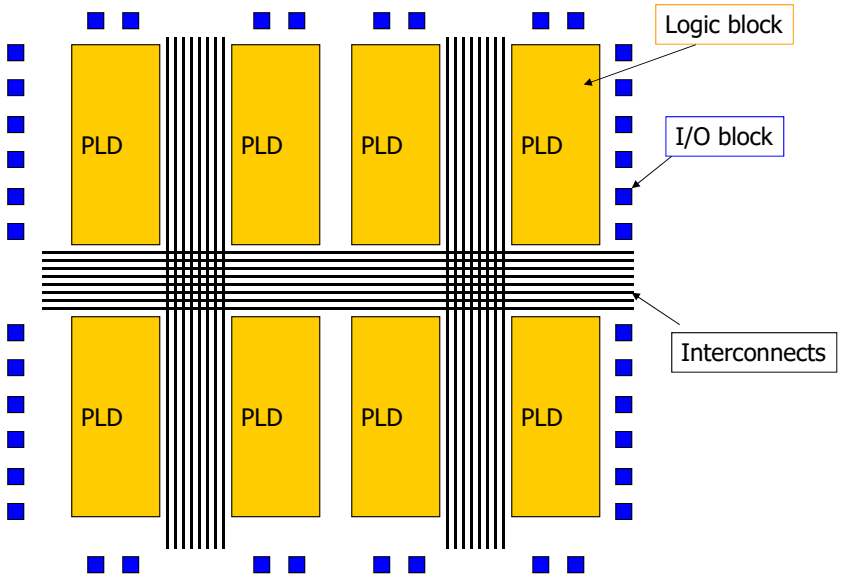


Adresa

Podatak

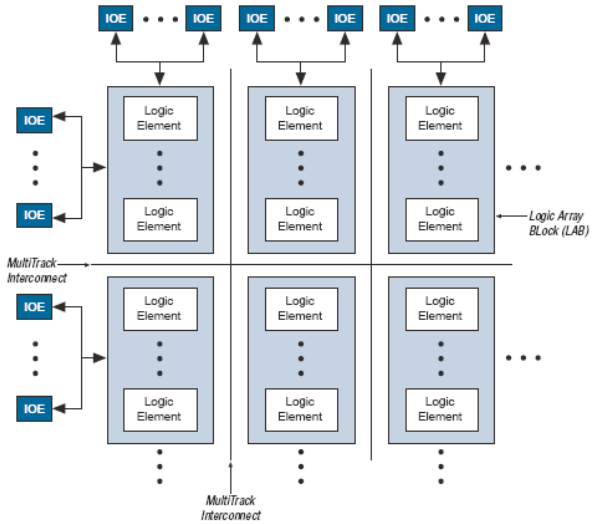
Kontrolni signali

Digitalna elektronika
Programabilne logičke komponente – CPLD

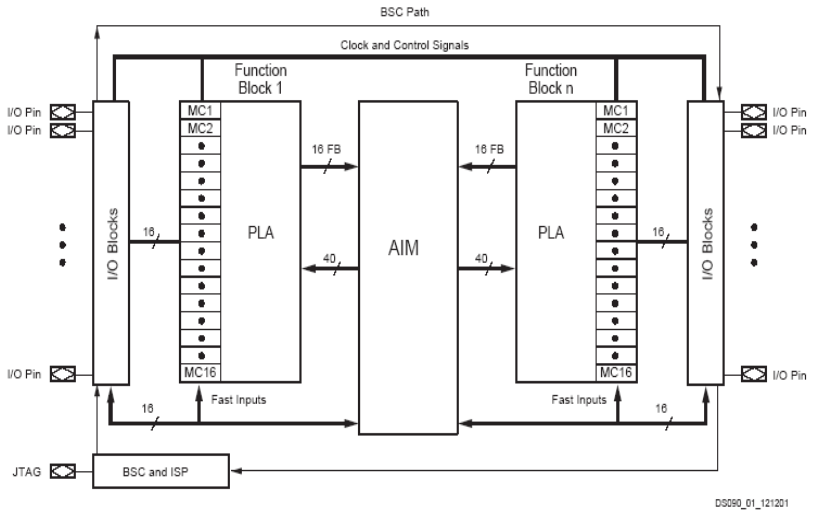


Digitalna elektronika
Programabilne logičke komponente – CPLD

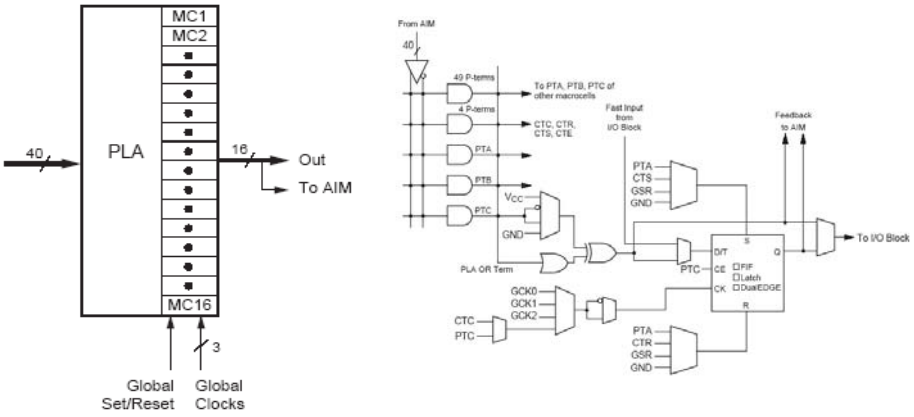
Figure 2–1. MAX II Device Block Diagram



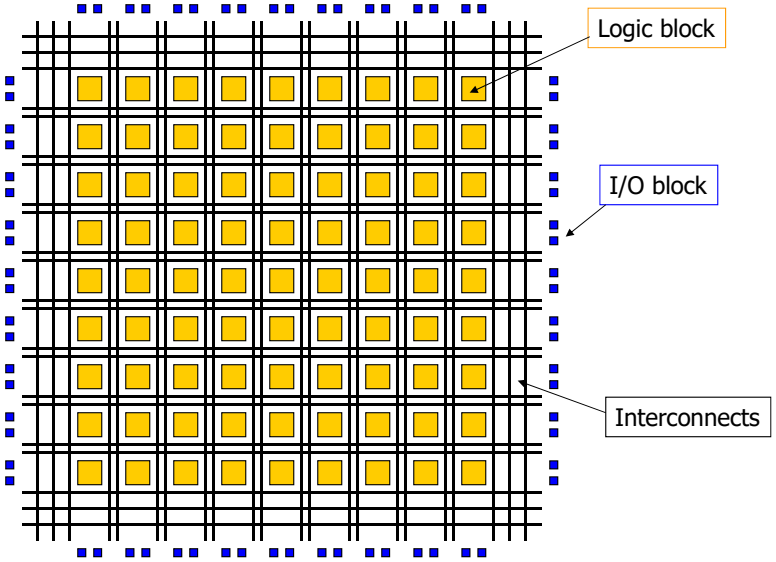
Digitalna elektronika
Programabilne logičke komponente – CPLD



Digitalna elektronika
Programabilne logičke komponente – CPLD

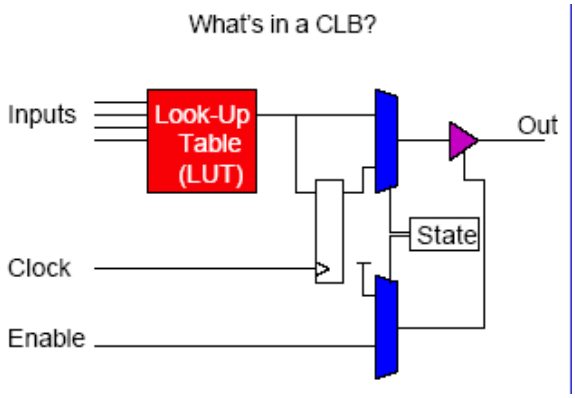


Digitalna elektronika
Programabilne logičke komponente – FPGA



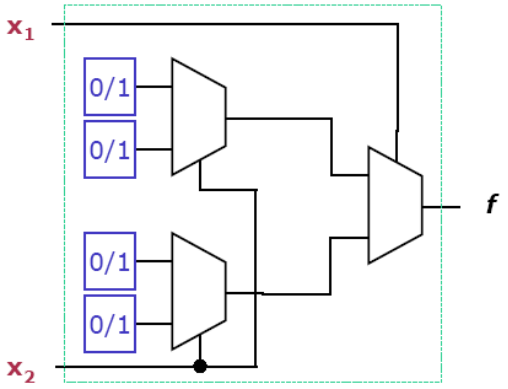
Digitalna elektronika
Programabilne logičke komponente – FPGA

CLB Configurable logic block

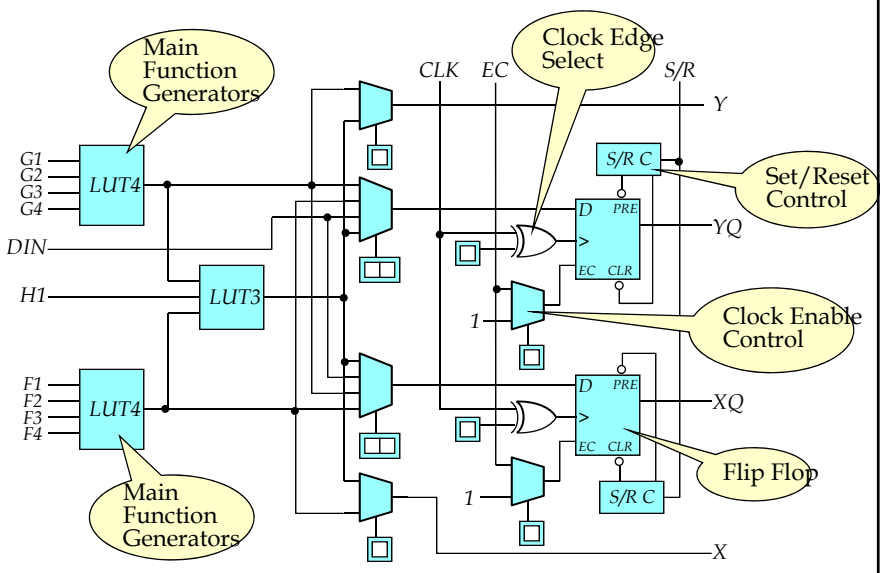


Digitalna elektronika
Programabilne logičke komponente – FPGA

LUT – Look Up Table

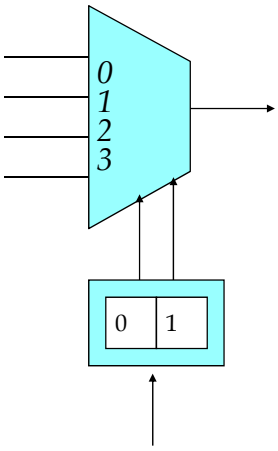


Digitalna elektronika
Programabilne logičke komponente – FPGA

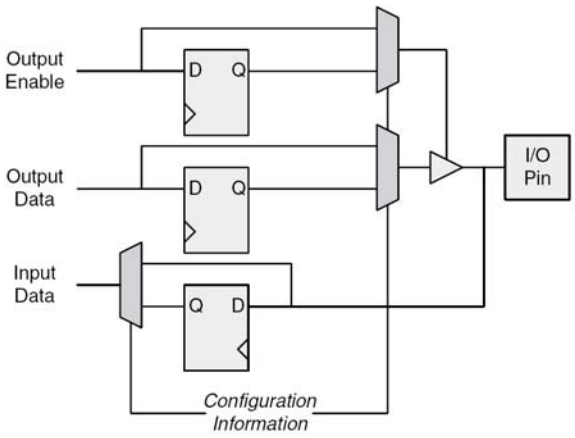


Digitalna elektronika
Programabilne logičke komponente – FPGA

Rutiranje multipleksorom – često unutar blokova

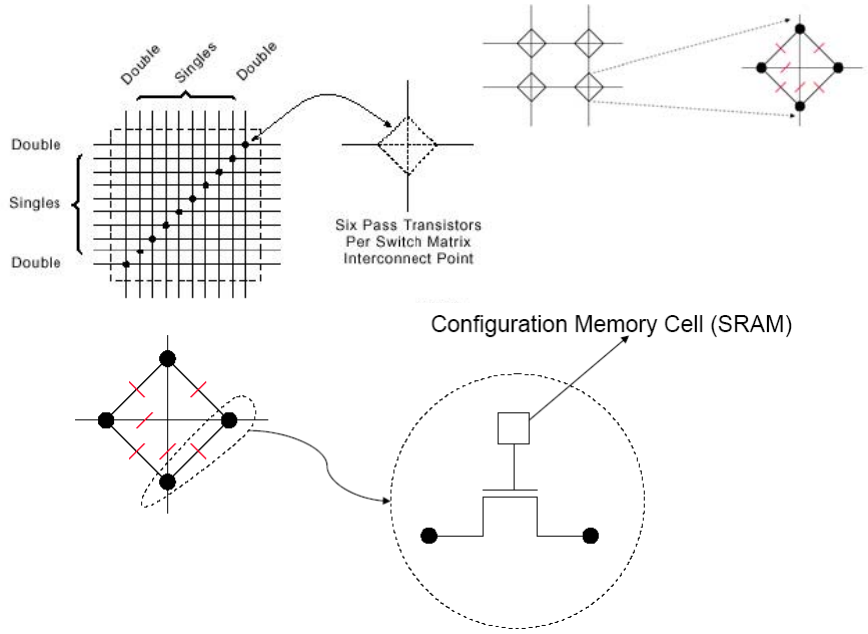


Digitalna elektronika
Programabilne logičke komponente – FPGA

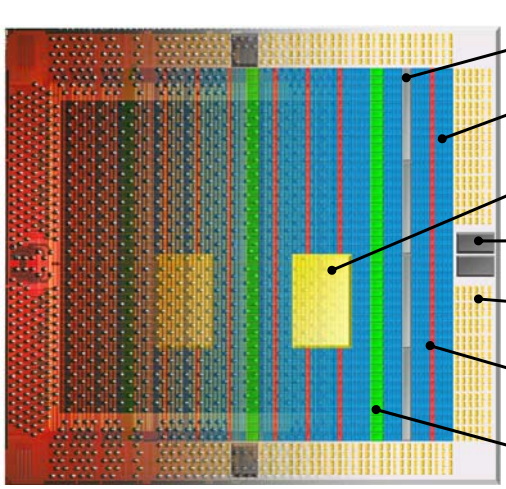


IOB Input Output Block

Digitalna elektronika
Programabilne logičke komponente – FPGA Rutiranje između blokova



Digitalna elektronika
Programabilne logičke komponente – FPGA



Broj pinova = ?
BGA

Digitalna elektronika
Programabilne logičke komponente – Programiranje CPLD FPGA

Floating gate transistor

SRAM-controlled switch — Control Pass transistors

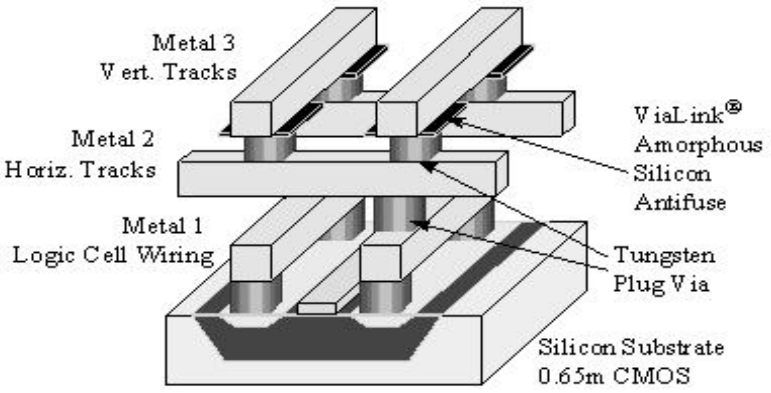
Multiplexers (to determine how to route inputs)

Antifuse Similar to fuse Originally an Open-Circuit

One-Time Programmable (OTP)

Digitalna elektronika
Programabilne logičke komponente – Programiranje CPLD FPGA

ANTIFUSE



Digitalna elektronika
Programabilne logičke komponente – Programiranje CPLD FPGA

"Isprogramirana" konfiguracija?

U lokacijama tipa statičkog RAM-a

Prednost - lako menjanje konfiguracije

Mana - nestaje kada se isključi napajanje

Proces "punjenja" konfiguracije obično iz PROM-a po uspostavljanju napajanja