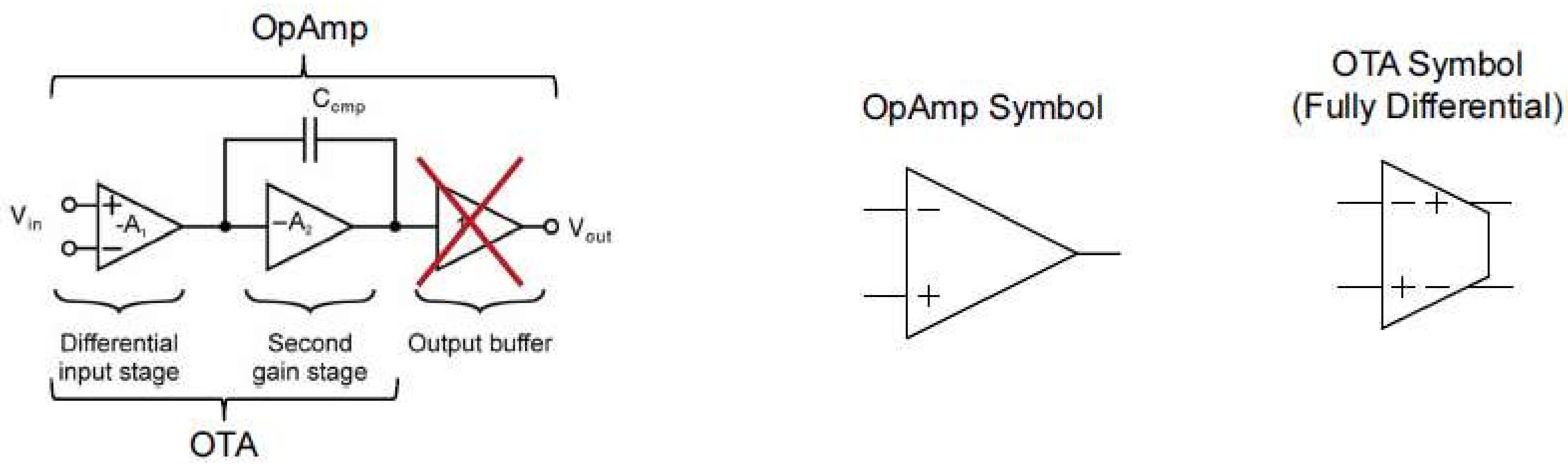
OTA-1

❖ OVA-Operational Voltage Amplifier

- Ideally a voltage-controlled voltage source
- Typically contains an output stage that can drive “arbitrary” loads, including small resistances
- Predominantly used for board-level circuitry

❖ OTA-Operational Transconductance Amplifier

- Ideally a voltage controlled current source
- Typically restricted to capacitive (or moderate resistive) loads
- Primarily used in integrated circuits



- The op-amp (OVA and OTA) is a fundamental building block in Mixed Signal design.
- Employed profusely in data converters, filters, sensors, drivers etc.
- Continued scaling in CMOS technology has been challenging the established paradigms for op-amp design.

•With downscaling in channel length (L)

✓Transition frequency increases (more speed)

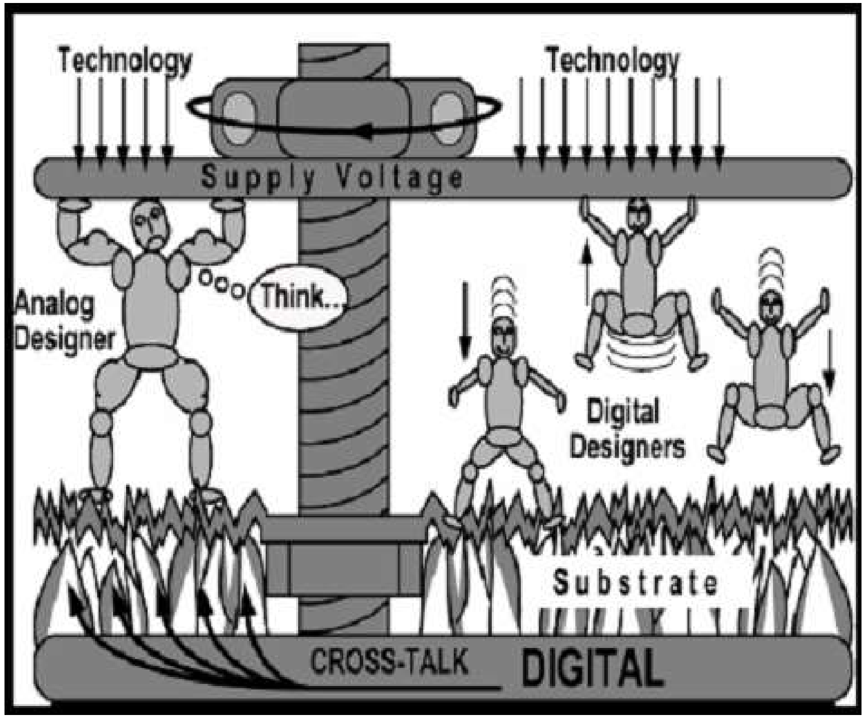
✓Open-loop gain reduces (lower intrinsic gain)

✓Supply voltage is scaled down (lower headroom)

✓VDD is scaling down but V_{TH} is almost constant (Design headroom is shrinking faster)

✓Random offsets due to device mismatches

$$\sigma_{\Delta V_{TH}} \propto \frac{1}{\sqrt{WL}}$$



•Integration of Analog into Nano-CMOS?

✓Design low-VDD op-amps.

✓Replace vertical stacking (cascoding) by horizontal cascading of gain stages

✓Explore more effective op-amp compensation techniques.

✓Offset tolerant designs.

✓Also minimize power and layout area to keep up with the digital trend.

✓Better power supply noise rejection (PSRR)

•Even if we employ wide-swing biasing for low-voltage designs, three- or higher stage opamps will be indispensable in realizing large open-loop DC gain.

The op amp (operational amplifier) is a high gain, dc coupled amplifier designed to be used with negative feedback to precisely define a closed loop transfer function.

The basic requirements for an op amp:

- Sufficiently large gain (the accuracy of the signal processing determines this)
- Differential inputs
- Frequency characteristics that permit stable operation when negative feedback is applied

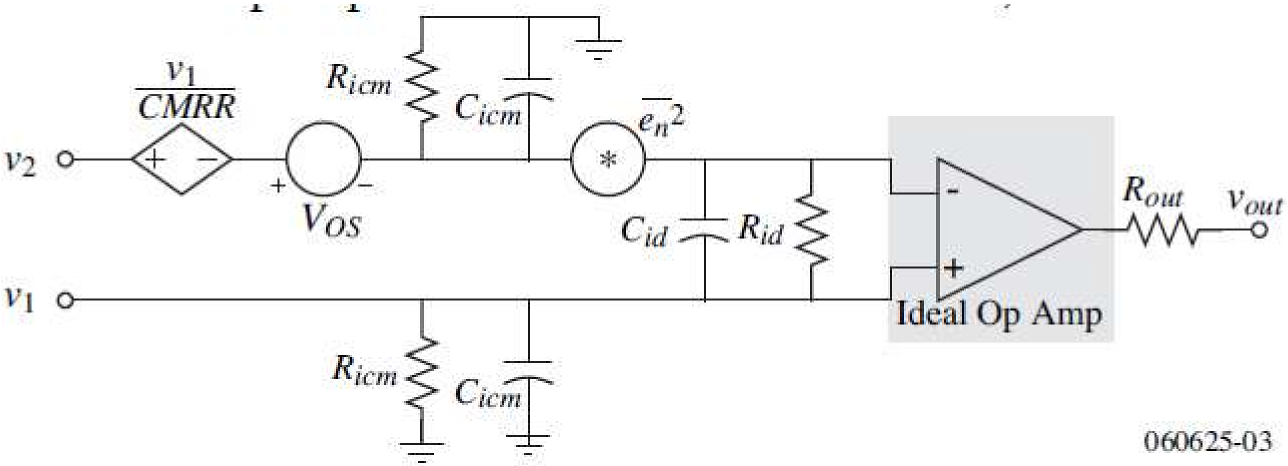
Other requirements:

- High input impedance
- Low output impedance
- High speed/frequency

❖OP AMP CHARACTERIZATION

•Linear and Static Characterization of the CMOS Op Amp

A model for a nonideal op amp that includes some of the linear, static nonidealities:



where
R_{id} = *differential input resistance*
C_{id} = *differential input capacitance*
R_{icm} = *common mode input resistance*
R_{icm} = *common mode input capacitance*
V_{OS} = *input-offset voltage*
CMRR = common-mode rejection ratio (when v_1=v_2 an output results)
e_n^2 = *voltage-noise spectral density (mean-square volts/Hertz)*

▪ Linear and Dynamic Characteristics of the Op Amp

Differential and common-mode frequency response:

$$V_{out}(s) = A_v(s)\left[V_1(s) - V_2(s)\right] \pm A_c(s)\frac{V_1(s)+V_2(s)}{2}$$

Differential-frequency response:

$$A_v(s) = \frac{A_{v0}}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)\left(1-\frac{s}{p_3}\right)\cdots}$$

$$p_i = -\omega_i$$

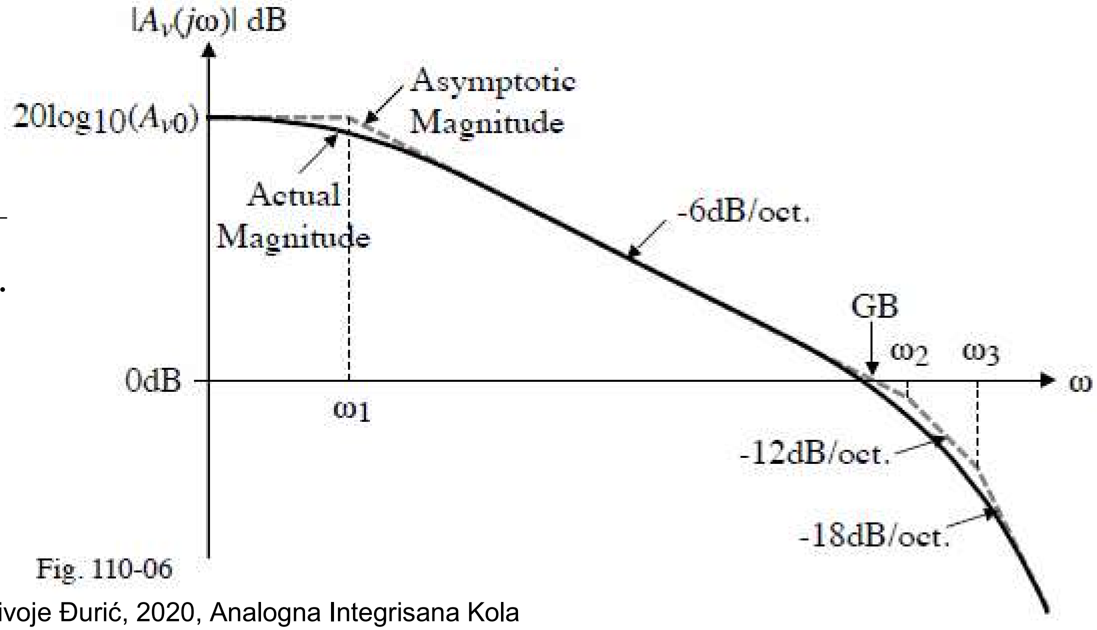


Fig. 110-06

▪Other Characteristics of the Op Amp

•Power supply rejection ratio (*PSRR):*

$$PSRR = \frac{V_{out}(s)/V_{in}(s)\big|_{V_{dd}(s)=0}}{V_{out}(s)/V_{dd}(s)\big|_{V_{in}(s)=0}}$$

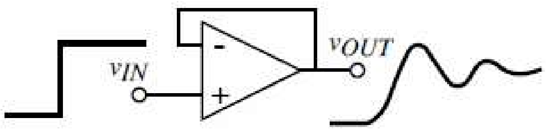
•Input common mode range (*ICMR):*

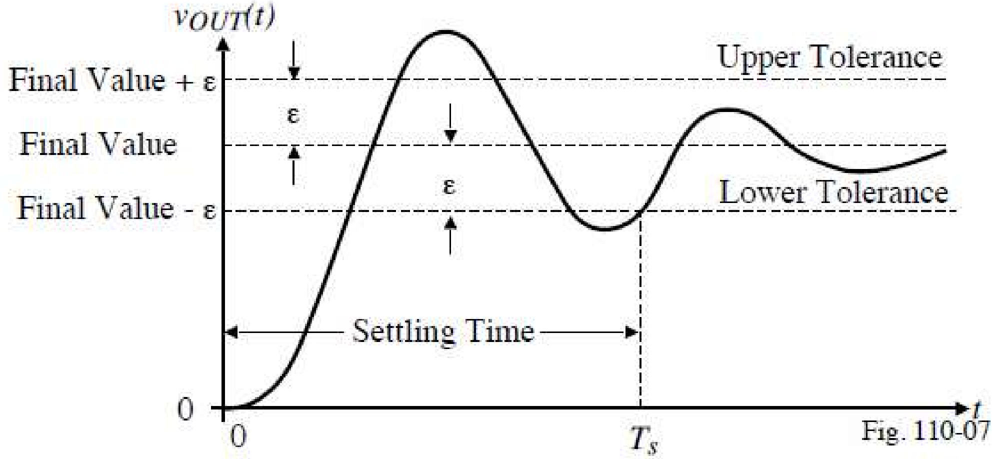
ICMR = the voltage range over which the input common-mode signal can vary without influence the differential performance

•Slew rate (*SR): maximum current available to charge and discharge a capacitance*

SR = output voltage rate limit of the op amp

•Settling time (*Ts): the time needed for the output of the output of the op amp to reach a final value value when excited by a small signal (SR is a large-signal phenomenon). Small-signal settling time can be completely determined from the location of the poles and zeros in the small-signal equivalent circuit.*

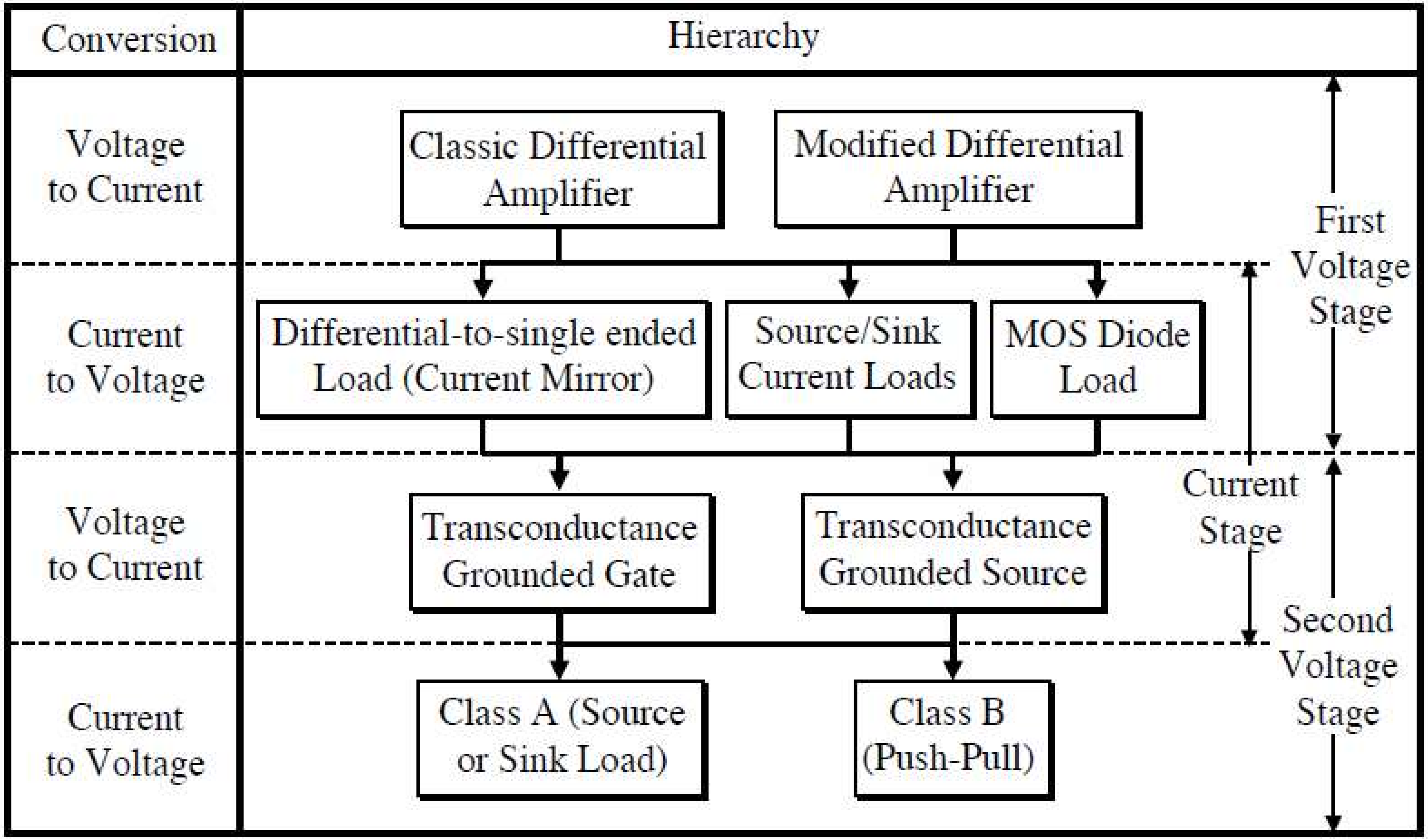




❖OP AMP CATEGORIZATION

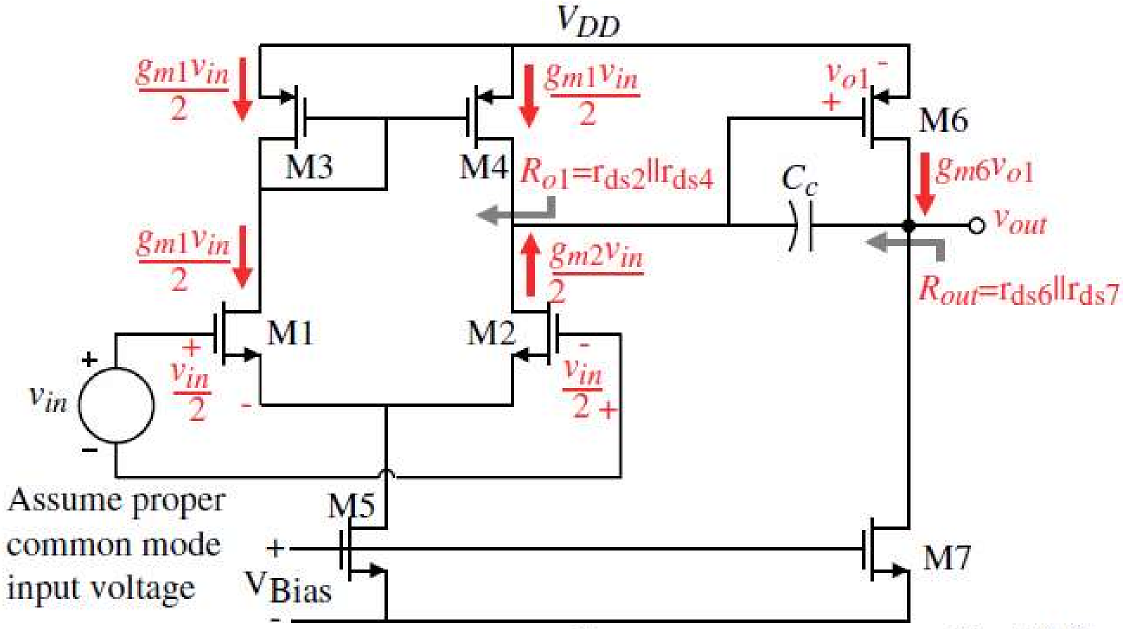
Amplifiers generaly consist of a cascade of V-I (transconductance stage) or I-V (load stage)

•Classification of CMOS Op Amps



➢Output configuration
– Single ended
– Differential
  • Predominantly used for integrated high-performance or high precision amplifiers
  • Requires common mode feedback circuit
– Class-A
  • Output cannot source/sink currents larger than quiescent point bias current
– Class-AB
  • Output can provide large drive currents “on demand”
– Dynamic, comparator-based
  • Still a research topic

✓Two-stage single ended Miller CMOS OTA



$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right)\left(\frac{-g_{m6}}{g_{ds6}+g_{ds7}}\right)$$

Fig. 170-01

•Classical two-stage CMOS op amp broken into voltage-to-current and current-to-voltage stages:

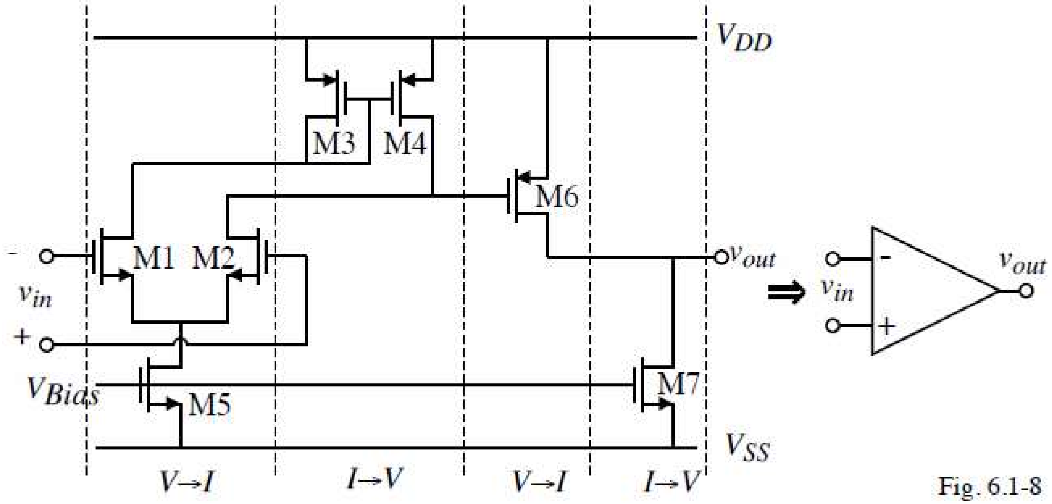
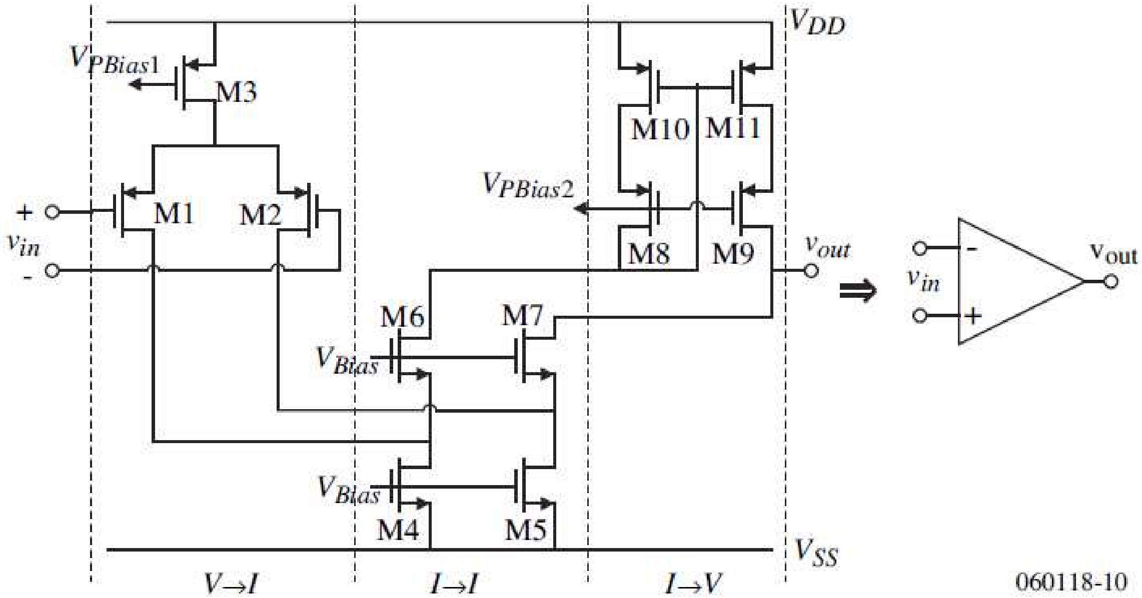


Fig. 6.1-8

•Folded cascode CMOS op amp broken into stages:



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✓Two-stage Single ended Folded-Cascode CMOS OTA

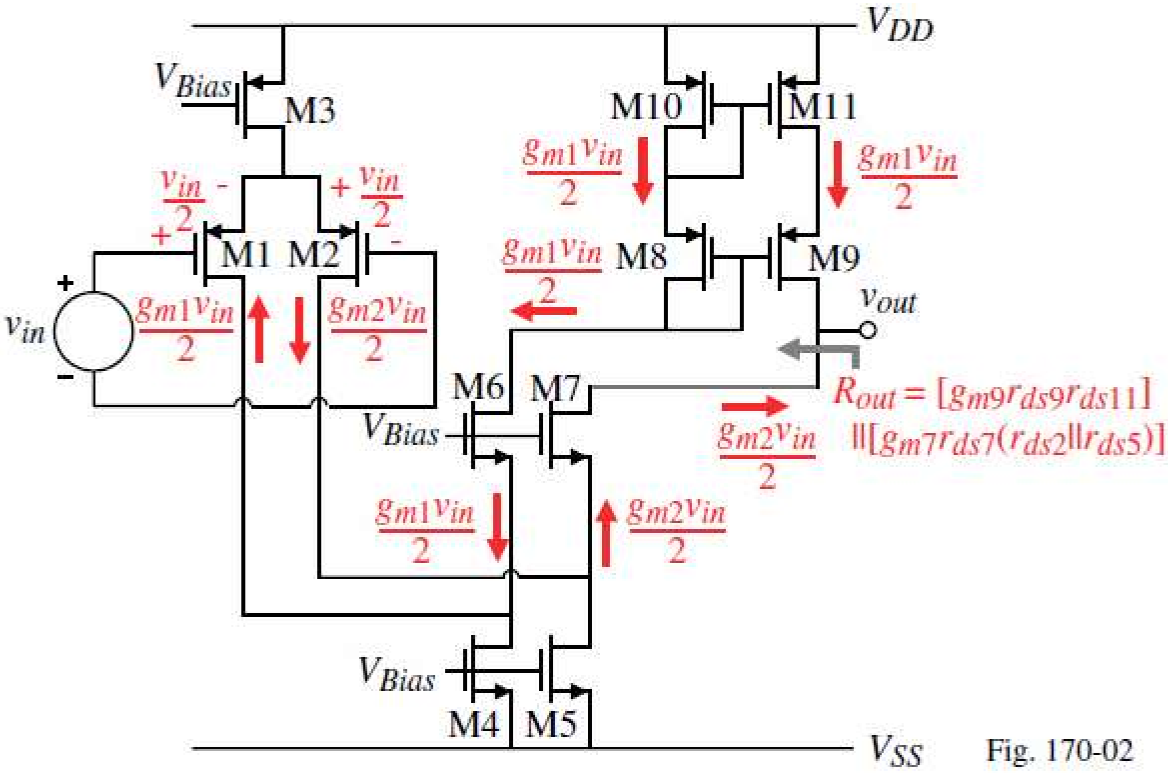


Fig. 170-02

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2}+\frac{g_{m2}}{2}\right)R_{out} = g_{m1}\{(g_{m9}r_{ds9}r_{ds11})||[g_{m7}r_{ds7}(r_{ds2}||r_{ds5})]\}$$

➢COMPENSATION OF OP AMPS

•Objective of compensation is to achieve stable operation when negative feedback is applied around the op amp.

$$L(s) = -A(s)F(s)$$

$$CLG(s) = \frac{A(s)}{1 + A(s)F(s)}$$

$$\left|A(j\omega_{0dB})F(j\omega_{0dB})\right| = \left|L(j\omega_{0dB})\right| = 1 \Rightarrow \omega_0$$

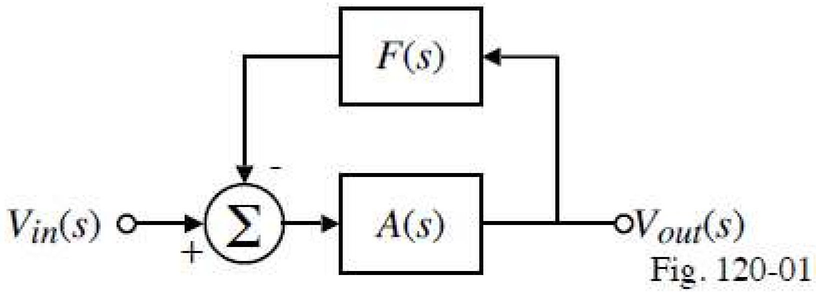
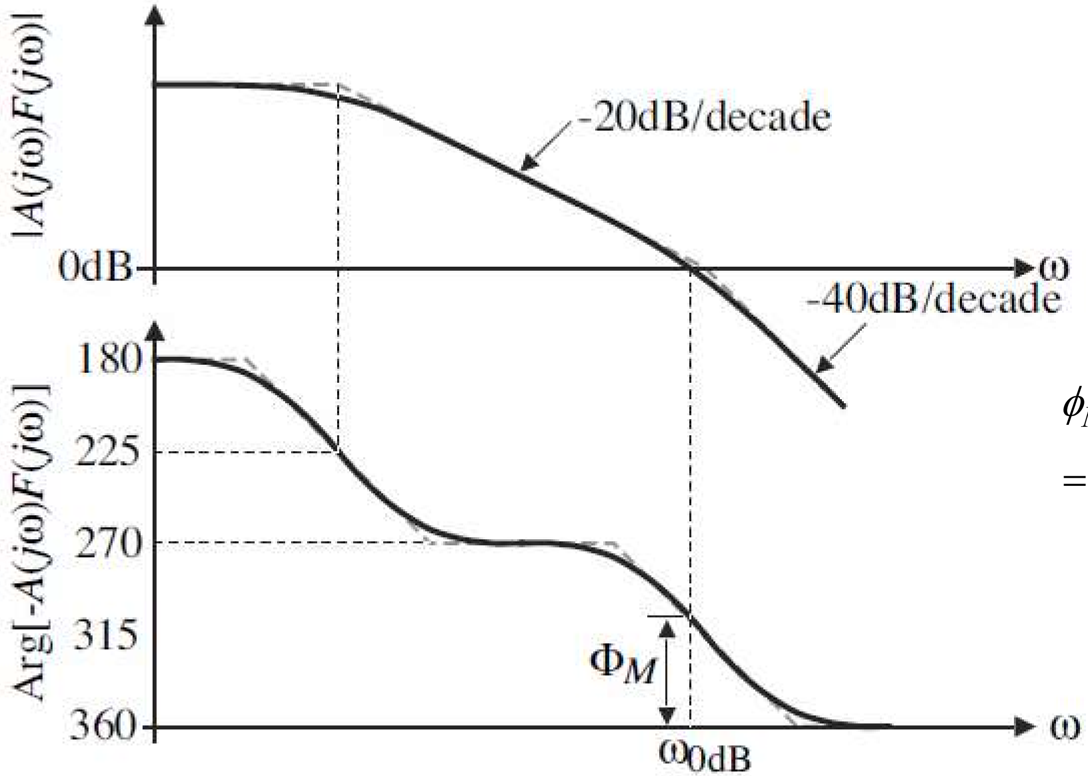


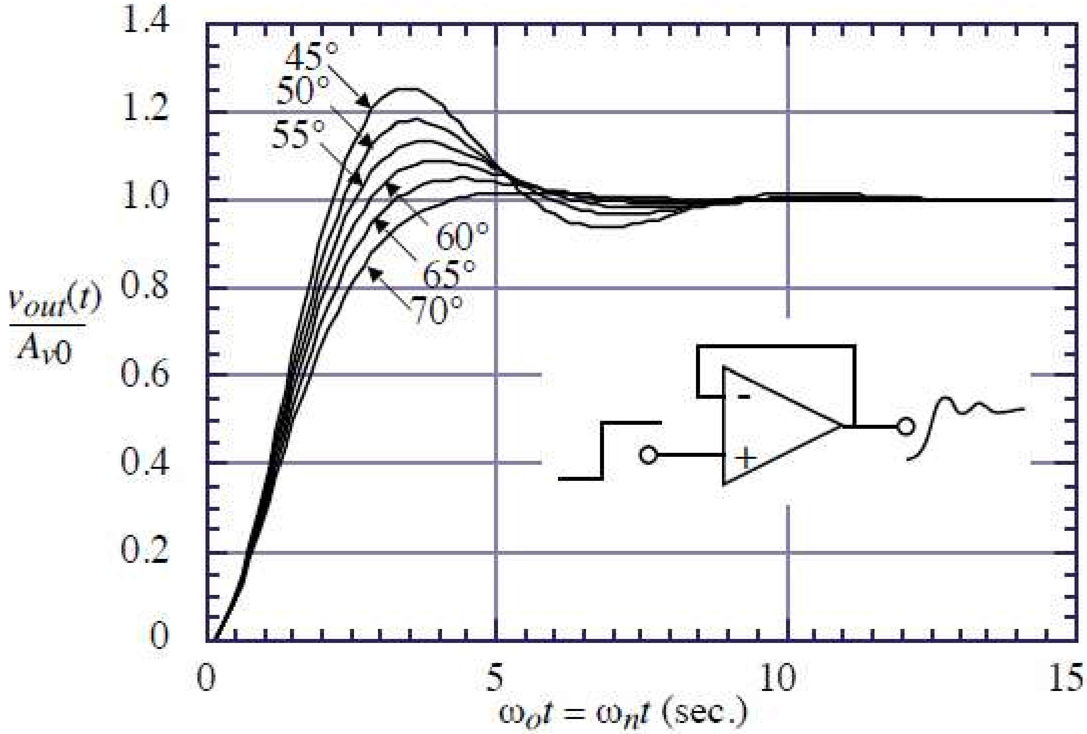
Fig. 120-01



$$\phi_M = 2\pi - \arg\left[-A(j\omega_{0dB})F(j\omega_{0dB})\right]$$
$$= 2\pi - \arg\left[L(j\omega_{0dB})\right]$$

Why Do We Want Good Stability?

•Consider the step response of second-order system which closely models the closed-loop gain of the op amp connected in unity gain.



•A "good" step response is one that quickly reaches its final value.

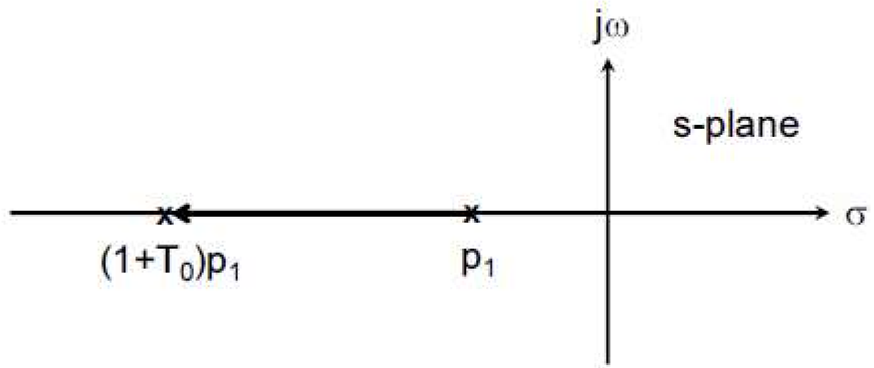
•Therefore, we see that phase margin should be at least 45° and preferably 60° or larger.

(A rule of thumb for satisfactory stability is that there should be less than three rings.)

•Note that good stability is not necessarily the quickest rise time.

Root Locus

- 1st order feedback system



•A so-called “root locus” plot shows the movement of the poles in the s plane as we vary the low-frequency loop gain T0

- 2nd order feedback system

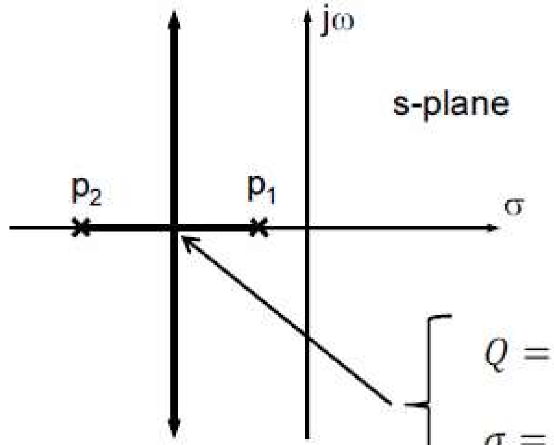
$$\mathrm{H}(s) = \frac{1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}$$

$$for\ Q > 0.5 \qquad s_{1,2} = -\frac{\omega_0}{2Q}\left(1 \pm j\sqrt{4Q^2 - 1}\right)$$

$$for\ Q \leq 0.5 \qquad s_{1,2} = -\frac{\omega_0}{2Q}\left(1 \pm \sqrt{1 - 4Q^2}\right)$$

$$\omega_0 = \sqrt{(1 + T_0)\omega_{p1}\omega_{p2}}$$

$$Q = \frac{\sqrt{(1 + T_0)\omega_{p1}\omega_{p2}}}{\omega_{p1} + \omega_{p2}}$$

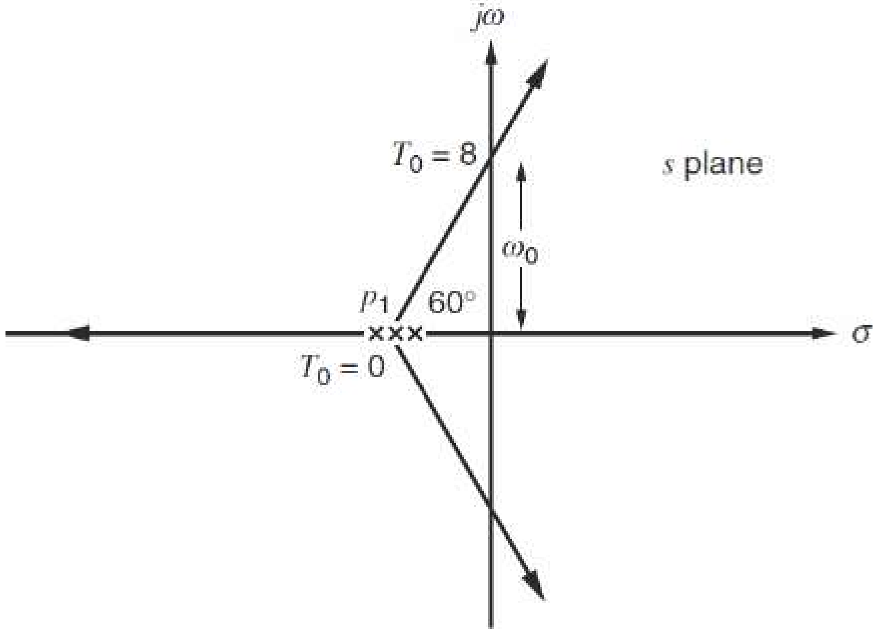


$$\left\{ \begin{array}{l} Q = 0.5 \\ \sigma = -\frac{\omega_0}{2Q} = -\frac{\omega_{p1} + \omega_{p2}}{2} \end{array} \right.$$

➢3rd order feedback system

•Consider a feedback network consisting of a forward amplifier with three identical poles, and a feedback network with a constant transfer function f

$$a(s)=\frac{a_0}{\left(1-\frac{s}{p_1}\right)^3} \qquad T_0=a_0 f$$



$$A(s)=\frac{a(s)}{1+a(s)f}=\frac{\dfrac{a_0}{\left(1-\frac{s}{p_1}\right)^3}}{1+a\dfrac{a_0}{\left(1-\frac{s}{p_1}\right)^3}f}=\frac{a_0}{\left(1-\frac{s}{p_1}\right)^3+T_0}$$

The poles of A(s) are therefore the solution to

$$\left(1-\frac{s}{p_1}\right)^3+T_0=0 \qquad \left(1-\frac{s}{p_1}\right)^3=-T_0$$

$$\left(1-\frac{s}{p_1}\right)=\sqrt[3]{-T_0}=-\sqrt[3]{T_0} \quad \text{or} \quad \left(1-\frac{s}{p_1}\right)=\sqrt[3]{T_0}e^{j60^\circ} \quad \text{or} \quad \left(1-\frac{s}{p_1}\right)=\sqrt[3]{T_0}e^{-j60^\circ}$$

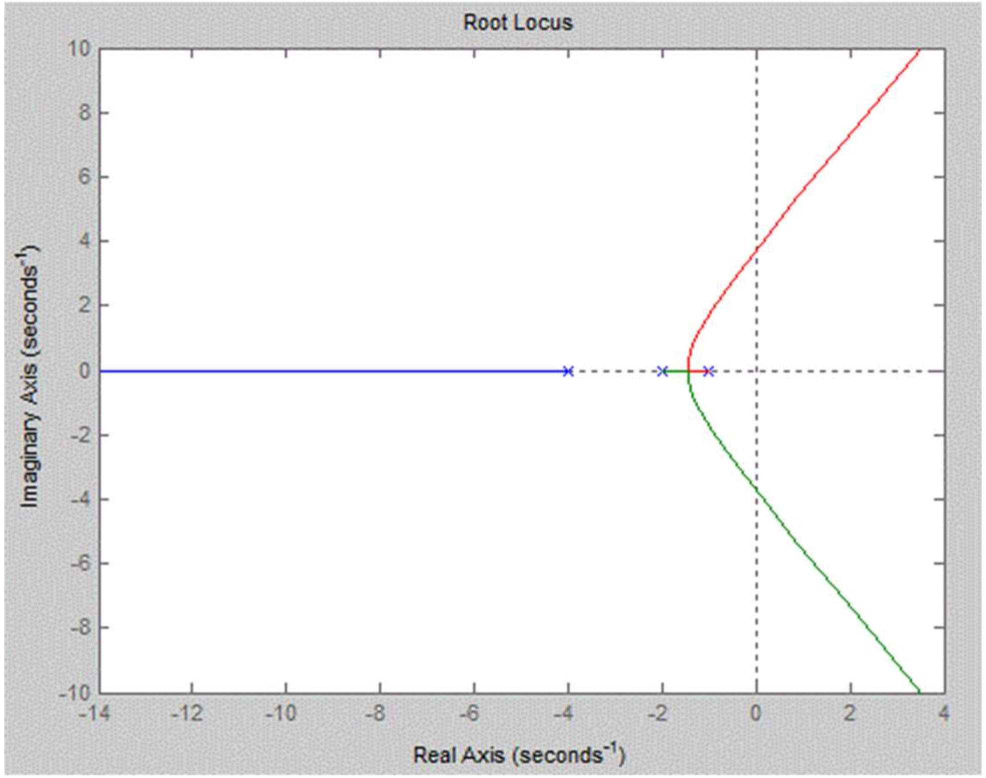
$$s_1=p_1\left(1+\sqrt[3]{T_0}\right) \qquad s_2=p_1\left(1-\sqrt[3]{T_0}e^{j60^\circ}\right) \qquad s_3=p_1\left(1-\sqrt[3]{T_0}e^{-j60^\circ}\right)$$

$$0=1-\mathrm{Re}\left(\sqrt[3]{T_0}e^{j60^\circ}\right) \qquad 0=1-\sqrt[3]{T_0}\cos(60^\circ) \;\Rightarrow T_0=8$$

MATLAB:

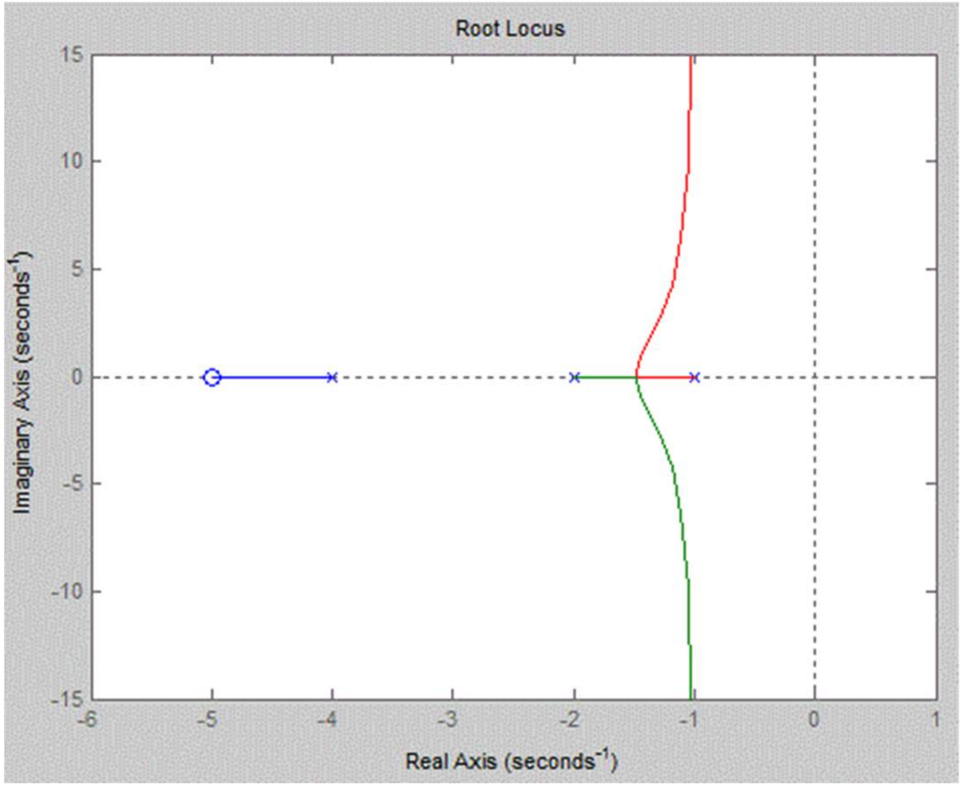
The transfer function with three poles

```
s = tf('s');
p1=-1; p2=-2; p3=-4;
T = 1 / [(1-s/p1)*(1-s/p2)*(1-s/p3)];
rlocus(T)
```



Adding a Zero:

```
s = tf('s');
z=-5; p1=-1; p2=-2; p3=-4;
T = (1-s/z) / [(1-s/p1)*(1-s/p2)*(1-s/p3)];
rlocus(T)
```



▪Benchmarking

•In order to compare the merit of various compensation techniques, it makes sense to inspect the loop's unity gain frequency before and after the compensation is applied

•Rationale: The maximum bandwidth we can possibly expect from a feedback amplifier is the unity gain frequency of the loop

✓Regardless of the order of the feedback system, the closed-loop response departs from 1/f as |T(s)| crosses unity

$$A(s) = \frac{a(s)}{1 + a(s)f(s)} \begin{cases} \cong \dfrac{1}{f(s)} & for\ |T(s)| \gg 1 \\ \cong a(s) & for\ |T(s)| \ll 1 \end{cases}$$

✓Consider a loop transfer function with n "dominant" poles that occur before the unity crossover

$$T(s) = \frac{T_0}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) \dots \left(1 - \frac{s}{p_n}\right)} = \frac{\mathrm{T}_0}{1 + \dots + \frac{\mathrm{s}^{\mathrm{n}}}{\mathrm{p}_1 \mathrm{p}_2 \dots \mathrm{p}_{\mathrm{n}}}}$$

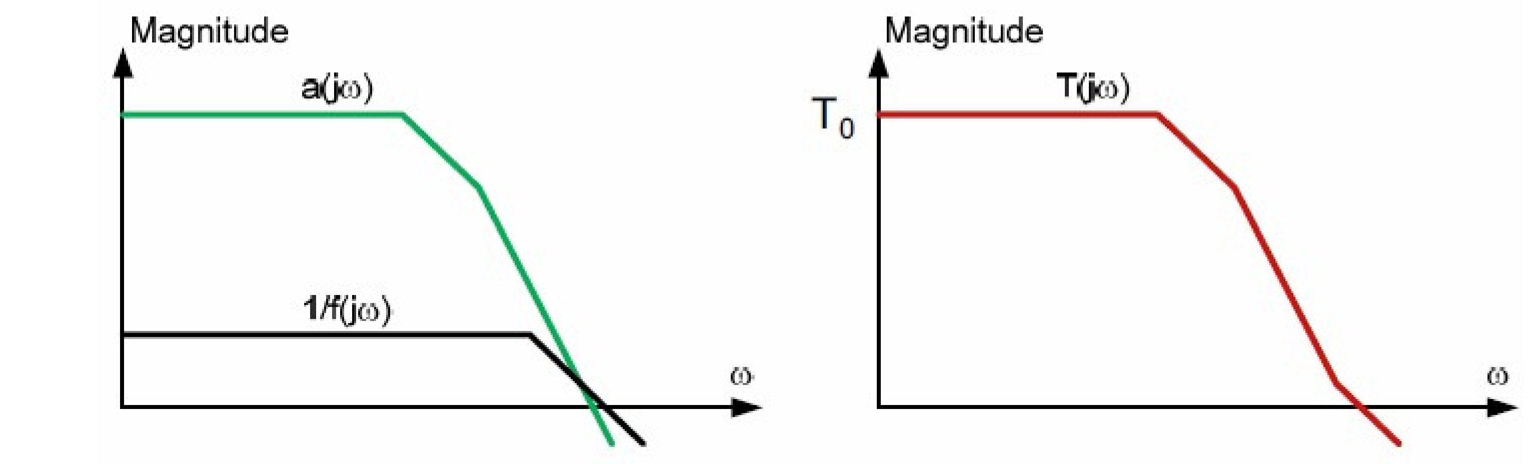
$$\omega_u \cong \sqrt[n]{T_0 |\mathrm{p}_1||\mathrm{p}_2| \dots |\mathrm{p}_{\mathrm{n}}|} = \sqrt[n]{LP}$$

✓The product of the low frequency loop gain and all dominant poles is called the loop gain pole product (LP product)

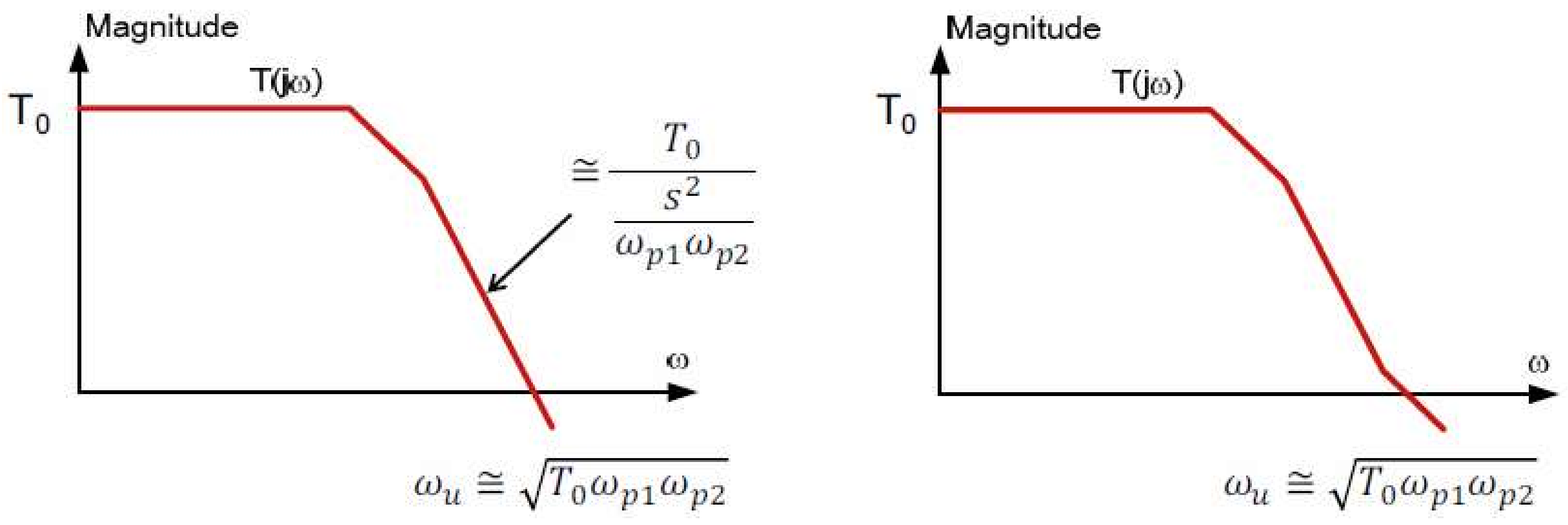
✓Note that in a first-order system, the LP product is simply the gain bandwidth product

▪Feedback Zero Compensation

✓Leave amplifier poles unchanged and introduce a zero in the feedback network

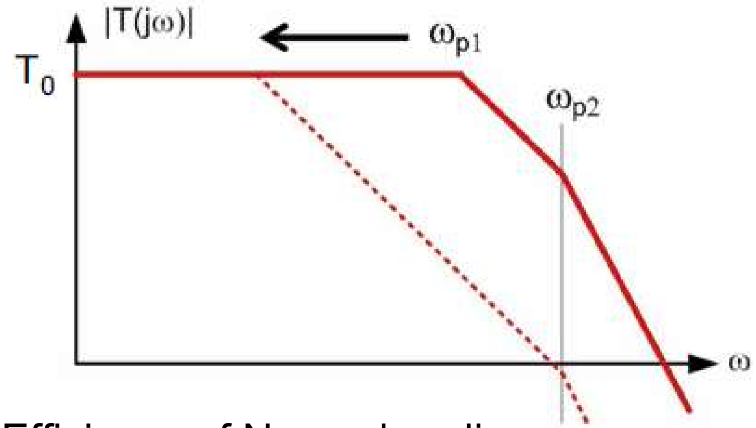


•Efficiency of Feedback Zero Compensation



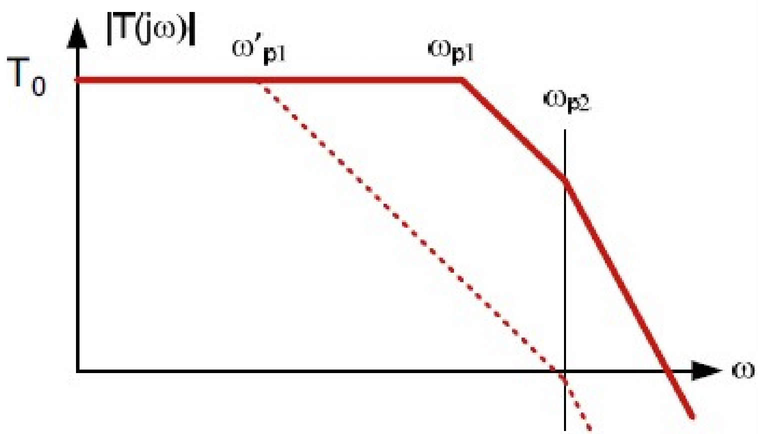
✓To first order, since we do not change the poles, the LP product and ω_u are (approximately) unchanged.
✓Feedback zero compensation is therefore bandwidth efficient, since we do not need to sacrifice bandwidth to stabilize the circuit.
✓To second order, the LP product will change slightly due to loading from the capacitance added in the feedback network

▪Narrowbanding Compensation



Idea: Make one of the loop poles dominant, leave other poles unchanged

•Efficiency of Narrowbanding



ω_{p1} that gives a maximally flat magnitude response for the closed-loop amplifier?

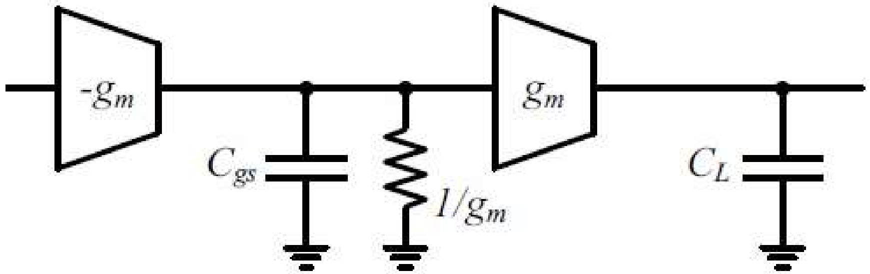
$$\omega_{p1} = \frac{1}{2}\frac{\omega_{p2}}{T_0}$$

$$\omega_u \cong \sqrt{T_0 \omega_{p1} \omega_{p2}}$$

$$\omega_u' \cong T_0 \omega_{p1} \cong \frac{1}{2}\omega_{p2}$$

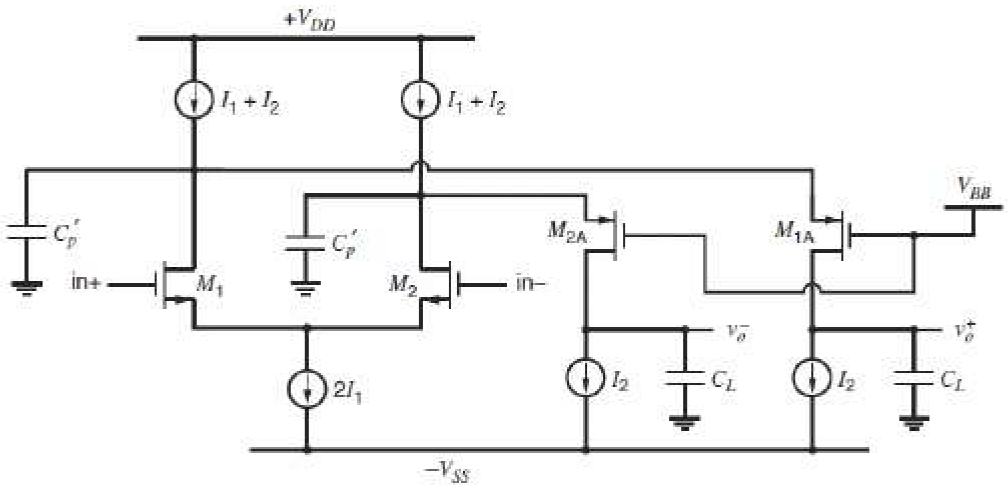
✓The crossover and bandwidth is limited to some fraction of ω_{p2}
✓ At first glance, this makes narrowbanding appear to be inefficient
✓However, provided that ω_{p2} is close to the transit frequency of the process technology, this compensation approach is acceptable and hard to surpass in terms of absolute achievable closed-loop speed

❖Example: Single Gain Stage with Current Buffer



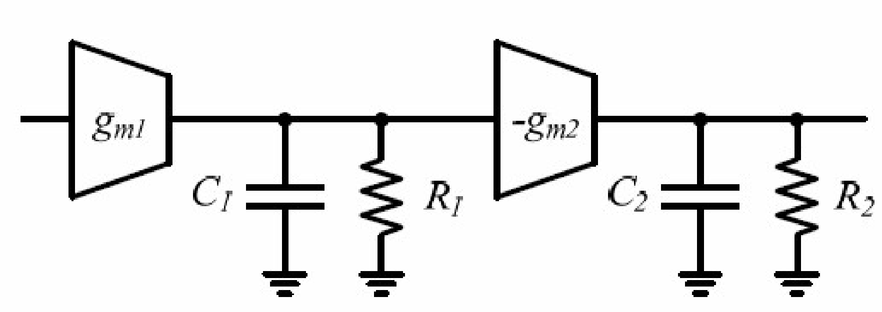
•Cgs introduces a non-dominant pole at high frequencies $\omega_{p2} = \omega_T$
•CL is adjusted until the circuit achieves the desired phase margin
•This type of narrowbanding is called “load compensation,” since stability is ensured by properly sizing the load capacitance CL

✓Example Realizations



▪Two-Stage OTA

•The two-stage amplifier shown below has two comparable poles, assuming that there is no additional significant pole from the feedback network



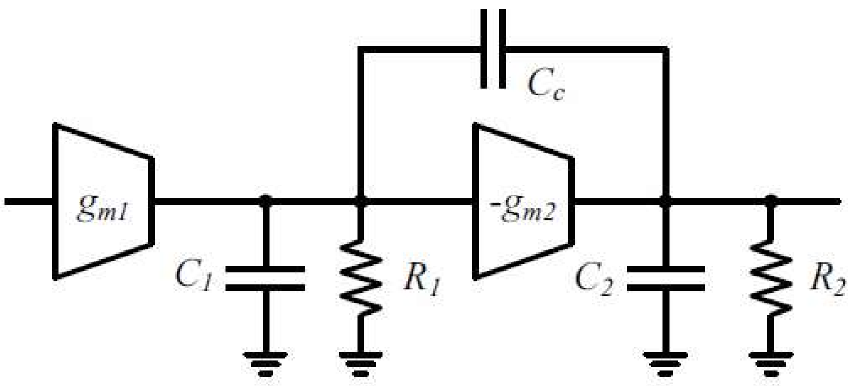
✓If the feedback network is resistive, we may be able to compensate the amplifier by introducing a feedback zero

✓What can we do if the feedback is capacitive?

✓Narrowbanding is not a good idea, since both poles are at low frequencies

➢**Miller Compensation**

✓Purposely connect a capacitor across the second transconductor!



•Two interesting things happen

✓Low frequency input capacitance of second stage becomes large – moves the first pole to a lower frequency

✓Qualitatively speaking, at high frequencies, Cc turns the second stage into a “diode connected device” – low impedance, i.e. large ω_{p2}

- Using the dominant pole approximation:

$$p_1 \cong -\frac{1}{R_1\left[C_1 + C_c(1+g_{m2}R_2)\right] + R_2(C_2 + C_c)} \qquad p_2 \cong -\frac{R_1\left[C_1 + C_c(1+g_mR_2)\right] + R_2(C_2 + C_c)}{R_1R_2(C_1C_2 + C_1C_c + C_2C_c)}$$

RHP zero: $z = +\frac{g_{m2}}{C_C}$

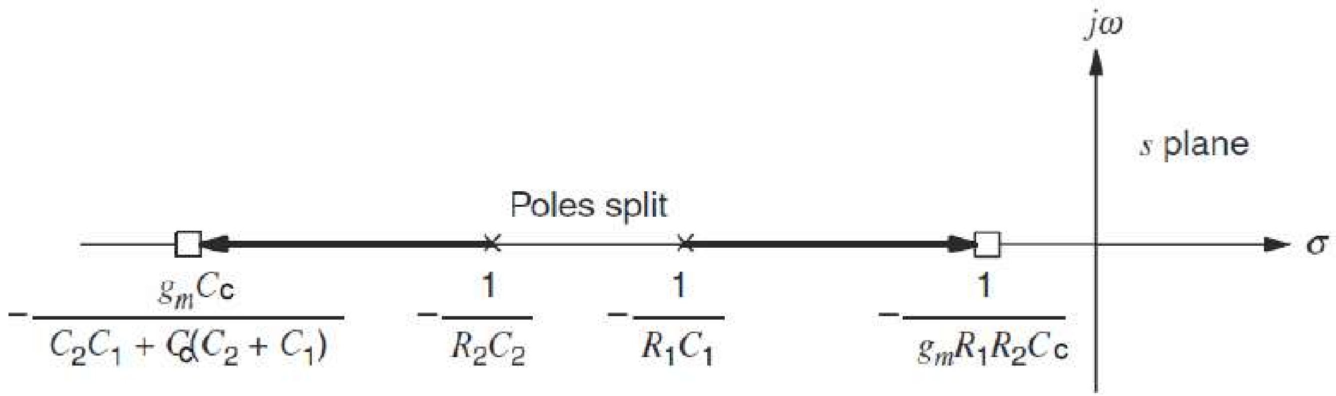
✓We can approximate further as shown below

$$\omega_{p1} \cong \frac{1}{g_{m2}R_2R_1C_C} \qquad a_0\omega_{p1} \cong \frac{g_{m1}R_1g_{m2}R_2}{g_{m2}R_2R_1C_C} = \boxed{\frac{g_{m1}}{C_C}}$$

GBW set by gm1 and Cc

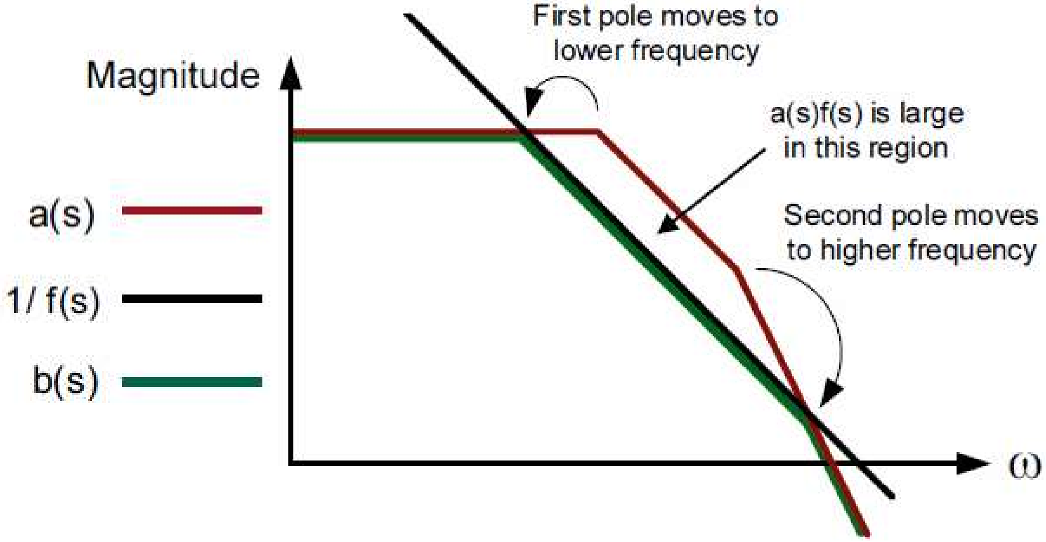
$$\omega_{p2} \cong \frac{g_{m2}C_c}{C_1C_2 + C_c(C_1 + C_2)} \qquad \frac{1}{\omega_{p2}} \cong \left(\frac{C_1}{g_{m2}} + \frac{C_2}{g_{m2}}\right)\left(1 + \frac{\frac{C_1C_2}{C_1 + C_2}}{C_c}\right)$$

✓"Pole Splitting": Increasing Cc reduces ω_{p1} , and increases ω_{p2}



✓A very nice “knob” for adjusting the phase margin of the circuit!

•Graphical View of Pole Splitting



$$b(s)=\frac{a(s)}{1+a(s)f(s)}\cong\begin{cases} a(s) & \text{when } |a(s)f(s)|<<1 \\ \dfrac{1}{f(s)} & \text{when } |a(s)f(s)|>>1 \end{cases}$$

➢Miller Compensation of the Two-Stage Op Amp

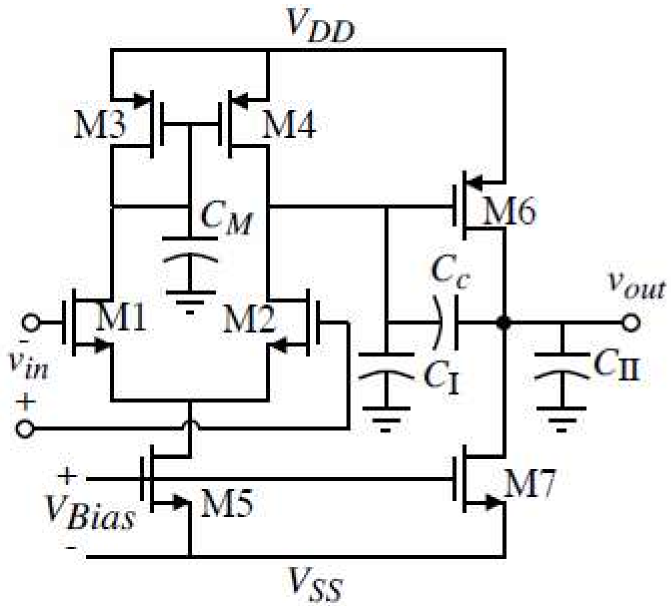
The various capacitors are:

C_c = accomplishes the Miller compensation

C_M = capacitance associated with the first-stage mirror (mirror pole)

C_I = output capacitance to ground of the first-stage

C_{II} = output capacitance to ground of the second-stage



➢Compensated Two-Stage, Small-Signal Frequency Response Model Simplified

Use the CMOS op amp to illustrate:

• Assume that:

$$C_C >> C_{gd6},\ g_{m3} >> g_{ds3} + g_{ds1},\ \frac{g_{m3}}{C_M} >> \omega_u = GB$$

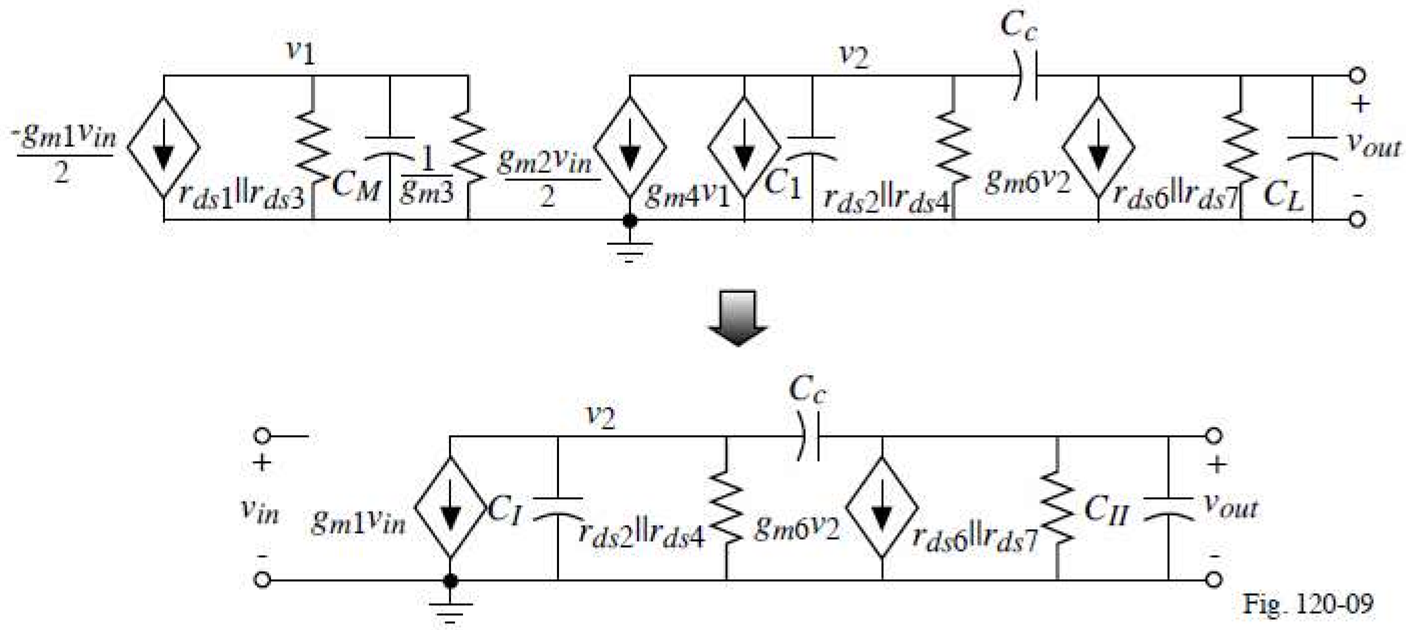


Fig. 120-09

$$g_{m1} = g_{mI},\ g_{m6} = g_{mII}$$

$$\frac{1}{g_{ds2} + g_{ds4}} = R_I,\ \frac{1}{g_{ds6} + g_{ds7}} = R_{II}$$

$$C_I = C_{db2} + C_{db4} + C_{gs6},\ C_{II} = C_L + C_{db6} + C_{db7} + C_{gd7}$$

Nodal Equations:

$$\left[G_I + s\left(C_I + C_c\right)\right]V_2 - sC_cV_{out} = -g_{mI}V_{in}$$

$$\left[g_{mII} - sC_c\right]V_2 + \left[G_{II} + s\left(C_{II} + C_c\right)\right]V_{out} = 0$$

$$\Rightarrow \frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mI}\left(g_{mII} - sC_c\right)}{G_IG_{II} + s\left[G_{II}\left(C_I + C_{II}\right) + G_I\left(C_{II} + C_c\right) + g_{mII}C_c\right] + s^2\left[C_IC_{II} + C_cC_I + C_cC_{II}\right]}$$

$$\Rightarrow \frac{V_{out}(s)}{V_{in}(s)} = \frac{A_0\left(1 - \dfrac{s}{g_{mII}/C_c}\right)}{1 + s\left[R_I\left(C_I + C_{II}\right) + R_{II}\left(C_{II} + C_c\right) + g_{mII}R_IR_{II}C_c\right] + s^2R_IR_I\left[C_IC_{II} + C_cC_I + C_cC_{II}\right]}$$

$$A_0 = \frac{g_Ig_{II}}{G_IG_{II}} = \frac{g_{m1}}{g_{ds2} + g_{ds4}}\frac{g_{m6}}{g_{ds6} + g_{ds7}}$$

$$D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1p_2}$$

$$\left|p_2\right| >> \left|p_1\right| \Rightarrow D(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1p_2} = 1 + as + bs^2$$

$$\Rightarrow p_1 = -\frac{1}{a},\ p_2 = -\frac{a}{b}$$

$$p_1 = -\frac{1}{R_I\left(C_I + C_{II}\right) + R_{II}\left(C_{II} + C_c\right) + g_{mII}R_I R_{II} C_c} \approx -\frac{1}{g_{mII}R_I R_{II} C_c} = -\frac{g_{ds2} + g_{ds4}}{g_{m6}}\frac{g_{ds6} + g_{ds7}}{C_c}$$

$$C_I < C_c < C_{II}$$

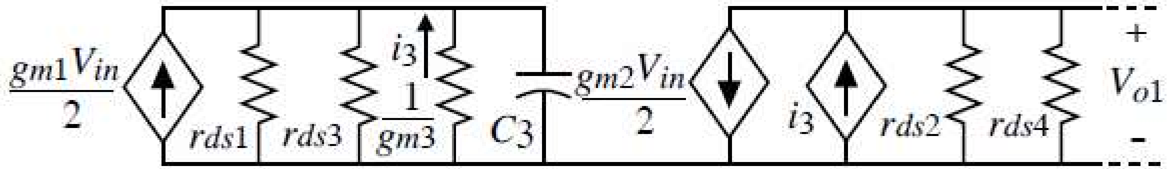
$$p_2 = -\frac{a}{b} = -\frac{R_I\left(C_I + C_{II}\right) + R_{II}\left(C_{II} + C_c\right) + g_{mII}R_I R_{II} C_c}{R_I R_I\left[C_I C_{II} + C_c C_I + C_c C_{II}\right]} \approx -\frac{g_{mII}}{C_{II}} = -\frac{g_{m6}}{C_L}$$

✓Right-half plane zero: $z_1 = +\frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c}$

✓The unity gain bandwidth: $GB = A_0\left|p_1\right| = \frac{g_I g_{II}}{G_I G_{II}}\frac{1}{g_{mII}R_I R_{II} C_c} = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c}$

✓ω_{p2} must be greater than unity-gainbandwidth or satisfactory phase margin will not be achieved.

•Influence of the Mirror Pole

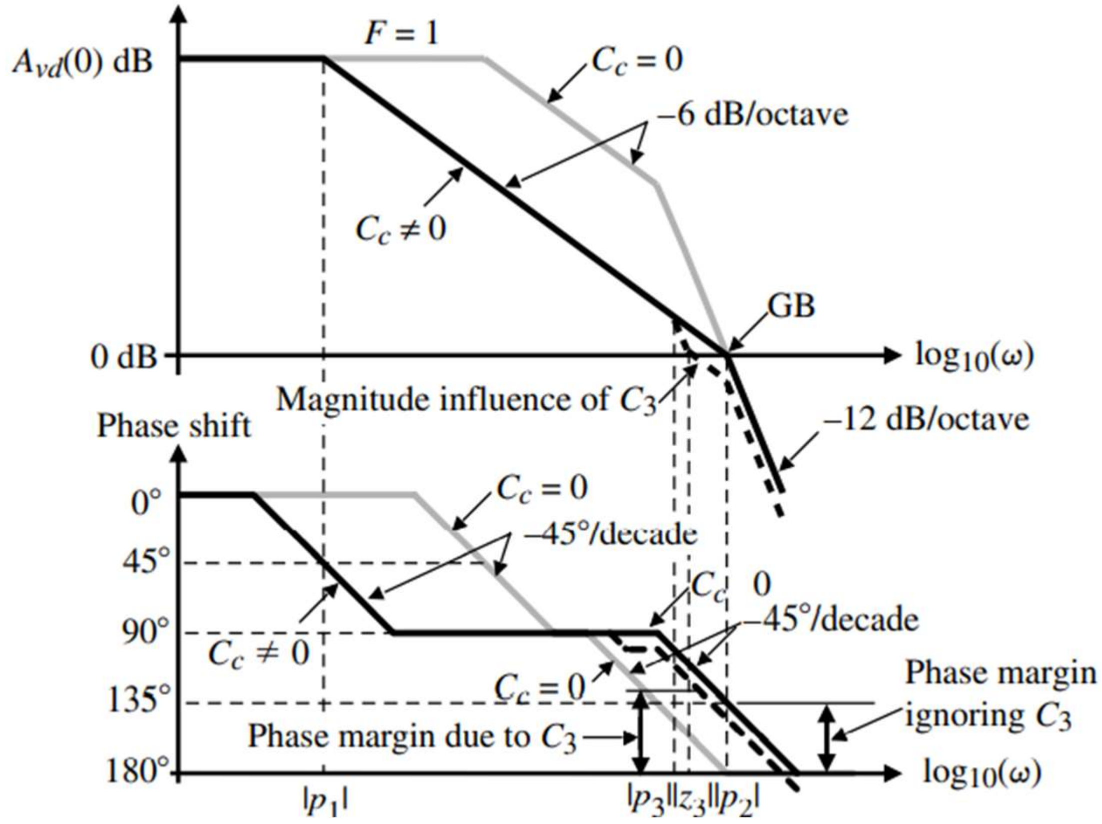


$$C_M = C_3 = C_{db1} + C_{db3} + C_{gs3} + C_{gs4}$$

The transfer function from the input to the output voltage of the first stage

$$\frac{V_{01}(s)}{V_{in}(s)} = -\frac{g_{m1}/2}{g_{ds2} + g_{ds4}}\left[\frac{g_{m3} + g_{ds1} + g_{ds3}}{g_{m3} + g_{ds1} + g_{ds3} + sC_3} + 1\right] \approx -\frac{g_{m1}}{g_{ds2} + g_{ds4}}\frac{1 + \frac{s}{2g_{m3}/C_3}}{1 + \frac{s}{g_{m3}/C_3}}$$

$$z_3 = -2g_{m3} / C_3$$
$$p_3 = -g_{m3} / C_3$$



•The requirement for 45° phase margin is:

$$\Phi_M = \pm 180^\circ - \arg\left[A(j\omega)F(j\omega)\right] = \pm 180^\circ - arctg\left(\frac{\omega}{\omega_{p1}}\right) - arctg\left(\frac{\omega}{\omega_{p2}}\right) - arctg\left(\frac{\omega}{\omega_{z1}}\right) = 45^\circ$$

$$\omega_{pi} = -p_i, i = 1, 2, \omega_{z1} = -z_1$$

✓Let ω = *GB* and assume that ω_{z1} *>=10GB,*

$$45^\circ = \pm 180^\circ - arctg\left(\frac{GB}{\omega_{p1}}\right) - arctg\left(\frac{GB}{\omega_{p2}}\right) - arctg(0.1)$$

$$\Rightarrow 135^\circ \approx arctg\left(A_0\right)+arctg\left(\frac{GB}{\omega_{p2}}\right)+arctg\left(0.1\right),\ A_0 >> 1$$

$$\Rightarrow 135^\circ \approx 90^\circ + arctg\left(\frac{GB}{\omega_{p2}}\right)+5.7^\circ \Rightarrow 135^\circ \approx 90^\circ + arctg\left(\frac{GB}{\omega_{p2}}\right)+5.7^\circ$$

$$\Rightarrow arctg\left(\frac{GB}{\omega_{p2}}\right)^\circ \approx 39.3^\circ \Rightarrow \frac{GB}{\omega_{p2}} = 0.818 \Rightarrow \omega_{p2} \geq 1.22 \cdot GB$$

✓If 60° phase margin is required, then the following relationships apply:

$$\omega_{z1} \geq 10GB \Rightarrow \omega_{p2} \geq 2.2 \cdot GB$$

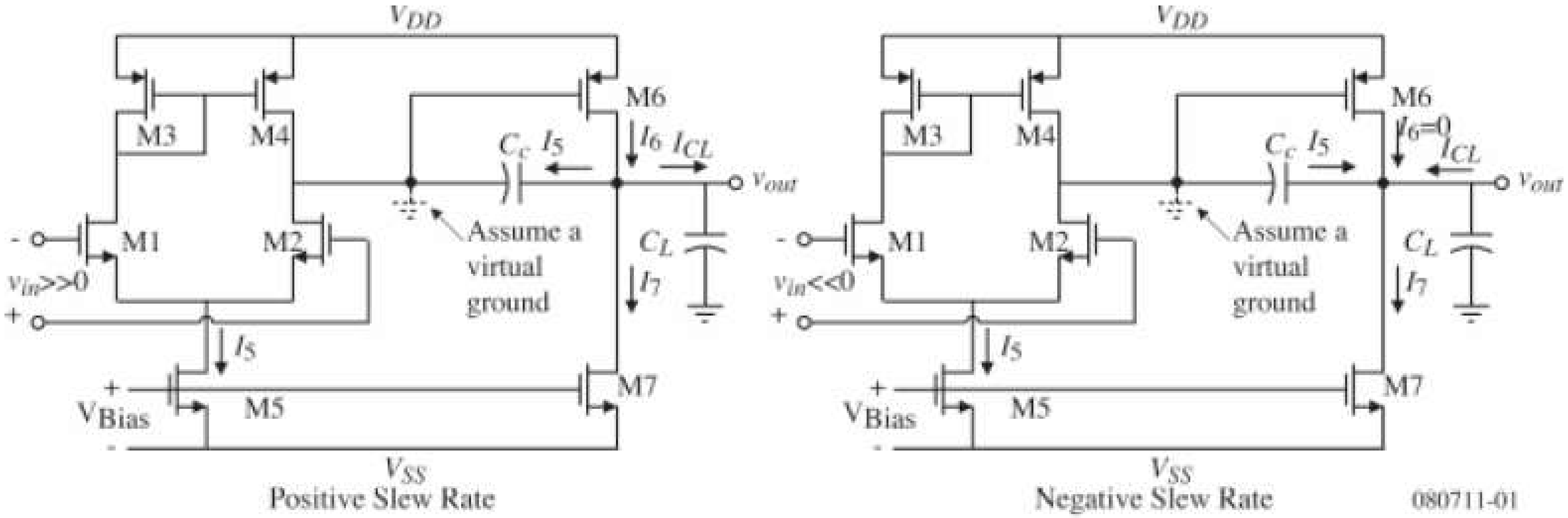
$$\frac{g_{m6}}{C_c} > \frac{10 g_{m1}}{C_c} \Rightarrow g_{m6} > 10 g_{m1}$$

$$\frac{g_{m6}}{C_c} > \frac{2.2 g_{m1}}{C_c} \Rightarrow C_c > 0.22 C_2$$

➢CMOS op amp Slew Rate (SR)

•Slew rate occurs when currents flowing in a capacitor become limited and is given as

$$I_{\lim} = C\frac{dv_C}{dt}$$



$$SR^{+} = \min\left[\frac{I_5}{C_c}, \frac{I_6 - I_5 - I_7}{C_L}\right] = \frac{I_5}{C_c}, I_6 >> I_5 \qquad SR^{-} = \min\left[\frac{I_5}{C_c}, \frac{I_7 - I_5}{C_L}\right] = \frac{I_5}{C_c}, if\ I_7 >> I_5$$

✓Therefore, if CL is not too large and if I7 is significantly greater than I5, then the slew rate of the two-stage op amp should be, I5/Cc.

➢RIGHT-HALF PLANE ZERO

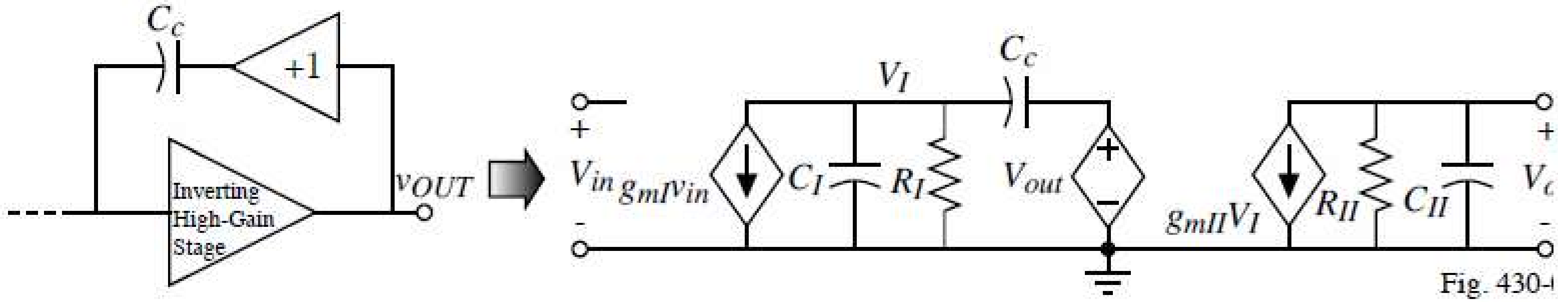
▪Controlling the Right-Half Plane Zero

Why is the RHP zero a problem?

✓Because it boosts the magnitude but lags the phase - the worst possible combination for stability.

✓Solution of the problem: The compensation comes from the feedback path through Cc, but the RHP zero comes from the feedforward path through Cc so eliminate the feedforward path!

➢Use of Buffer to Eliminate the Feedforward Path through the Miller Capacitor



$$\Rightarrow \frac{V_{out}(s)}{V_{in}(s)} = \frac{A_0}{1 + s\left[R_I(C_I + C_{II}) + R_{II}C_{II} + g_{mII}R_IR_{II}C_c\right] + s^2R_IR_{II}C_{II}(C_I + C_c)}$$

$$p_1 = -\frac{1}{R_I(C_I + C_{II}) + R_{II}C_{II} + g_{mII}R_IR_{II}C_c} \approx -\frac{1}{g_{mII}R_IR_{II}C_c} = -\frac{g_{ds2} + g_{ds4}}{g_{m6}}\frac{g_{ds6} + g_{ds7}}{C_c}$$

$$C_I < C_c < C_{II}$$

$$p_2 = -\frac{a}{b} = -\frac{R_I(C_I + C_{II}) + R_{II}C_{II} + g_{mII}R_IR_{II}}{R_IR_{II}C_{II}(C_I + C_c)} \approx -\frac{g_{mII}C_c}{C_{II}(C_I + C_c)}$$

✓Poles are approximately what they were before with the zero removed
✓For 45° phase margin, ω_{p2} must be greater than *GB*
✓For 60° phase margin, , ω_{p2} must be greater than *1.73GB*

➢Use of Buffer with Finite Output Resistance to Eliminate the RHP Zero

•Assume that the unity-gain buffer has an output resistance of Ro

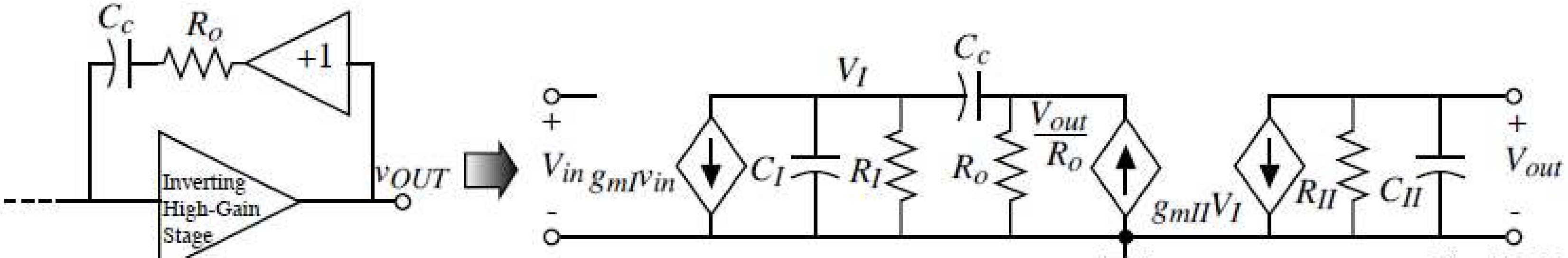


Fig. 430-03

• It can be shown that if the output resistance of the buffer amplifier, Ro, is not neglected that another pole occurs at,

$$p_4 \approx -\frac{1}{R_0\left[\left(C_I C_c\right)\left(C_I + C_c\right)\right]}$$

and a LHP zero at

$$z_2 \approx -\frac{1}{R_0 C_c}$$

✓Although the LHP zero can be used for compensation, the additional pole makes this method less desirable than the following method.

➢Use of Nulling Resistor to Eliminate the RHP Zero (or turn it into a LHP zero)

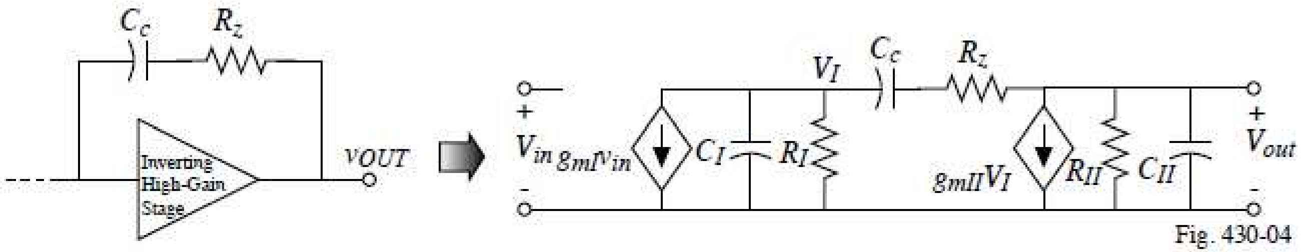


Fig. 430-04

Nodal Equations:

$$g_{mI}V_{in} + \frac{V_I}{R_I} + sC_IV_I + \left(\frac{sC_c}{1+sC_cR_z}\right)\left(V_I - V_{out}\right) = 0$$

$$g_{mI}V_I + \frac{V_I}{R_{II}} + sC_{II}V_{out} + \left(\frac{sC_c}{1+sC_cR_z}\right)\left(V_{out} - V_I\right) = 0$$

$$\Rightarrow \frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mI}g_{mII}R_IR_{II}\left(1 - s\left[\frac{C_c}{g_{mII}} - R_zC_c\right]\right)}{1 + bs + cs^2 + ds^3}$$

$$b = R_I\left(C_I + C_c\right) + R_{II}\left(C_{II} + C_c\right) + g_{mII}R_IR_{II}C_c + R_zC_c$$

$$c = R_IR_{II}\left(C_IC_{II} + C_cC_I + C_cC_{II}\right) + R_zC_c\left(R_IC_I + R_{II}C_{II}\right)$$

$$d = R_IR_{II}C_IC_{II}C_cR_z$$

✓If Rz is assumed to be less than R_I or R_{II} and the poles widely spaced, then the roots of the above transfer function can be approximated as

$$p_1 = -\frac{1}{R_I\left(C_I + C_c\right) + R_{II}\left(C_{II} + C_c\right) + g_{mII}R_IR_{II}C_c + R_zC_c} \approx -\frac{1}{\left(1 + g_{mII}R_{II}\right)R_IC_c} \approx -\frac{1}{g_{mII}R_{II}R_IC_c}$$

$$p_2 \approx -\frac{g_{mII}C_c}{C_cC_I + C_IC_{II} + C_cC_{II}} \approx -\frac{g_{mII}}{C_{II}}$$

$$z_1 = \frac{1}{C_c\left(\frac{1}{g_{mII}} - R_z\right)}$$

$$p_4 \approx -\frac{1}{R_zC_I}$$

✓**Note that the zero can be placed anywhere on the real axis!**
✓**We desire that z1 = p2 in terms of the previous notation**

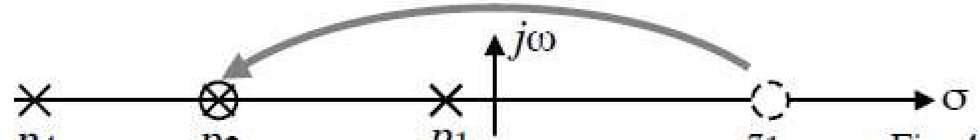


Fig. 430-06

$$p_2 = z_1 \Rightarrow C_c\left(\frac{1}{g_{mII}} - R_z\right) = -\frac{C_{II}}{g_{mII}} \Rightarrow R_z = \frac{C_c + C_{II}}{C_c}\frac{1}{g_{mII}}$$

✓With p2 canceled, the remaining roots are p1 and p4(the pole due to Rz) . For unity-gain stability, all that is required is that

$$\omega_{p4} > A_0\omega_{p1} = \frac{A_0}{g_{mII}R_{II}R_I C_c} = GB$$

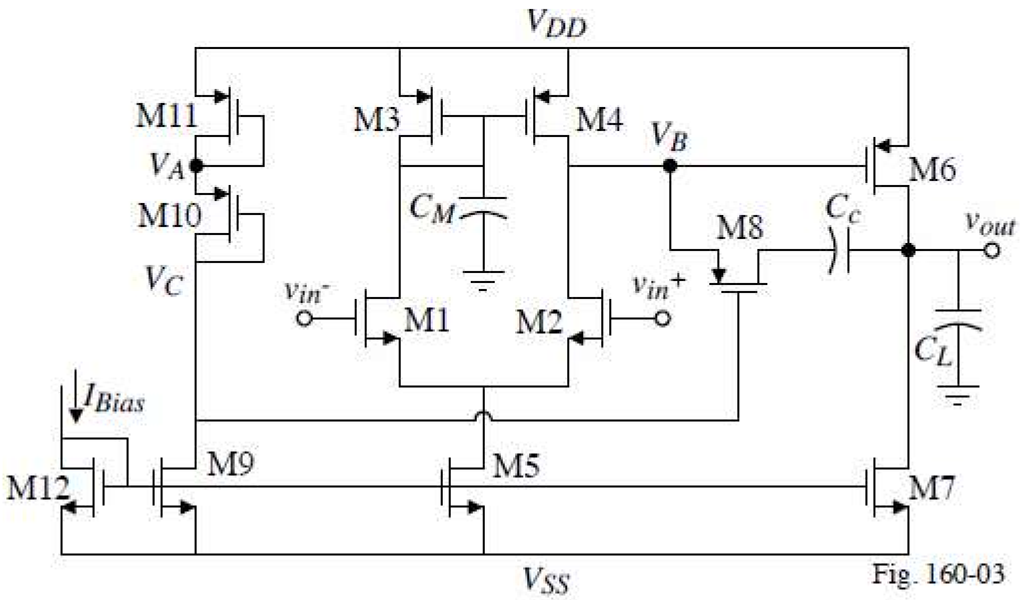
$$\frac{1}{R_z C_I} > \frac{g_{mI}}{C_c} = GB$$

✓Substituting Rz into the above inequality and assuming C_{II} >> C_c results in

$$C_c > \sqrt{\frac{g_{mI}}{g_{mII}} C_I C_{II}}$$

✓This procedure gives excellent stability for a fixed value of C_{II} (≈ C_L).
✓**Unfortunately, as C_L changes, p2 changes and the zero must be readjusted to cancel p2!**

➢Incorporating the Nulling Resistor into the Miller Compensated Two-Stage Op Amp



$$p_1 \approx -\frac{1}{g_{mII}R_{II}R_I C_c} = -\frac{g_{mI}}{(g_{mII}g_{mI}R_{II}R_I)C_c} = -\frac{g_{mI}}{A_0 C_c} \qquad p_2 \approx -\frac{g_{mII}}{C_{II}} \approx -\frac{g_{m6}}{C_L}$$

$$p_4 \approx -\frac{1}{R_z C_I} \qquad z_1 = \frac{1}{C_c\left(\frac{1}{g_{m6}} - R_z\right)}$$

•Design of the Nulling Resistor (M_8)

✓For the zero to be on top of the second pole (p2), the following relationship must hold

$$R_z = \frac{C_c + C_{II}}{C_c}\frac{1}{g_{mII}} \approx \frac{C_c + C_L}{C_c}\frac{1}{g_{m6}} = \frac{C_c + C_L}{C_c}\frac{1}{\sqrt{2I_{D6}\mu_p C_{ox}(W/L)_6}}$$

✓The resistor, Rz, is realized by the transistor M8 which is operating in the triode region because the dc current through it is zero. Therefore, Rz, can be written as

$$R_z = \left.\frac{1}{\partial i_{D8} / \partial v_{DS8}}\right|_{V_{DS8}=0} = \frac{1}{\mu_p C_{ox} (W/L)_8 \left(V_{SG8} - |V_{THP}|\right)}$$

✓The bias circuit is designed so that voltage VA is equal to VB. As a result

$$|V_{GS10} - V_{THP}| = \sqrt{\frac{2I_{D10}}{\mu_p C_{ox} (W/L)_{10}}} = |V_{GS8} - V_{THP}|$$

✓Equating the two expressions for Rz gives

$$R_z = \frac{1}{\mu_p C_{ox} (W/L)_8 \sqrt{\frac{2I_{D10}}{\mu_p C_{ox} (W/L)_{10}}}} = \frac{1}{(W/L)_8} \sqrt{\frac{(W/L)_{10}}{2\mu_p C_{ox} I_{D10}}}$$

$$R_z = \frac{C_c + C_L}{C_c} \frac{1}{\sqrt{2I_{D6} \mu_p C_{ox} (W/L)_6}} = \frac{1}{(W/L)_8} \sqrt{\frac{(W/L)_{10}}{2\mu_p C_{ox} I_{D10}}}$$

$$\Rightarrow (W/L)_8 = \frac{C_c}{C_c + C_L} \sqrt{(W/L)_{10} (W/L)_6 \frac{I_{D6}}{I_{D10}}}$$

$$V_{GS11} = V_{GS6} \Rightarrow \left(\frac{W}{L}\right)_{11} = \frac{I_{D10}}{I_{D6}} \left(\frac{W}{L}\right)_6 \Rightarrow \quad (W/L)_8 = \frac{C_c}{C_c + C_L} \sqrt{\frac{(W/L)_{10} (W/L)_6^2}{(W/L)_{11}}}$$

•An Alternate Form of Nulling Resistor

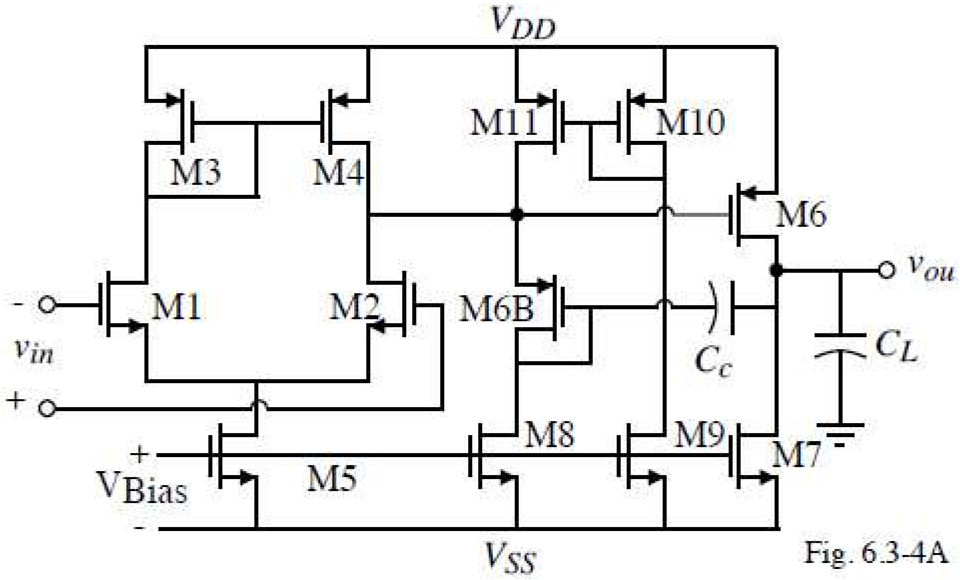


Fig. 6.3-4A

✓To cancel p2,

$$R_z \approx \frac{C_c + C_L}{C_c}\frac{1}{g_{m6}} = \frac{1}{g_{m6B}} \Rightarrow g_{m6} = g_{m6B}\left(1 + \frac{C_L}{C_c}\right)$$

$$\sqrt{\frac{2I_{D6}}{\mu_p C_{ox}(W/L)_6}} = \sqrt{\frac{2I_{D6B}}{\mu_p C_{ox}(W/L)_{6B}}}\left(1 + \frac{C_L}{C_c}\right)$$

➢Increasing the Magnitude of the Output Pole

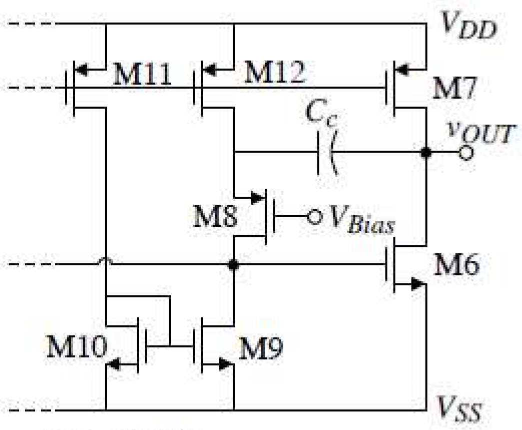
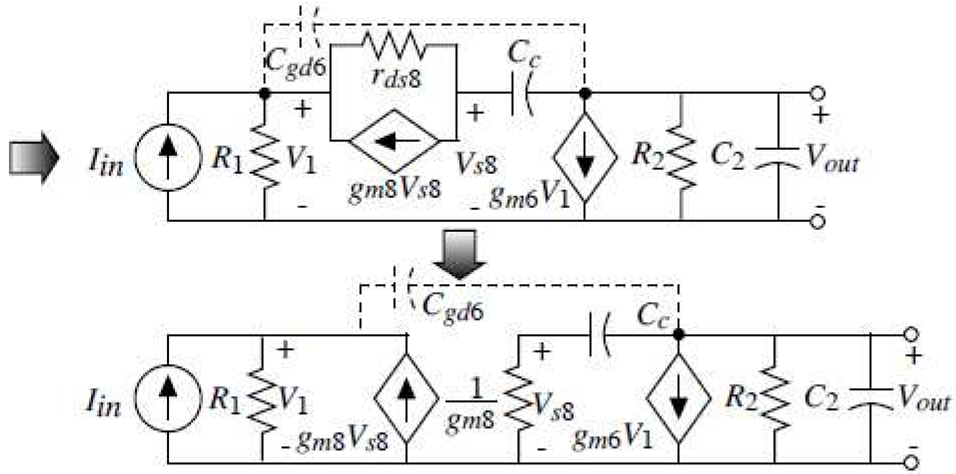


Fig. 6.2-15B



$$R_1 = \frac{1}{g_{ds2} + g_{ds4} + g_{ds9}} \qquad R_2 = \frac{1}{g_{ds6} + g_{ds7}}$$

Nodal equations:

$$I_{in} = G_1 V_1 - g_{m8} V_{s8} = G_1 V_1 - \frac{g_{m8} s C_c}{g_{m8} + s C_c} V_{out}$$

$$0 = g_{m6} V_1 + \left(G_2 + s C_2 + \frac{g_{m8} s C_c}{g_{m8} + s C_c} \right) V_{out}$$

✓Solving for the transfer function Vout/Iin gives

$$\frac{V_{out}(s)}{I_{in}(s)} = -\frac{g_{m6}}{G_1 G_2} \frac{1 + \frac{s C_c}{g_{m8}}}{1 + s\left(\frac{C_c}{g_{m8}} + \frac{C_2}{G_2} + \frac{C_c}{G_2} + \frac{g_{m6} C_c}{G_1 G_2} \right) + s^2 \frac{C_1 C_2}{g_{m8} G_2}}$$

✓Using the approximate method of solving for the roots of the denominator gives

$$p_1 = -\frac{1}{\frac{C_c}{g_{m8}} + \frac{C_2}{G_2} + \frac{C_c}{G_2} + \frac{g_{m6}C_c}{G_1 G_2}} \approx -\frac{6}{g_{m6} r_{ds}^2 C_c}$$

$$p_2 = -\frac{\frac{g_{m6} r_{ds}^2 C_c}{6}}{\frac{C_c C_2}{g_{m8} G_2}} = -\frac{g_{m8} r_{ds}^2 G_2}{6} \frac{g_{m6}}{C_2} = \frac{g_{m8} r_{ds}}{3} p_2' \qquad z_2 = -\frac{g_{m8}}{C_c}$$

where all the various channel resistance have been assumed to equal rds and p2' is the output pole for normal Miller compensation.

✓Result: Dominant pole is approximately the same and the output pole is increased by $\approx g_m r_{ds}$

✓In addition there is a LHP zero at $-g_{m8}/sC_c$ and a RHP zero due to C_{gd6} (shown dashed in the previous model) at g_{m6}/C_{gd6}.

✓Roots are:

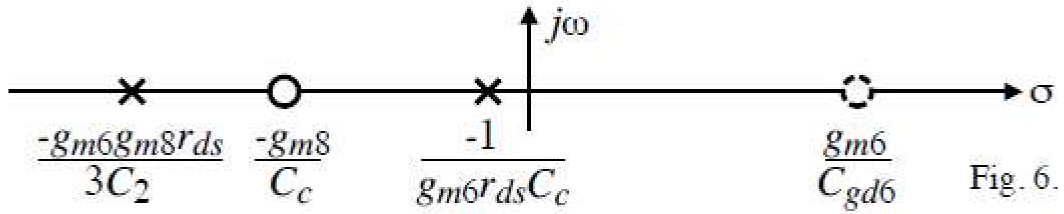


Fig. 6.

➢FEEDFORWARD COMPENSATION

✓Use two parallel paths to achieve a LHP zero for lead compensation purposes

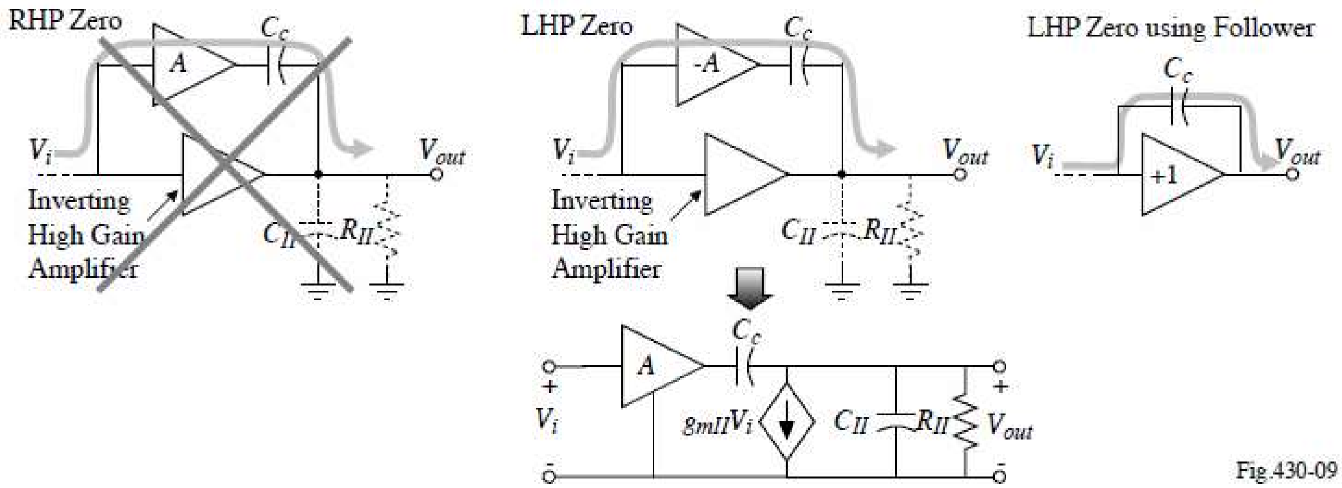


Fig.430-09

$$\frac{V_{out}(s)}{V_i(s)} = \frac{AC_c}{C_c + C_{II}} \frac{s + \frac{g_{mII}}{AC_c}}{s + \frac{1}{R_{II}C_c + C_{II}}}$$

•To use the LHP zero for compensation, a compromise must be observed

✓Placing the zero below GB will lead to boosting of the loop gain that could deteriorate the phase margin

✓Placing the zero above GB will have less influence on the leading phase caused by the zero

• Note that a source follower is a good candidate for the use of feedforward compensation

✓This type of compensation is often used in source followers. The capacitor will provide a path that bypasses the transistor at high frequencies

♦ POWER SUPPLY REJECTION RATIO OF THE TWO-STAGE OP AMP

What is *PSRR?*

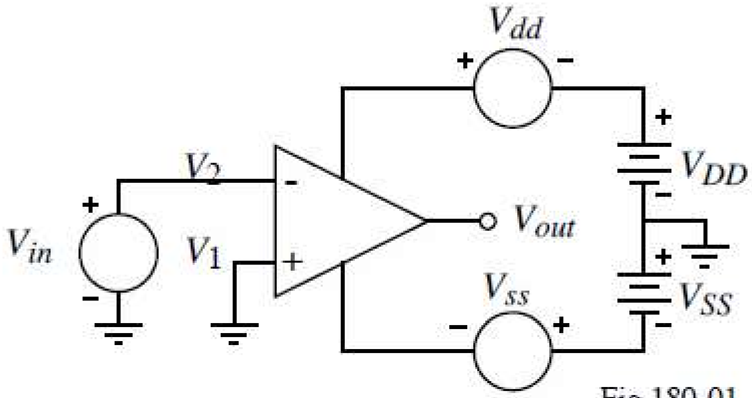


Fig.180-01

$$PSRR^{+} = \frac{A_v\left(v_{dd}=0\right)}{A_{dd}\left(v_{in}=0\right)}$$

$$PSRR^{-} = \frac{A_v\left(v_{ss}=0\right)}{A_{ss}\left(v_{in}=0\right)}$$

Method for calculating PSRR:

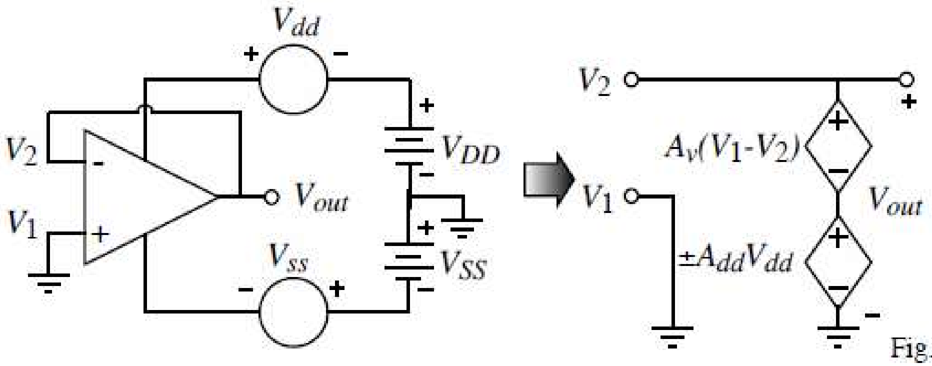


Fig. 180-02

$$V_{out} = A_{dd}V_{dd} - A_vV_2 = A_{dd}V_{dd} - A_vV_{out}$$

$$V_{out} = \frac{A_{dd}}{1+A_v}V_{dd} \approx \frac{A_{dd}}{A_v}V_{dd} = \frac{1}{PSRR^{+}}V_{dd}$$

$$\Rightarrow PSRR^{+} = \frac{V_{dd}}{V_{out}} \qquad \Rightarrow PSRR^{-} = \frac{V_{ss}}{V_{out}}$$

✓If we connect the op amp in the unity-gain mode and input an AC signal of Vdd (Vss) in series with VDD (VSS), PSRR will be equal

$$PSRR^{+} = \frac{V_{dd}}{V_{out}} \qquad PSRR^{-} = \frac{V_{ss}}{V_{out}}$$

❖Negative *PSRR*

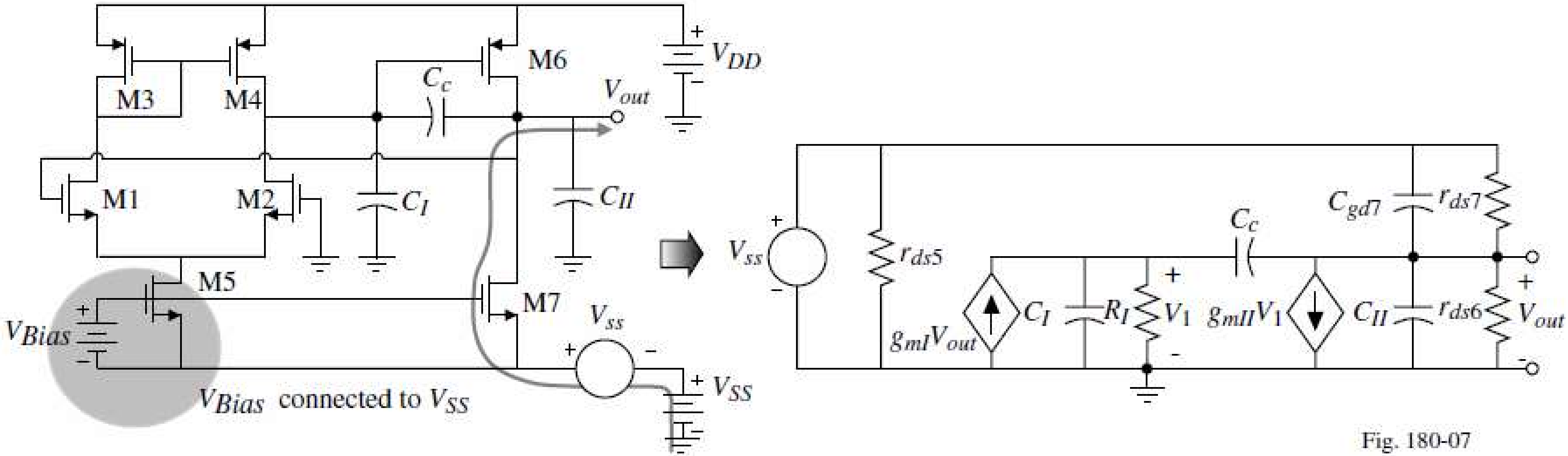


Fig. 180-07

$$(G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_{out} = 0$$

$$(g_{mII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II} + sC_{gd7})V_{out} = (g_{ds7} + sC_{gd7})V_{ss}$$

Solving for Vout/Vss and inverting:

$$\frac{V_{ss}}{V_{out}} = \frac{as^2 + bs + c}{g_{m7}\left[G_I + s(C_c + C_I)\right]}$$

$$a = C_cC_I + C_IC_{II} + C_{II}C_c + C_IC_{gd7} + C_cC_{gd7}$$

$$b = G_I(C_c + C_{II} + C_{gd7}) + G_{II}(C_c + C_I) + C_c(g_{mII} - g_{mI})$$

$$c = G_IG_{II} + g_{mII}g_{mI}$$

Solve for approximate roots:

$$PSRR^- = \frac{V_{ss}}{V_{out}} = \frac{g_{mII}g_{mI}}{G_Ig_{ds7}} \frac{\left(1 + s\frac{C_c}{g_{mI}}\right)\left(1 + s\frac{(C_cC_I + C_cC_{II} + C_cC_{II})}{g_{mII}C_c}\right)}{\left(1 + s\frac{C_c + C_I}{G_I}\right)\left(1 + s\frac{C_{gd7}}{g_{ds7}}\right)}$$

$$PSRR^{-} = \frac{V_{ss}}{V_{out}} \approx \frac{g_{mII}g_{mI}}{G_I g_{ds7}} \frac{\left(1+s\frac{C_c}{g_{mI}}\right)\left(1+s\frac{C_{II}}{g_{mII}}\right)}{\left(1+s\frac{C_{gd7}}{g_{ds7}}\right)\left(1+s\frac{C_c}{G_I}\right)} = \frac{G_{II}A_v(0)}{g_{ds7}} \frac{\left(1+\frac{s}{GB}\right)\left(1+\frac{s}{\omega_{p2}}\right)}{\left(1+s\frac{C_{gd7}}{g_{ds7}}\right)\left(1+\frac{s}{GB}\frac{g_{mI}}{G_I}\right)}$$

Comments:

- DC gain has been increased by the ratio of G_{II} to g_{ds7}
- Two poles instead of one, however the pole at $-g_{ds7}/C_{gd7}$ is large and can be ignored.

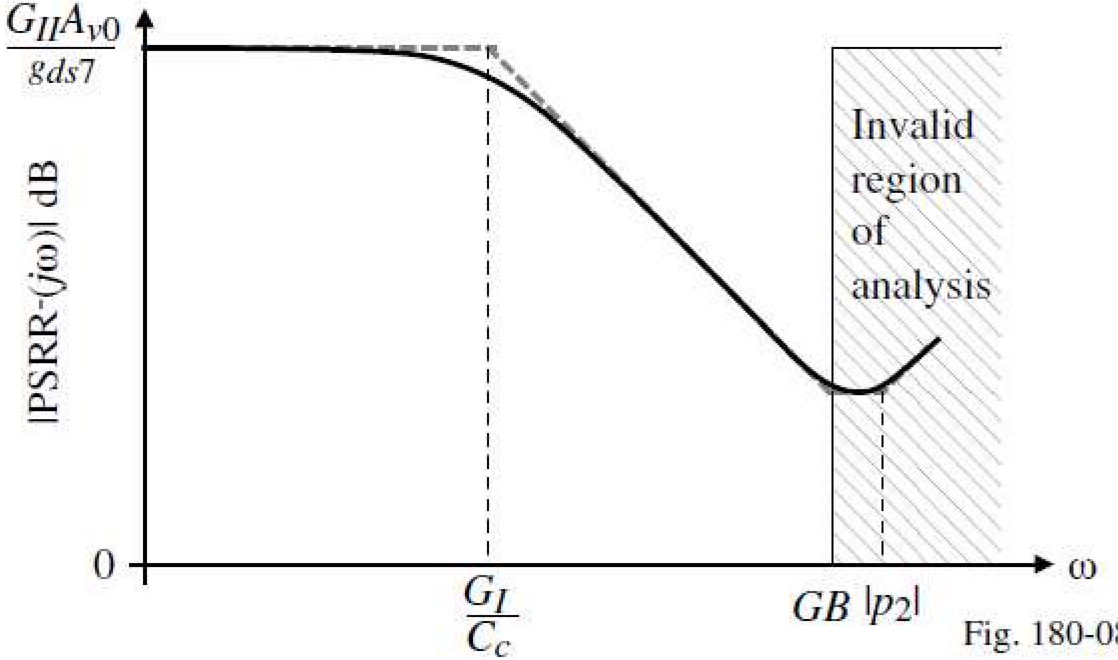


Fig. 180-08

❖Positive *PSRR*

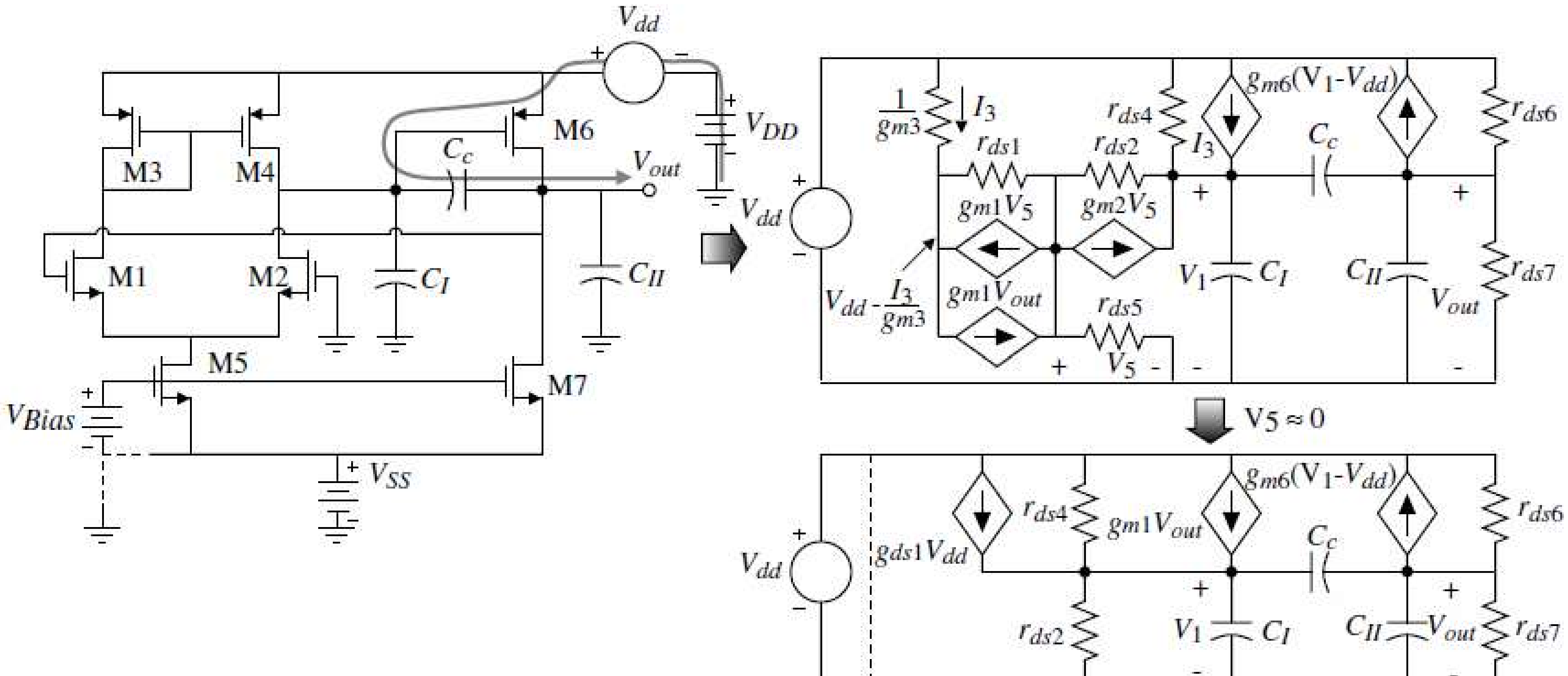


Fig. 180-03

$$\left(G_I + sC_c + sC_I\right)V_1 - \left(g_{mI} + sC_c\right)V_{out} = G_I V_{dd}$$

$$\left(g_{mII} - sC_c\right)V_1 + \left(G_{II} + sC_c + sC_{II}\right)V_{out} = \left(g_{mII} + g_{ds6}\right)V_{dd}$$

$$G_I = g_{ds1} + g_{ds4} = g_{ds2} + g_{ds4},\, G_{II} = g_{ds6} + g_{ds7},\, g_{mI} = g_{m1} = g_{m2},\, g_{mII} = g_{m6}$$

Using Cramers rule to solve for the transfer function V_{out}/V_{dd}, and inverting the transfer function gives the following result

$$\frac{V_{ss}}{V_{out}} = \frac{as^2 + bs + c}{G_I g_{ds6} + s\left[C_c\left(g_{mII} + G_I + g_{ds6}\right) + C_I\left(g_{mII} + g_{ds6}\right)\right]}$$

$$a = C_c C_I + C_I C_{II} + C_{II} C_c$$

$$b = G_I\left(C_c + C_{II}\right) + G_{II}\left(C_c + C_I\right) + C_c\left(g_{mII} - g_{mI}\right)$$

$$c = G_I G_{II} + g_{mII} g_{mI}$$

✓We may solve for the approximate roots of numerator as

$$PSRR^+ = \frac{V_{dd}}{V_{out}} = \frac{g_{mII} g_{mI}}{G_I g_{ds6}} \frac{\left(1 + s\frac{C_c}{g_{mI}}\right)\left(1 + s\frac{\left(C_c C_I + C_c C_{II} + C_c C_{II}\right)}{g_{mII} C_c}\right)}{\left[1 + s\frac{g_{mII} C_c}{G_I g_{ds6}}\right]}$$

Where $g_{mII} > g_{mI}$ and that all transconductances are larger than the channel conductances:

$$PSRR^+ = \frac{V_{dd}}{V_{out}} = \frac{g_{mII} g_{mI}}{G_I g_{ds6}} \frac{\left(1 + s\frac{C_c}{g_{mI}}\right)\left(1 + s\frac{C_{II}}{g_{mII}}\right)}{\left[1 + s\frac{g_{mII} C_c}{G_I g_{ds6}}\right]} = \frac{G_{II} A_v(0)}{g_{ds6}} \frac{\left(1 + \frac{s}{GB}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}{\left[1 + \frac{s}{GB}\frac{G_{II} A_v(0)}{g_{ds6}}\right]}$$

✓At approximately the dominant pole, the PSRR falls off with a -20dB/decade slope and degrades the higher frequency PSRR + of the two-stage op amp.

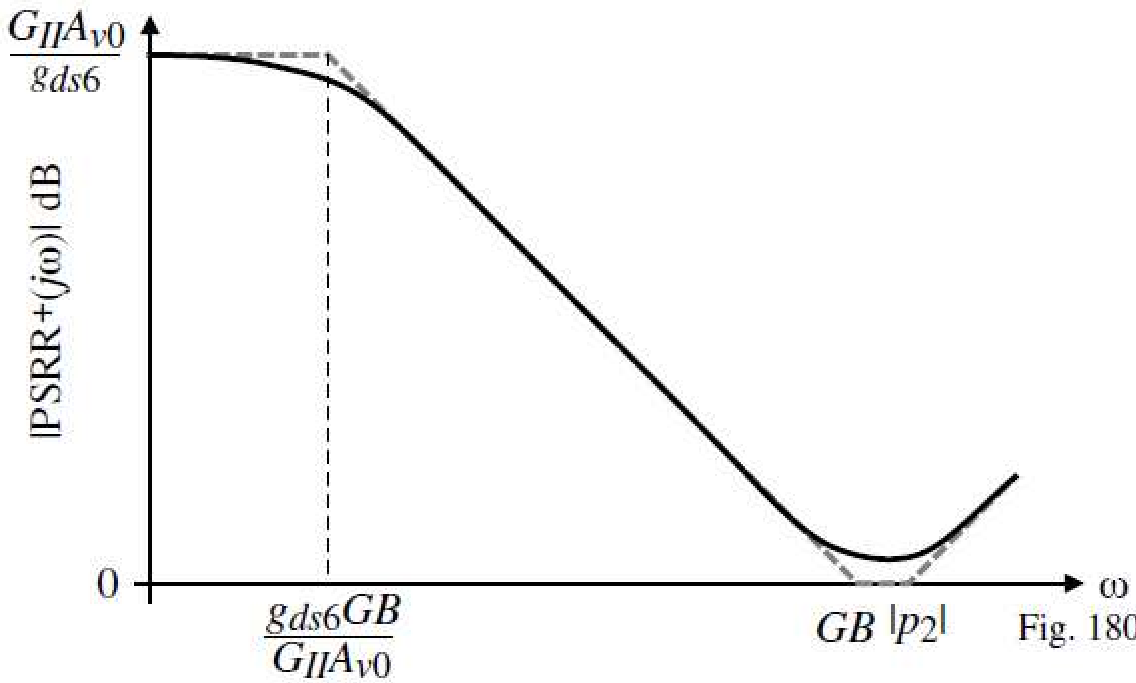


Fig. 180-04

Approximate Model for *PSRR+*

The M7 current sink causes VSG6 to act like a battery

2) Therefore, Vdd couples from the source to gate of M6

3) The path to the output is through any capacitance from gate to drain of M6

✓Conclusion: The Miller capacitor Cc couples the positive power supply ripple directly to the output.

✓**Must reduce or eliminate Cc!**

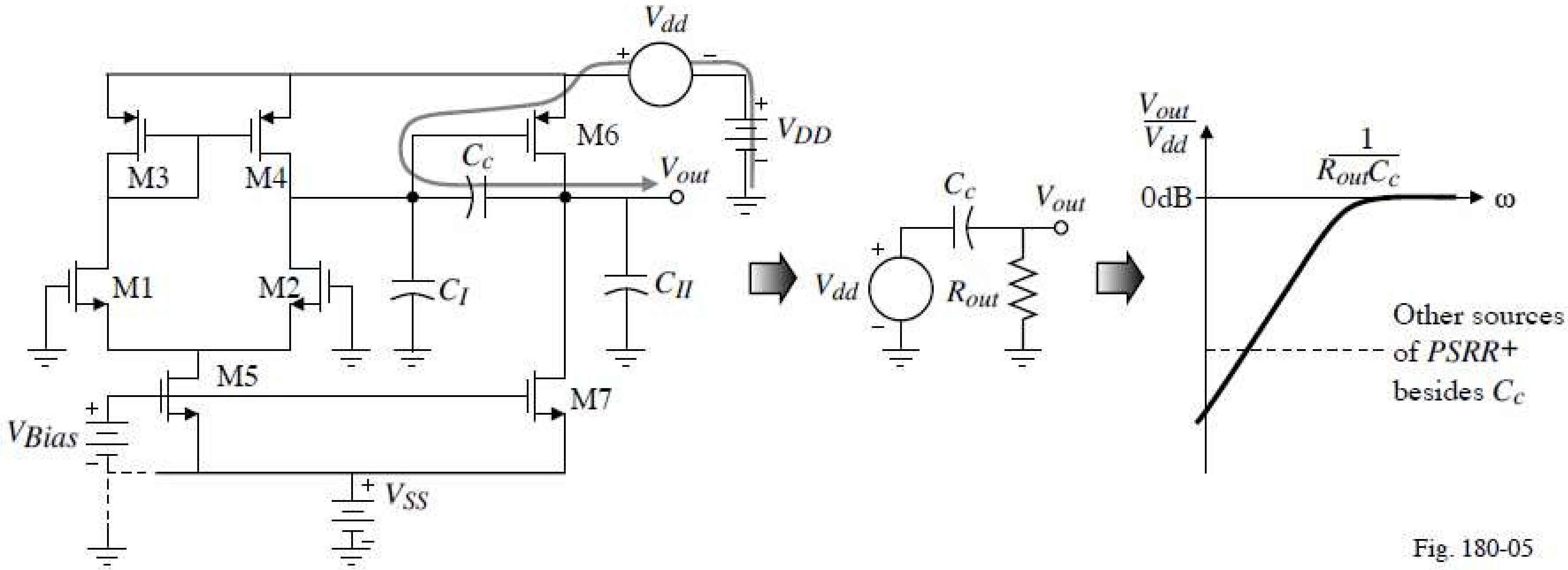


Fig. 180-05

Approximate Model for **Negative *PSRR with VBias Connected to Ground***

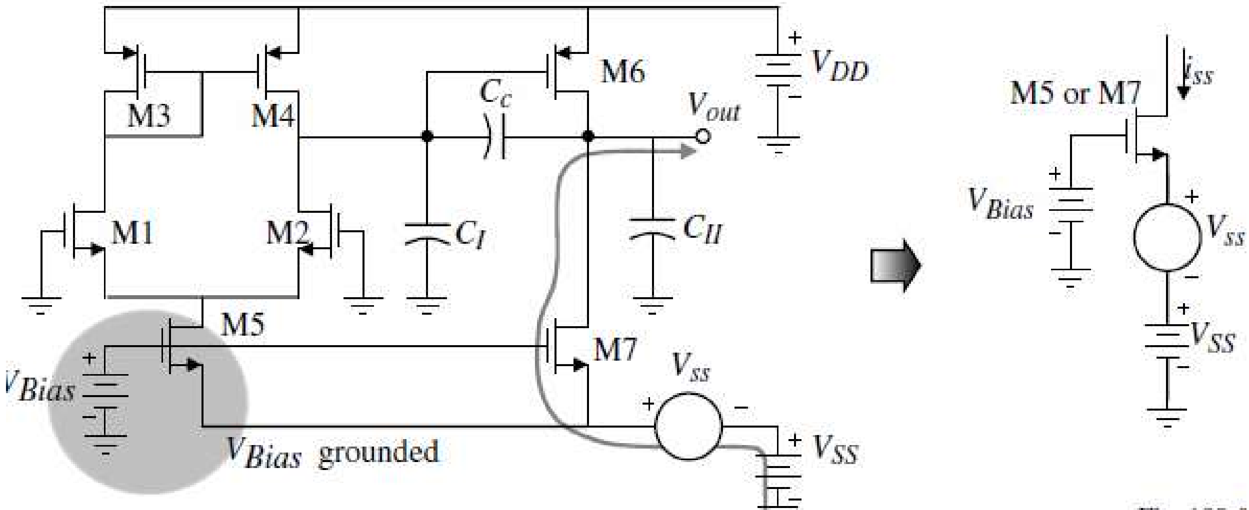
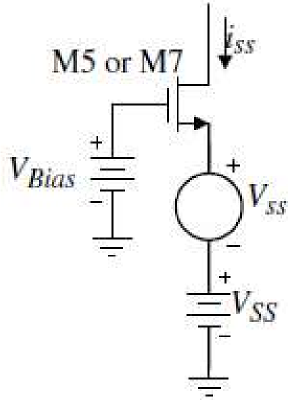


Fig. 180-(

✓Path through the input stage is not important as long as the *CMRR is high*



Path through the output stage:

$$V_{out} \approx I_{ss} Z_{out} = g_{m7} V_{ss} Z_{out}$$

$$Z_{out} = R_{out} \parallel \frac{1}{sC_{out}} = \frac{R_{out}}{1 + sC_{out} R_{out}}$$

$$\frac{V_{out}}{V_{ss}} \approx \frac{g_{m7} R_{out}}{1 + sC_{out} R_{out}}$$

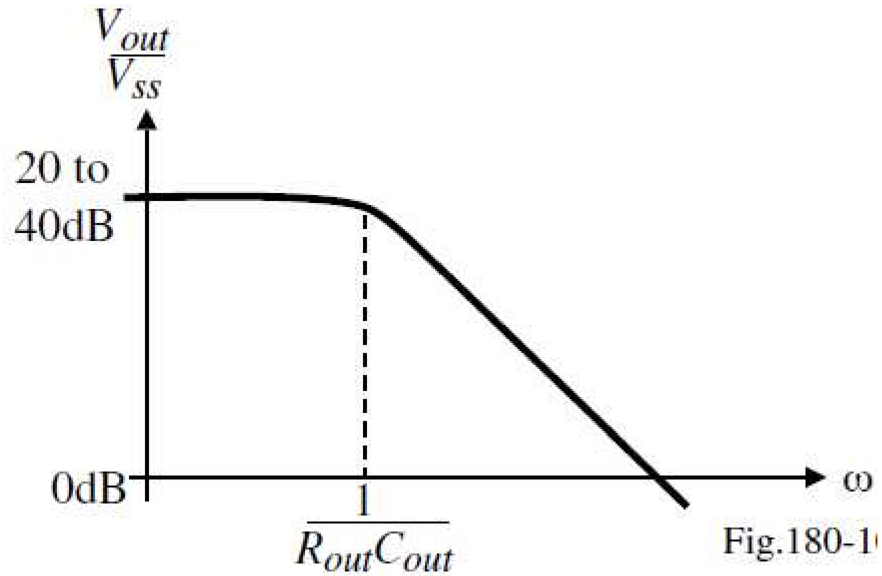


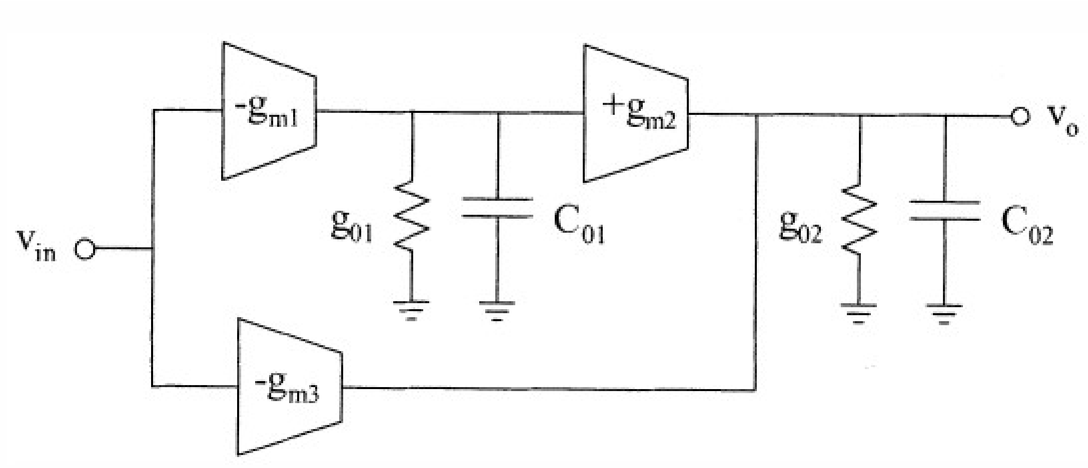
Fig.180-1

✓The two-stage op amp will never have good PSRR because of the Miller compensation
✓The two-stage op amp is a very general and flexible op amp
✓**Cascoding!**

➢Feedforward compensation without Miller Capacitor

•The compensation scheme used in this paper employs a feedforward path to create LHP zeros, but does not use any Miller capacitor.

•The dominant pole is not pushed to lower frequencies, resulting in a higher gain-bandwidth product with a fast step response.



$$A_{vi} = \frac{g_{mi}}{g_{0i}}, i = 1,2,3$$

$$\omega_{pj} = \frac{g_{0j}}{C_{0j}}, j = 1,2$$

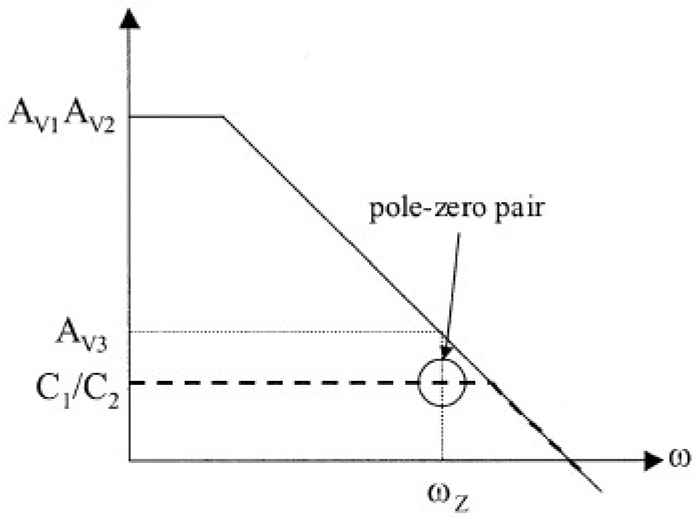
$$H(s) = -\frac{A_{v1}A_{v2} + A_{v3}\left(1+\frac{s}{\omega_{p1}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} = -\left(A_{v1}A_{v2} + A_{v3}\right)\frac{1+\frac{A_{v3}s}{\left(A_{v1}A_{v2}+A_{v3}\right)\omega_{p1}}}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$$

✓The OTA transfer function has two poles and a LHP zero created by the feedforward path. The location of the LHP zero is

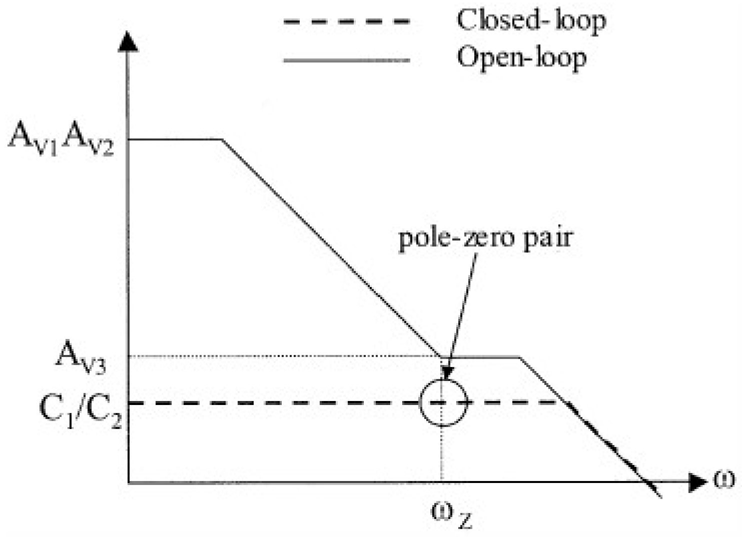
$$z_1 = -\left(1+\frac{A_{v1}A_{v2}}{A_{v3}}\right)\omega_{p1} \approx -\frac{g_{m1}}{C_{01}}\frac{g_{m2}}{g_{m3}}$$

✓The second and feedforward stages can be designed such that the negative phase shift due to ω_{p2} is compensated by the positive phase shift of the LHP zero
When the frequency of ω_{p2} exactly coincides with that of the LHP zero, the amplifier phase margin is 90 and the unity-gain frequency is given by

$$GB \approx \left(A_{v1}A_{v2} + A_{v3} \right) \approx A_{v1}A_{v2}\omega_{p1}$$



(a) Perfect pole–zero cancellation



(b) Pole–zero mismatch

✓This compensation scheme results in an amplifier with high gain and fast response
✓The bandwidth improvement is due to the fact that the poles are not split, as is the case in any amplifier with Miller compensation

❑Two-Stage CMOS Unbuffered Op Amp-Design

Relationships for the Two-Stage Op Amp:

•Slew rate *SR =I5/Cc(Assuming I7 >>I5 and CL > Cc)*

•First-stage gain

$$A_{v1} = -\frac{g_{m1}}{g_{ds2} + g_{ds4}} = -\frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$$

•Second-stage gain

$$A_{v2} = -\frac{g_{m6}}{g_{ds6} + g_{ds7}} = -\frac{2g_{m6}}{I_5(\lambda_6 + \lambda_7)}$$

Gain bandwidth

$$GB = g_{m1} / C_c$$

•Output pole

$$p_2 = -g_{m6} / C_L$$

•RHP zero

$$z_1 = g_{m6} / C_c$$

•Positive ICM

$$V_{in\max} = V_{DD} - |V_{T03}|_{\max} + V_{T1\min} - \sqrt{I_5 / \beta_3}, \beta_3 = \mu_p C_{ox}(W/L)_3$$

•Negative ICM

$$V_{in\min} = V_{SS} + V_{DS5sat} + V_{T1\max} + \sqrt{I_5 / \beta_1}, \beta_1 = \mu_n C_{ox}(W/L)_1$$

•60° phase margin requires that $C_c > 0.22C_L$

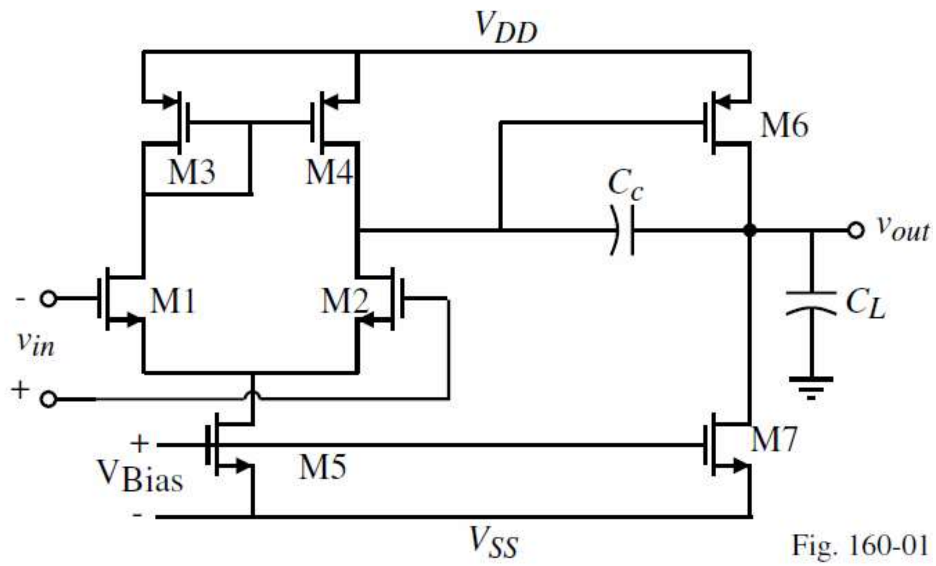
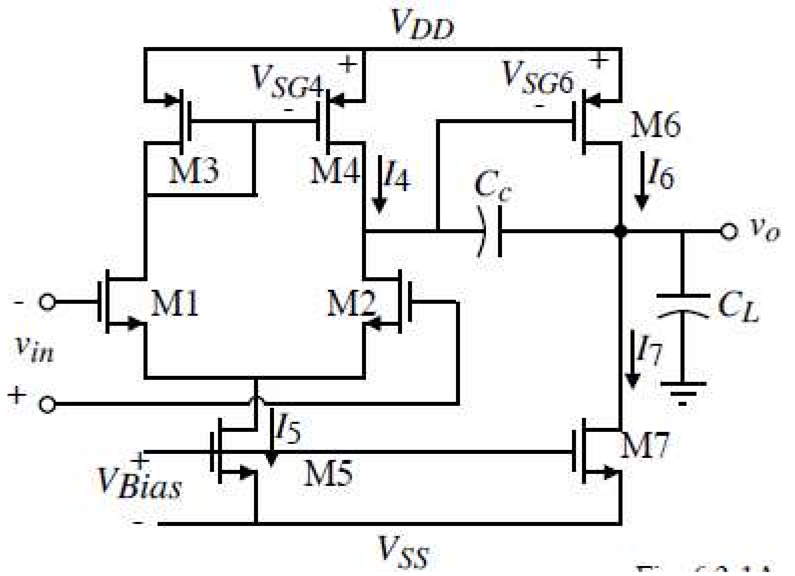


Fig. 160-01

DC Balance Conditions for the Two-Stage Op Amp

•For best performance, keep all transistors in saturation.

•M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages. Therefore, we develop conditions to force M4 to be in saturation.



1. First *assume that* $V_{SG4} = V_{SG6}$. *This will* cause "proper mirroring" in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is "guaranteed" to be in saturation.
2. *If VSG4 = VSG6, then*

$$I_6 = (S_6 / S_4) I_4$$

3. *However,*

$$I_7 = (S_7 / S_5) I_5$$

4. For balance, *I6 must equal I7*

$$(S_6 / S_4) = 2(S_7 / S_5) \quad \text{"balance conditions"}$$

5. So if the balance conditions are satisfied, then *VDG4 = 0 and M4 is saturated*

Op Amp Specifications:

The following design procedure assumes that specifications for the following parameters are given

1. Gain at dc, *Av(0)*
2. Gain-bandwidth, *GB*
3. Phase margin (or settling time)
4. Input common-mode range, ICMR
5. Load Capacitance, *CL*
6. Slew-rate, *SR*
7. Output voltage swing
8. Power dissipation, *Pdiss*

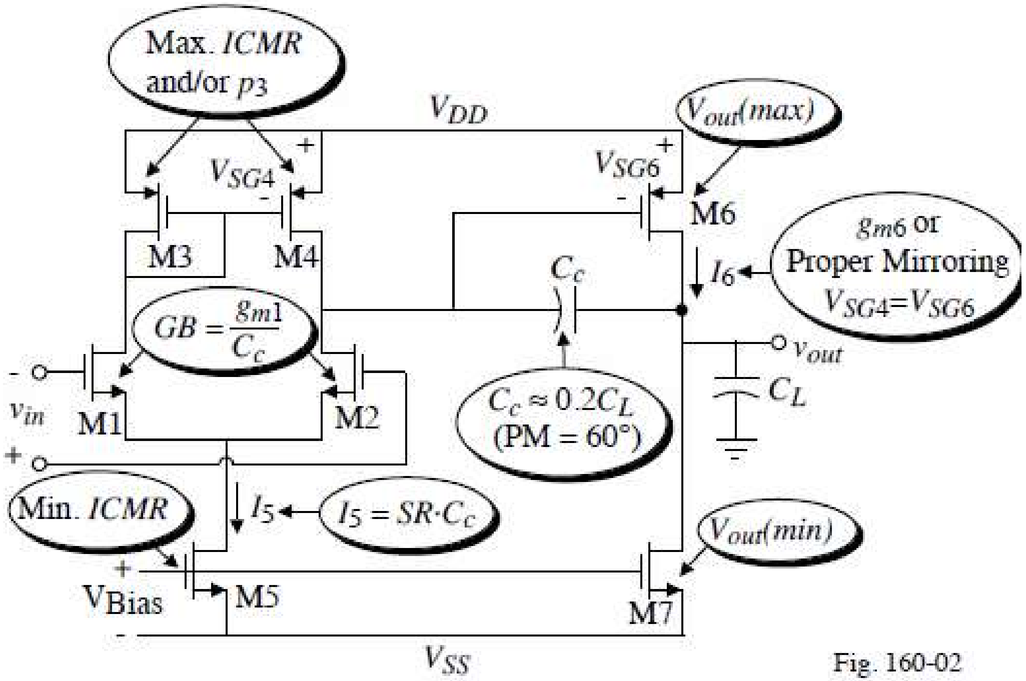


Fig. 160-02

Unbuffered Op Amp Design Procedure:

1. From the desired phase margin, choose the minimum value for *Cc, i.e. for a 60° phase* margin we use the following relationship. This assumes that *z ≥ 10GB.*

$$C_c > 0.22C_L$$

2. Determine the minimum value for the “tail current” (*I5)*

$$I_5 = SR \cdot C_c$$

3. Design for *S3* from the maximum input CM voltage specification.

$$S_3 = (W/L)_3 = \frac{I_5}{k_{pp}\left(V_{DD} - V_{in\max} - |V_{T03}|_{\max} + V_{T1\min}\right)^2}, k_{pp} = \mu_p C_{ox}$$

4. Verify that the pole of M_3 due to C_{gs3} *and* C_{gs4} *(= 0.67$W_3L_3C_{ox}$) will not be dominant* by assuming it to be greater than 10 *GB*

$$\frac{g_{m3}}{2C_{gs3}} > 10GB$$

5. Design for S_1 (S_2) to achieve the desired GB

$$g_{m1} = GB \cdot C_c \Rightarrow S_{1,2} = \frac{g_{m1}^2}{k_{pn} I_5}, k_{pn} = \mu_n C_{ox}$$

6. Design for S_5 from the minimum input voltage. First calculate $V_{DS5(sat)}$ then find S_5.

$$V_{DS5sat} = V_{in\min} - V_{SS} - V_{T1\max} - \sqrt{I_5 / \beta_1} \geq 100 \text{ mV} \Rightarrow \text{S}_5 = \frac{2I_5}{k_{pn} V_{DS5sat}^2}$$

7. Find S_6 by letting the second pole (p_2) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$

$$g_{m6} = 2.2 g_{m2} \frac{C_L}{C_c}, \frac{g_{m6}}{g_{m4}} = \frac{\sqrt{S_6 I_6}}{\sqrt{S_4 I_4}} = \frac{S_6}{S_4} \Rightarrow S_6 = S_4 \frac{g_{m6}}{g_{m4}}$$

8. Calculate I_6 from

$$I_6 = \frac{g_{m6}^2}{2k_{pp} S_6}$$

Check to make sure that S_6 satisfies the $V_{out(max)}$ requirement and adjust as necessary.

9. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$$S_7 = \left(I_7 / I_5\right) S_5$$

Check the minimum output voltage requirements.

10. Check gain and power dissipation specifications

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2+\lambda_4)I_6(\lambda_6+\lambda_7)} \qquad P_{diss} = (V_{DD}+|V_{SS}|)(I_5+I_6)$$

11. If the gain specification is not met, then the currents, I5 and I6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied.
    If the power dissipation is too high, then one can only reduce the currents I5 and I6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.
12. Simulate the circuit to check to see that all specifications are met.

❖DESIGN EXAMPLE OF A TWO-STAGE OP AMP

If $K_{n'}$=120μA/V^2, $K_{p'}$= 25μA/V^2, V_{TN} = $|V_{TP}|$ = 0.5V, λ_n = 0.06 V^{-1}, and λ_p = 0.08 V^{-1}, design a two-stage, CMOS op amp that meets the following specifications: *Av > 3000*, V_{DD} =2.5V GB = 5MHz, SR > 10V/μs, 60° phase margin 0.5V<$V_{out\ range}$<2V, I_{CMR} = 1.25V to 2V, P_{diss} ≤ 2mW. Assume the channel length is to be 0.5μm and the load capacitor is C_L = 10pF.

1) The first step is to calculate the minimum value of the compensation capacitor C_c,

$$C_c > 0.22C_L = 2.2\text{pF}$$

2) Choose C_c *as 3pF.* Using the slew-rate specification and C_c calculate I_5.

$$I_5 = SR \cdot C_c = 22\ \mu\text{A} \Rightarrow I_5 = 30\ \mu\text{A}$$

3) Next calculate (*W/L)3 using ICMR requirements (use worst case thresholds ±0.15V).*

$$S_3 = (W/L)_3 = \frac{I_5}{k_{pp}\left(V_{DD} - V_{in\max} - \left|V_{T03}\right|_{\max} + V_{T1\min}\right)^2} = 30$$

$$(W/L)_3 = (W/L)_4$$

4) Now we can check the value of the mirror pole, *p3, to make sure that it is in fact* greater than 10*GB. Assume the Cox = 6fF/μm2. The mirror pole can be found as*

$$\left|p_3\right| = \frac{g_{m3}}{2\pi \cdot 2C_{gs3}} = \frac{1.25 \cdot 10^9}{2\pi} \text{ grad/s} = 199\text{MHz} > 10GB = 50\text{MHz}$$

5) The next step in the design is to calculate *gm1 to get*

$$g_{m1} = GB \cdot C_c = 94.25\ \mu\text{S} \Rightarrow S_{1,2} = \frac{g_{m1}^2}{k_{pn} I_5} = 2.47 \Rightarrow \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 3$$

6) Next calculate *VDS5,*

$$V_{DS5sat} = V_{in\min} - V_{SS} - V_{T1\max} - \sqrt{I_5/\beta_1} = 0.31\text{V} > 100\text{ mV} \Rightarrow \text{S}_5 = \frac{2I_5}{k_{pn} V_{DS5sat}^2} = 5.16 \Rightarrow \left(\frac{W}{L}\right)_5 = 6$$

7) For 60° phase margin, we know that

$$g_{m6} \geq 10 g_{m1} = 942.5\ \mu\text{S}$$

Assuming that *gm6 = 942.5μS and knowing that gm4 = 150μS, we calculate (W/L)6 as*

$$S_6 = S_4 \frac{g_{m6}}{g_{m4}} = 188.5 \Rightarrow \left(\frac{W}{L}\right)_6 = 190$$

8) Calculate *I6 using the small-signal gm expression:*

$$I_6 = \frac{g_{m6}^2}{2k_{pp}S_6} = 94.2\ \mu\text{A} \approx 95\ \mu\text{A}$$

Calculating (*W/L)6 based on Vout(max), gives a value of 15. Since 190 exceeds the* specification and gives better phase margin, we choose (*W/L)6 = 190 and I6 = 95µA.*
With *I6 = 95µA the power dissipation is*

$$P_{diss} = \left(V_{DD} + |V_{SS}|\right)\left(I_5 + I_6\right) = 2.5\left(30 + 95\right)\ \mu\text{W} = 312.5\ \mu\text{W}$$

9) Finally, calculate (*W/L)7*

$$S_7 = \left(I_7 / I_5\right) S_5 = 19 \Rightarrow \left(W / L\right)_7 = 20$$

Let us check the *Vout(min) specification although the W/L of M7 is so large that this is* probably not necessary. The value of *Vout(min) is*

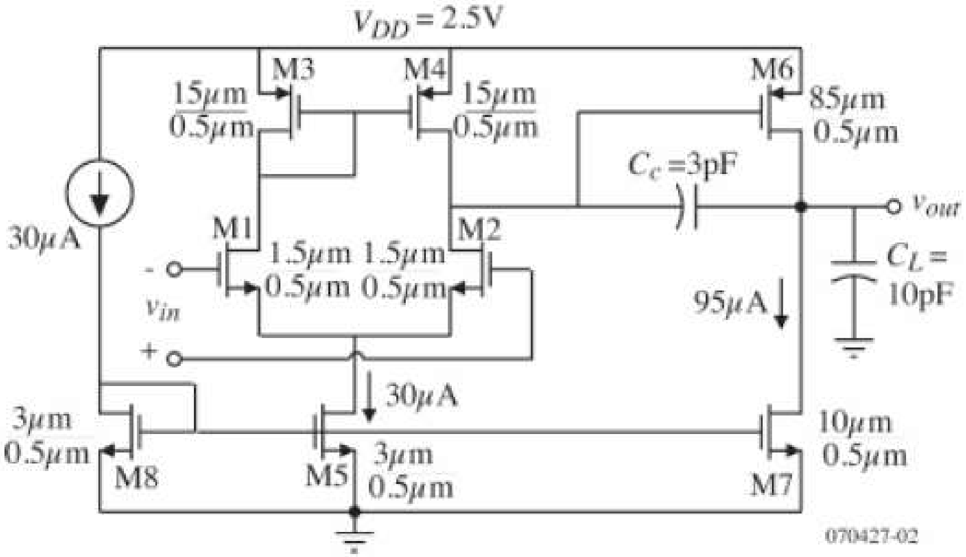
$$v_{OUT\,\min} = V_{DSsat7} = \sqrt{\frac{2I_{D7}}{\mu_n C_{ox} W / L}} = 281\ \text{mV}$$

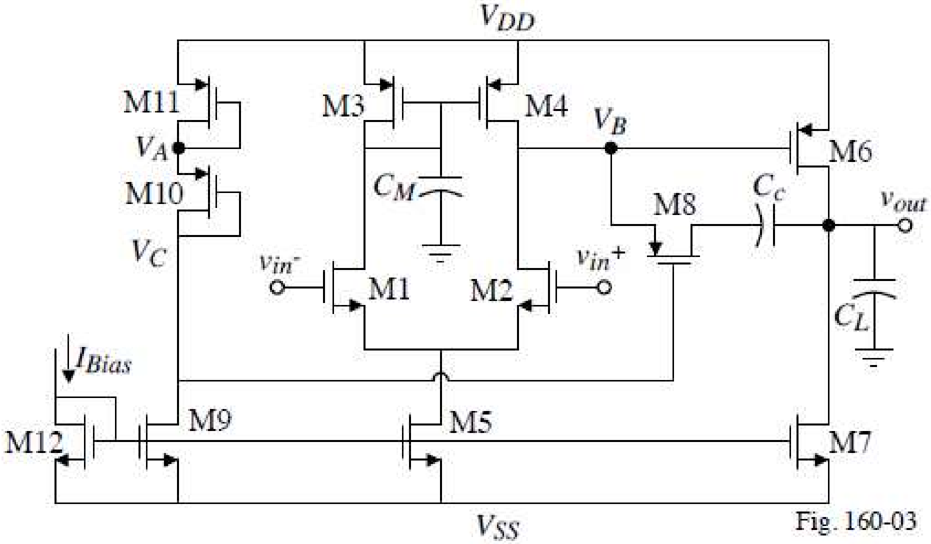
which is less than required.
At this point, the first-cut design is complete.
10) Now check to see that the gain specification has been met

$$A_{v0} = \frac{2g_{m1}}{I_5\left(\lambda_2 + \lambda_4\right)} \frac{2g_{m6}}{I_6\left(\lambda_6 + \lambda_7\right)} = 3180$$

which barely exceeds the specifications. Since we are at 2x*Lmin, it won't do any good to* increase the channel lengths. Decreasing the currents or increasing *W6/L6 will help.*

•The figure below shows the results of the first-cut design. The W/L ratios shown do not account for the lateral diffusion discussed above. The next phase requires simulation.





➢Incorporating the Nulling Resistor into the Miller Compensated Two-Stage Op Amp

•Design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole *p2*

•The task at hand is the design of transistors M8, M9, M10, M11, and bias current *I10. The first step in this design is to establish the bias components. In order to set VA* equal to *VB, then VSG11 must equal VSG6*

$$S_{11} = (I_{11} / I_6) S_6$$

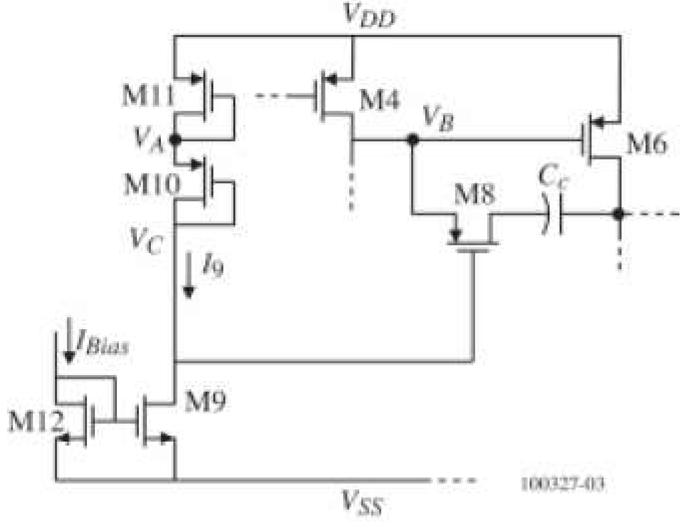
•Choose *I11 = I10 = I9 = 15μA which gives*

$$S_{11} = (I_{11} / I_6) S_6 = (15/95)190 = 30$$

•The aspect ratio of M10 is essentially a free parameter, and will be set equal to 1. There must be sufficient supply voltage to support the sum of *VSG11, VSG10, and VDS9.*

•*The ratio of I10/I5 determines the* (*W/L*) *of M9. This ratio is*

$$(W/L)_9 = (I_{10}/I_5)(W/L)_5 = (15/30)6 = 3$$



•Now (*W/L)8 is determined to be*

$$R_z = \frac{C_c + C_L}{C_c}\frac{1}{\sqrt{2I_{D6}\mu_p C_{ox}(W/L)_6}} = \frac{1}{(W/L)_8}\sqrt{\frac{(W/L)_{10}}{2\mu_p C_{ox} I_{D10}}}$$

$$\Rightarrow (W/L)_8 = \frac{C_c}{C_c + C_L}\sqrt{(W/L)_{10}(W/L)_6\frac{I_{D6}}{I_{D10}}} = \frac{3}{3+10}\sqrt{\frac{1\cdot 190\cdot 95}{15}} = 8$$

•It is worthwhile to check that the RHP zero has been moved on top of *p2. To do this, first* calculate the value of *Rz. VSG8 must first be determined. It is equal to VSG10, which is*

$$V_{SG10} = \sqrt{\frac{2I_{D10}}{\mu_p C_{ox} S_{10}}} + |V_{TP}| = \sqrt{\frac{2\cdot 15}{25\cdot 1}} + 0.5 = 1.6\ \text{V}$$

•Next determine *Rz*

$$R_z \approx \frac{1}{\mu_p C_{ox} S_8 (V_{SG10} - |V_{TP}|)} = 4.56\ \text{k}\Omega$$

•The location of *z1 is calculated as*

$$z_1 = \frac{1}{C_c\left(\frac{1}{g_{m6}} - R_z\right)} = -94.91\,\text{Mrad/s}$$

•The output pole, *p2, is*

$$p_2 \approx -\frac{g_{m6}}{C_L} = -95\ \text{Mrad/s}$$

✓Thus, we see that for all practical purposes, the output pole is canceled by the zero that has been moved from the RHP to the LHP.

✓The results of this design are summarized below where $L = 0.5\mu m$, $W_8 = 4\mu m$, $W_9 = 1.5\mu m$ $W_{10} = 0.5\mu m$ *and* $W_{11} = 15\ \mu m$

➢The Folded Cascode Op Amp

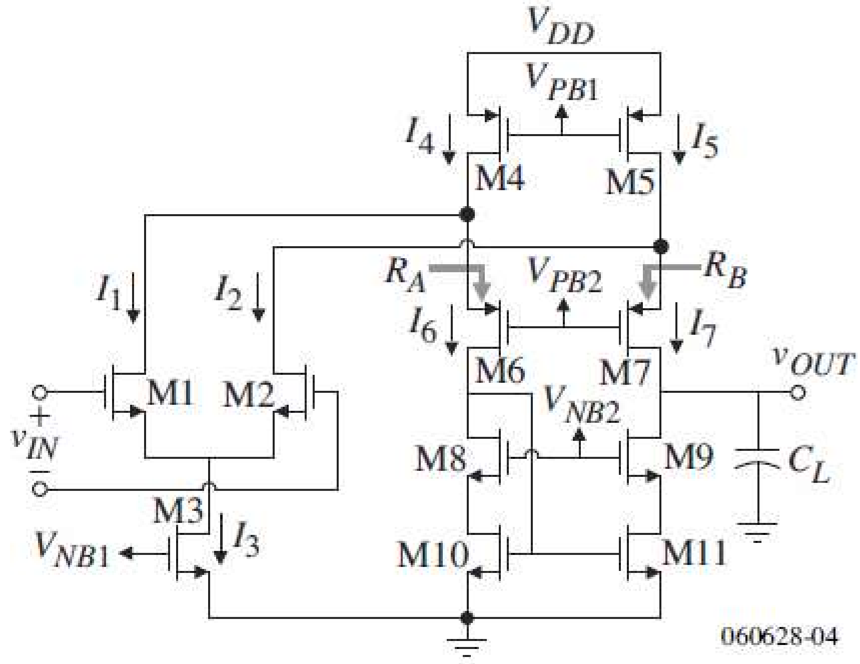
Comments:

• I_4 and I_5, should be designed so that I_6 and I7 never become zero (i.e. I_4=I_5=1.5I_3)

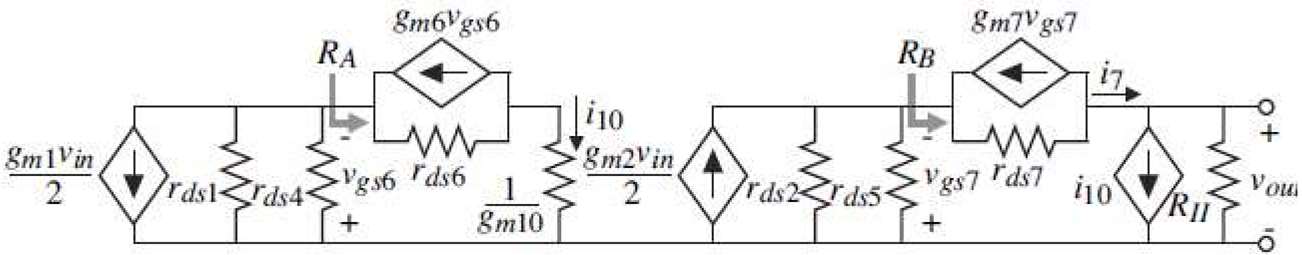
• This amplifier is nearly balanced (would be exactly if R_A was equal to R_B)

• Self compensating

• Poor noise performance, the gain occurs at the output so all intermediate transistors contribute to the noise along with the input transistors. (Some first stage gain can be achieved if R_A and R_B are greater than g_{m1} or g_{m2}.



❖Small-Signal Analysis of the Folded Cascode Op Amp



$$R_A = \frac{r_{ds6} + (1/g_{m10})}{1 + g_{m6} r_{ds6}} \approx \frac{1}{g_{m6}} \qquad R_B = \frac{r_{ds7} + R_{II}}{1 + g_{m7} r_{ds7}} \approx \frac{R_{II}}{g_{m7} r_{ds7}} = \frac{g_{m9} r_{ds9} r_{ds11}}{g_{m7} r_{ds7}} \approx r_{ds}$$

$$i_{10} = -\frac{g_{m1}V_{in}}{2}\frac{r_{ds1} \| r_{ds4}}{R_A + r_{ds1} \| r_{ds4}} \approx -\frac{g_{m1}V_{in}}{2}$$

$$i_7 = \frac{g_{m2}V_{in}}{2}\frac{r_{ds2} \| r_{ds5}}{R_B + r_{ds2} \| r_{ds5}} \approx \frac{g_{m2}V_{in}}{2}\frac{r_{ds2} \| r_{ds5}}{\frac{R_{II}}{g_{m7}r_{ds7}} + r_{ds2} \| r_{ds5}} = \frac{g_{m2}V_{in}}{2}\frac{1}{\frac{R_{II}\left(g_{ds2}+g_{ds5}\right)}{g_{m7}r_{ds7}}+1}$$

$$\Rightarrow i_7 = \frac{g_{m2}V_{in}}{2}\frac{1}{k+1}, k = \frac{R_{II}\left(g_{ds2}+g_{ds5}\right)}{g_{m7}r_{ds7}}$$

$$\frac{V_{out}}{V_{in}} = \left(i_7 + i_{10}\right)R_{out} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2}\frac{1}{k+1}\right) = \frac{1}{2}\frac{k+2}{k+1}g_{mI}R_{out}$$

$$R_{II} \approx g_{m9}r_{ds9}r_{ds11} \qquad R_{out} \approx g_{m9}r_{ds9}r_{ds11} \| g_{m7}r_{ds7}\left(r_{ds5} \| r_{ds2}\right)$$

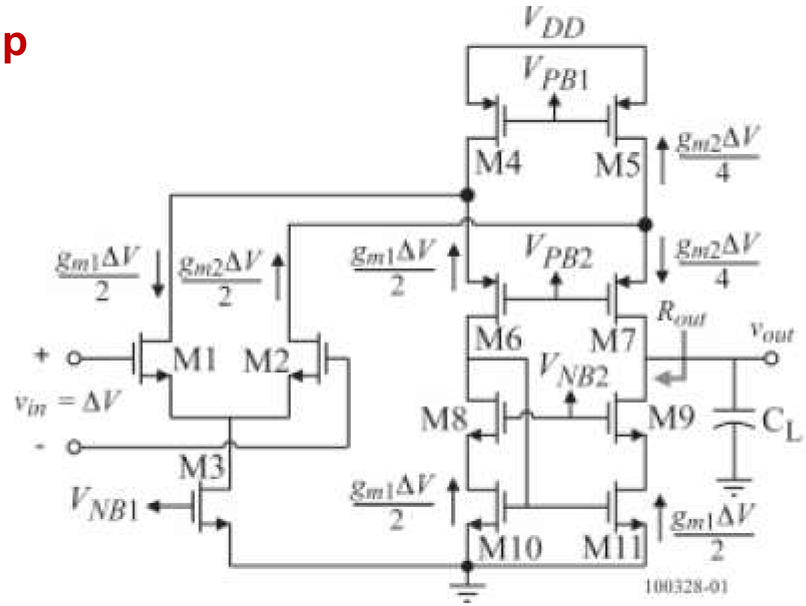
❖Intuitive Analysis of the Folded Cascode Op Amp

$$R_A \approx \frac{1}{g_{m6}} \qquad R_B \approx r_{ds}$$

$$i_{10} \approx -\frac{g_{m1}V_{in}}{2} \qquad i_7 \approx \frac{1}{2}\frac{g_{m2}V_{in}}{2} = \frac{g_{m2}V_{in}}{4}$$

$$\frac{V_{out}}{V_{in}} = \left(i_7 + i_{10}\right)R_{out} = \left(\frac{g_{m1}V_{in}}{2} + \frac{g_{m2}V_{in}}{4}\right)R_{out}$$

$$R_{out} \approx g_{m9}r_{ds9}^2 \| g_{m7}r_{ds7}^2 / 2 \approx g_m r_{ds}^2 / 3$$



❖Frequency Response of the Folded Cascode Op Amp

•The frequency response of the folded cascode op amp is determined primarily by the output pole which is given as

$$p_{out} = -\frac{1}{R_{out}C_{out}}$$

where C_{out} is all the capacitance connected from the output of the op amp to ground.
• All other poles must be greater than $GB = g_{m1}/C_{out}$. The approximate expressions for each pole is

1) Pole at node A:

$$p_A = -\frac{1}{R_A C_A} \approx -\frac{g_{m6}}{C_{gs6} + C_{db1} + C_{db4}}$$

2) Pole at node B:

$$p_B = -\frac{1}{R_B C_B} \approx -\frac{1}{\left(C_{gs7} + C_{db2} + C_{db5}\right)\left(r_{ds5} \,||\, r_{ds7} \,||\, r_{ds2}\right)}$$

3) Pole at drain of M_6:

$$p_6 = -\frac{1}{R_6 C_6} \approx -\frac{g_{m10}}{\left(C_{gs10} + C_{gs11} + C_{db8} + C_{db10}\right)}$$

4) Pole at source of M_8:

$$p_8 = -\frac{1}{R_8 C_8} \approx -\frac{g_{m8} r_{ds8} r_{ds10}}{\left(C_{gs8} + C_{db10}\right)}$$

5) Pole at source of M_9:

$$p_9 = -\frac{1}{R_9 C_9} \approx -\frac{g_{m9}}{\left(C_{gs9} + C_{db11}\right)}$$

•One might feel that because R_B is approximately $r_{ds}/3$ that this pole also might be small. However, at frequencies where this pole has influence, C_{out}, causes R_{out} to be much smaller making p_B also nondominant.

❖PSRR of the Folded Cascode Op Amp

•Consider the following circuit used to model the *PSRR-:*

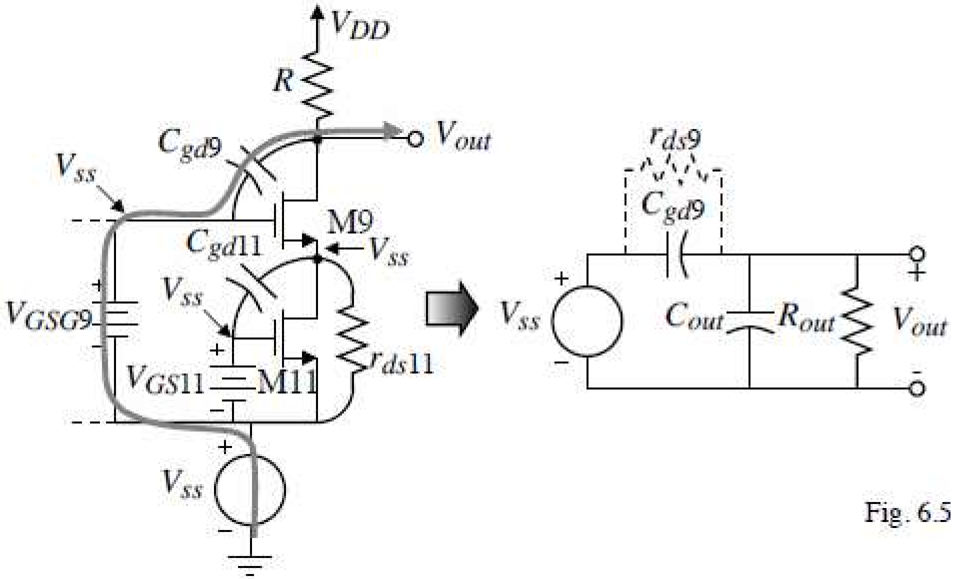


Fig. 6.5

•This model assumes that gate, source and drain of M_{11} and the gate and source of M_9 all vary with V_{SS}. We shall examine V_{out}/V_{ss} rather than *PSRR- (*Small V_{out}/V_{ss} will lead to large *PSRR-)*

•The transfer function of V_{out}/V_{ss} can be found as

$$\frac{V_{out}}{V_{ss}} \approx \frac{sc_{gd9}R_{out}}{1+sC_{out}R_{out}}, C_{gd9} < C_{out}$$

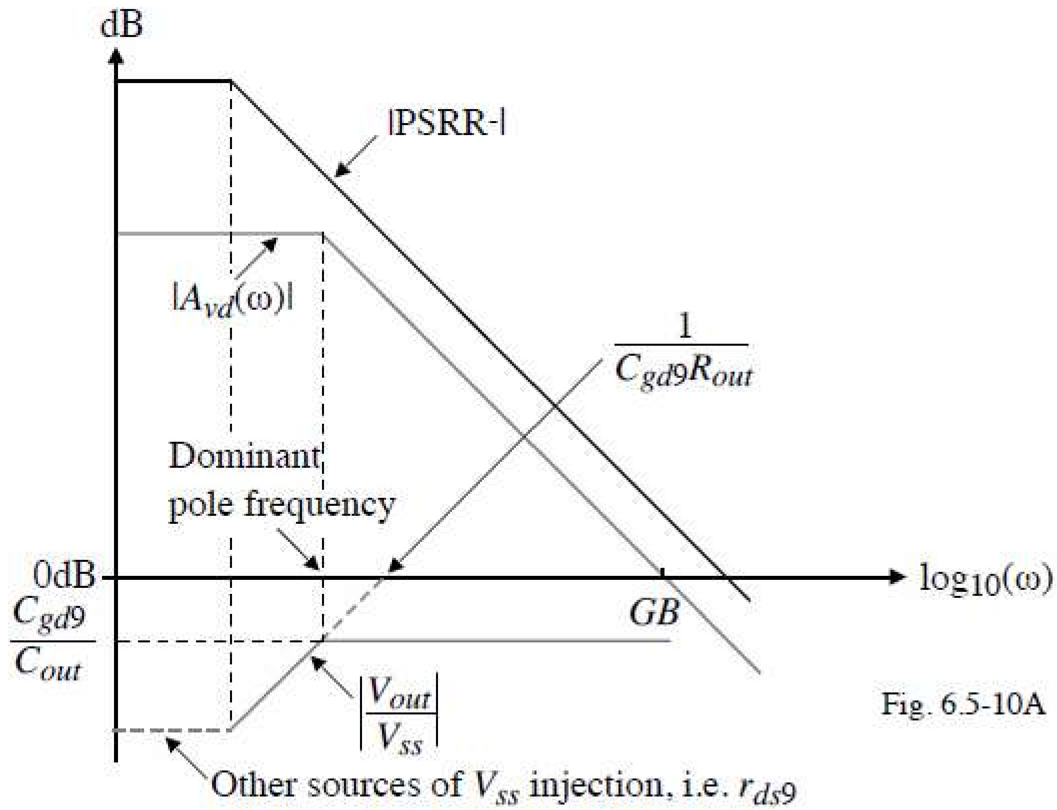


Fig. 6.5-10A

•The positive PSRR is similar to the negative PSRR. The ripple appears at the gates of M_4, M_5, M_6, M_7, M_{13}, and M_{14}. The primary source of injection is through the gate/drain capacitor of M_7, which is the same situation as for the negative power-supply injection.

•**The PSRR of the cascode op amp is much better than the two-stage op amp without any modifications to improve the PSRR!**

❖Design Approach for the Folded-Cascode Op Amp

Step #	Relationship/Requirement	Design equation/Constraint	Comments
1	SR	$I_3 = SR \cdot C_L$	
2	Bias current at output cascodes	$I_4 = I_5 = (1.2 - 1.5) I_3$	Avoid zero current in cascodes
3	V_{outmax}	$S_5 = \dfrac{2I_5}{k_{pp} V_{SD5}^2}, S_7 = \dfrac{2I_7}{k_{pp} V_{SD7}^2}, S_4 = S_5, S_6 = S_7$	$V_{SD5sat} = V_{SD7sat} = 0.5(V_{DD} - V_{out\max})$
4	V_{outmin}	$S_{11} = \dfrac{2I_{11}}{k_{pn} V_{DS11}^2}, S_9 = \dfrac{2I_9}{k_{pn} V_{DS9}^2}, S_{10} = S_{11}, S_8 = S_9$	$V_{DS9sat} = V_{DS11sat} = 0.5(V_{out\min} - V_{SS})$
5	$GB = g_{m1}/C_L$	$S_1 = S_2 = \dfrac{g_{m1}^2}{k_{pn} I_3} = \dfrac{(GB \cdot C_L)^2}{k_{pn} I_3}$	
6	Minimum input CM voltage	$S_3 = \dfrac{2I_3}{k_{pn}\left(V_{in\min} - V_{SS} - \sqrt{I_3 / (k_{pn} S_1)} - V_{T1}\right)^2}$	
7	Maximum input CM voltage	$S_4 = S_5 = \dfrac{2I_4}{k_{pp}(V_{DD} - V_{in\max} + V_{T1})^2}$	S4 and S5 must meet or exceed value in step 3
8	Differential voltage gain	$A_v = \left(\dfrac{g_{m1}}{2} + \dfrac{g_{m2}}{2}\dfrac{1}{k+1}\right) = \dfrac{1}{2}\dfrac{k+2}{k+1} g_{mI} R_{out}$	$k = \dfrac{R_{II}(g_{ds2} + g_{ds5})}{g_{m7} r_{ds7}}$
9	Power Dissipation	$P_{diss} = (V_{DD} + V_{SS})(I_3 + I_{11} + I_{10})$	

❖Design of a Folded-Cascode Op Amp

Design a folded-cascode op amp if the slew rate is 10V/μs, the load capacitor is 10pF, the maximum and minimum output voltages are 2V and 0.5V for a 2.5V power supply, the *GB is 10MHz,* the minimum input common mode voltage is *+1V* and the maximum input common mode voltage is 2.5V. The differential voltage gain should be greater than 3000 and the power dissipation should be less than 5mW. Use *Kpn'=120μA/V2, Kpp'= 25μA/V2, VTN = |VTP| = 0.5V, λn = 0.06(1/V), and λp = 0.08(1/V).* Let *L = 0.5 μm.*

Solution:

Following the approach outlined above we obtain the following results

$$I_3 = SR \cdot C_L = 100\ \mu\text{A}$$

Select $I_4 = I_5 = 125\mu A$.

Next, we see that the value of $0.5(V_{DD}\text{-}V_{out(max)})$ is *0.5V/2* or *0.25V.* Thus

$$S_4 = S_5 = \frac{2I_5}{k_{pp}V_{SD5}^2} = 160$$

and assuming worst case currents in M_6 and M_7 gives,

$$S_6 = S_7 = \frac{2I_7}{k_{pp}V_{SD7}^2} = 160$$

The value of $0.5^*V_{out(min)}$ is *0.25V* which gives the value of *S8, S9, S10* and *S11* as

$$S_{8-11} = \frac{2I_8}{k_{pp}V_{DS8}^2} = 20$$

In step 5, the value of GB gives S_1 and S_2 as

$$S_1 = S_2 = \frac{g_{m1}^2}{k_{pn} I_3} = \frac{\left(GB \cdot C_L\right)^2}{k_{pn} I_3} = 32.9 \approx 33$$

The minimum input common mode voltage defines S_3 as

$$S_3 = \frac{2I_3}{k_{pn}\left(V_{in\min} - V_{SS} - \sqrt{I_3 / \left(k_{pn} S_1\right)} - V_{T1}\right)^2} = 14.3 \approx 15$$

We need to check that the values of *S_4 and S_5* are large enough to satisfy the maximum input common mode voltage. The maximum input common mode voltage of 2.5V requires

$$S_4 = S_5 = \frac{2I_4}{k_{pp}\left(V_{DD} - V_{in\max} + V_{T1}\right)^2} = 40$$

which is less than 160. In fact, with *S4 = S5 = 160,* the maximum input common mode voltage is 2.75V.
The power dissipation is found to be

$$P_{diss} = \left(V_{DD} + V_{SS}\right)\left(I_3 + I_{11} + I_{10}\right) = 625\ \mu\text{W}$$

The small-signal voltage gain requires the following values to evaluate:

- $g_{m5}=g_{m4}=1000\mu S$, $g_{ds4}=g_{ds5}=10\mu S$
- $g_{m6}=g_{m7}=774.6\mu S$, $g_{ds6}=g_{ds7}=10\mu S$
- $g_{m(8\text{-}11)}= 600\mu S$, $g_{ds(8\text{-}11)}=4.5\mu S$
- $g_{m1}=g_{m2}=629\mu S$, $g_{ds1}=g_{ds2}=3\mu S$

Thus,

$R_{II} \approx g_{m9}r_{ds9}r_{ds11}$=29.63MΩ

$R_{out} \approx$7.44MΩ

$$k = \frac{R_{II}\left(g_{ds2}+g_{ds5}\right)}{g_{m7}r_{ds7}} = 0.75$$

The small-signal, differential-input, voltage gain is

$$A_v = \left(\frac{g_{m1}}{2}+\frac{g_{m2}}{2}\frac{1}{k+1}\right) = \frac{1}{2}\frac{k+2}{k+1}g_{mI}R_{out} = 3678$$

The gain is slightly larger than the specified 3000.

Comments on Folded Cascode Op Amps

•Good PSRR
• Good ICMR
• Self compensated
• Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
• Need first stage gain for good noise performance
• Widely used in telecommunication circuits where large dynamic range is required