# Rail-to-Rail OTA

❑ Rail-to-rail CMOS op amp

• Generally, rail-to-rail amplifiers are useful in low-voltage applications, where it is necessary to efficiently use the limited span offered by the power supply.

• While conventional amplifiers are capable of linear operation only for signals with a small excursion around the common-mode levels, rail-to-rail amplifiers are designed to allow signals to swing within millivolts of either power supply rail.

• The input and output voltage ranges are dependent on the amplifier topology, and the rail-to-rail operation can be achieved for either the input or the output, or both input and output
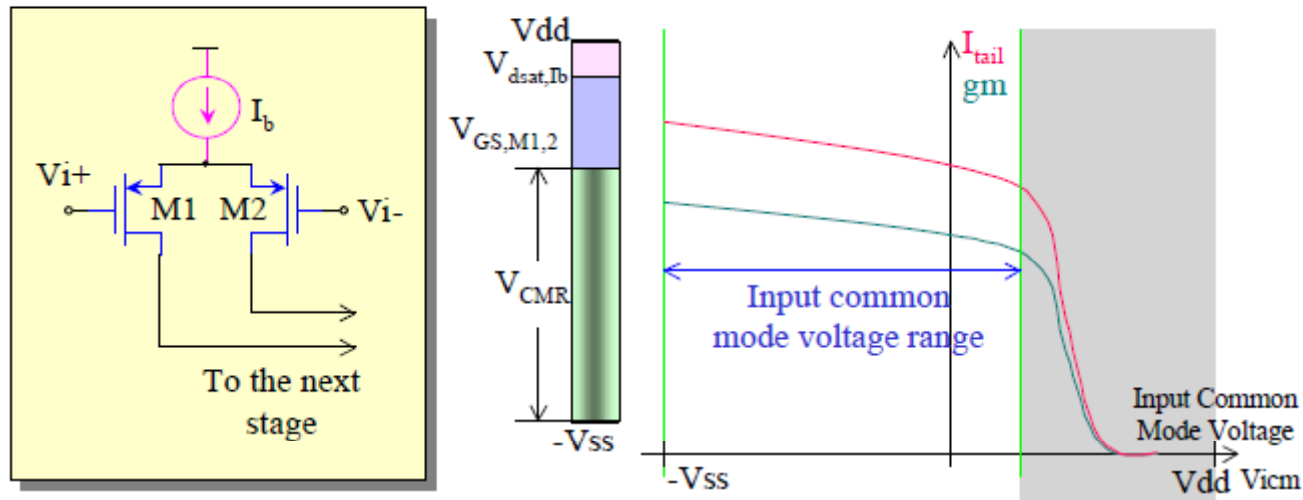
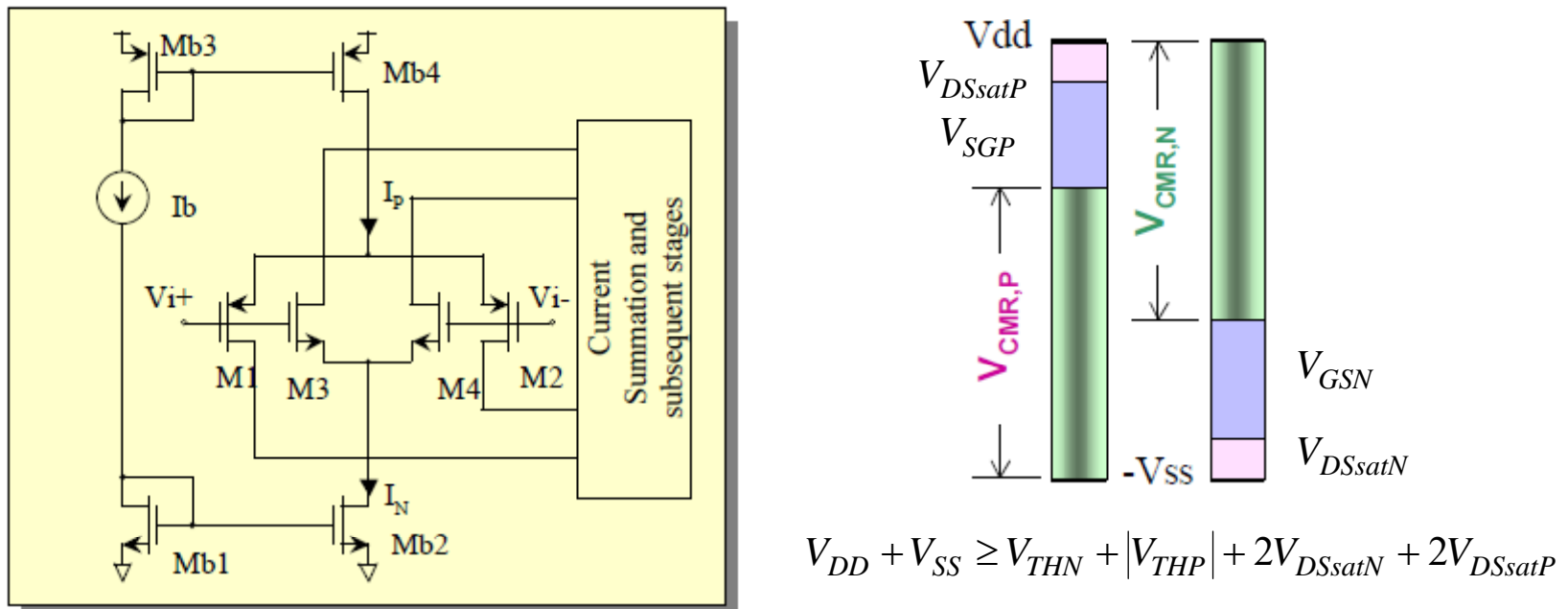➤ CMOS amplifier with rail-to-rail input

• NMOS differential pair
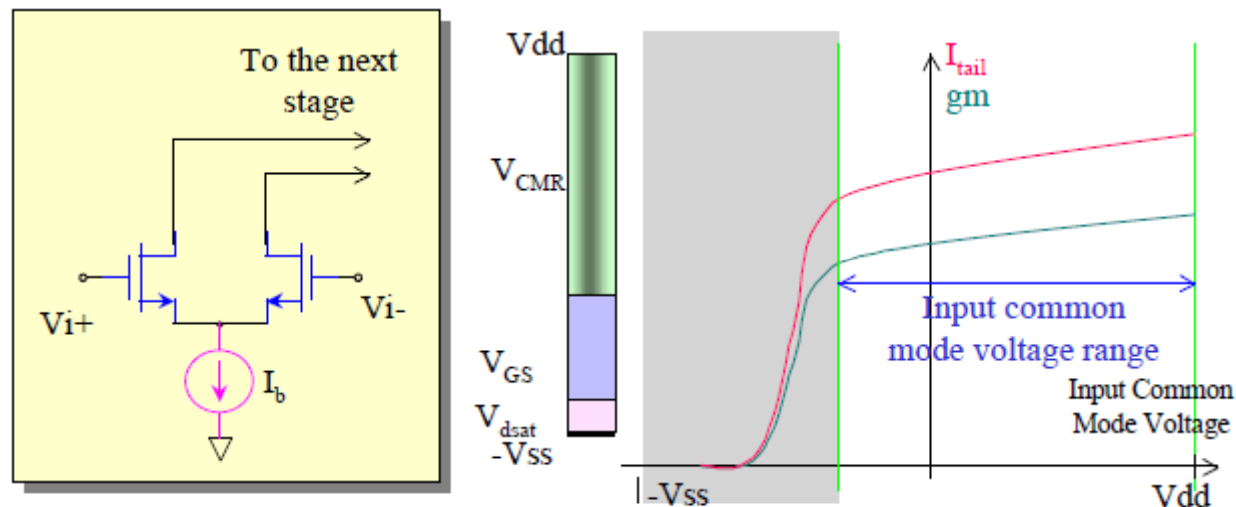
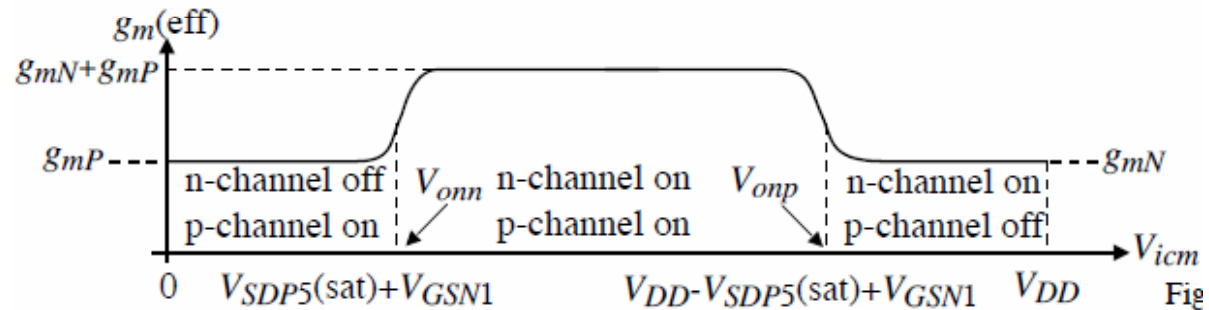Radivoje Đurić, 2015, Analogna Integrisana Kola

• PMOS differential pair

• PMOS+NMOS differential pair

$$V_{DD} + V_{SS} \geq V_{THN} + |V_{THP}| + 2V_{DSsatN} + 2V_{DSsatP}$$

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•Due to the different dc behavior of each pair, the resulting transconductance varies with the common-mode input voltage and is not constant.

•When the common-voltage, vCM, is at mid-rail, both n- and p-channel transistor stages operate normally, as a result, the total transconductance gmT, which is about two times greater than that obtained in the cases where vCM is close to either of the supply voltages, VSS or VDD, and only one pair type remains
operational.

•This transconductance variation can be efficiently reduced by using differential pairs based on improved biasing circuits
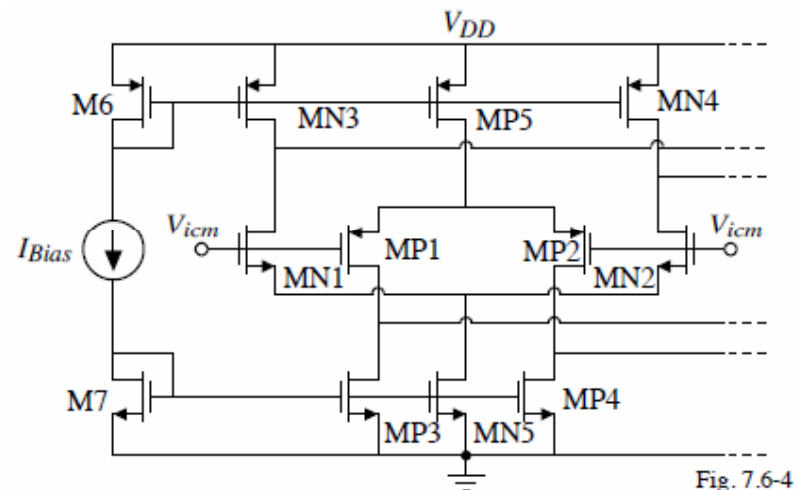

Folded cascode OTA:

Fig. 7.6-4

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Techniques for N-P Complementary Rail-to-Rail Input Stage

1. **For input stages with input transistors working in weak-inversion region, using current complementary circuit to keep the sum of In and Ip constant**

Basic idea:

• For CMOS transistors working in weak-inversion region

$$I_{Dwi} = \frac{W}{L} I_{D0} \exp(\frac{V_{GS}}{nKT/q}) \qquad g_{mwi} = \frac{W}{L} \frac{I_{D0}}{nKT/q} \exp(\frac{V_{GS}}{nKT/q}) = \frac{I_{Dwi}}{nKT/q} = k \cdot I_{Dwi}$$
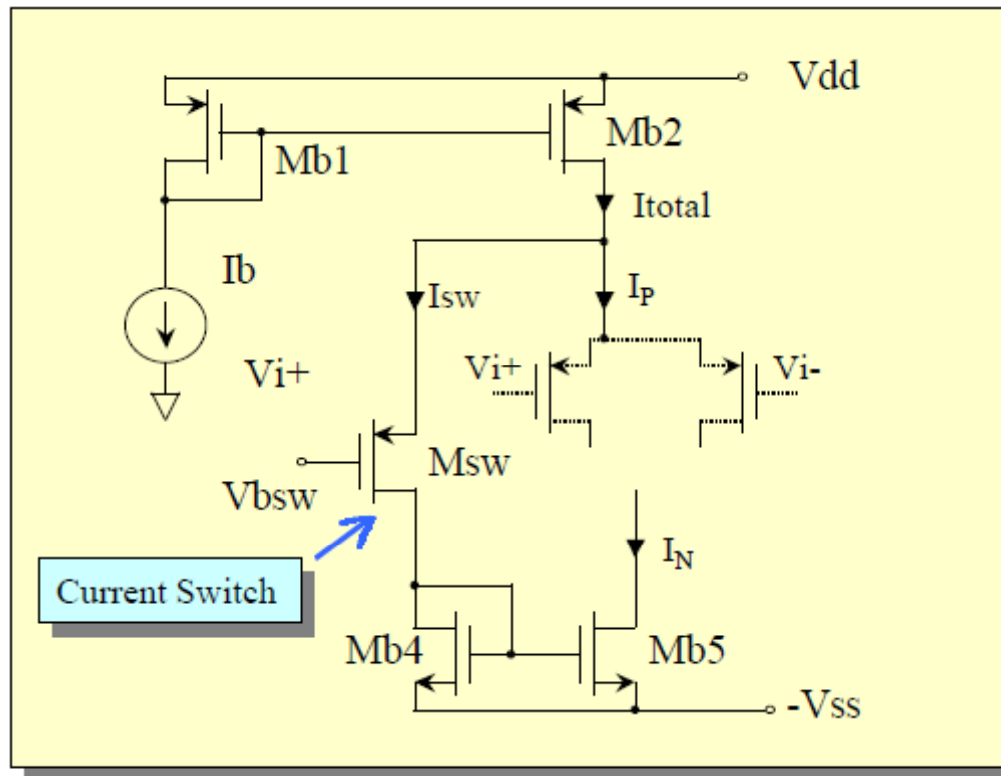

• So, the total transconductance of the input stage is

$$g_{mT} = g_{mN} + g_{mP} = k(I_N + I_P)$$

Thus the transconductance of the input stage is proportional to the sum of the tail currents of N and P pairs.

• Mb4 and Mb5 mirror the current through Msw, Isw, to provide the tail current of the N-channel input pair. Mb4 and Mb5 are with the same geometry.

• Mb2 always works in saturation region, and never to ohmic region, by properly selecting the gate biasing voltage Vbsw of Msw.

- Msw works as a current switch
  - ✓ When the input common mode voltage, Vicm, is close to Vdd, the P input pair cuts off, the drain current of Mb2, Itotal is diverted to Msw. And then mirrored through Mb4 and Mb5, to the source node of the N input pair.
  - ✓ When Vicm is close to -Vss, the switch Msw cuts off, Itotal then flows to the P input pair.
  - ✓ In between, part of Itail flows to P pair, and the rest to Msw, through current mirror Mb4 and Mb5, to the N pair.
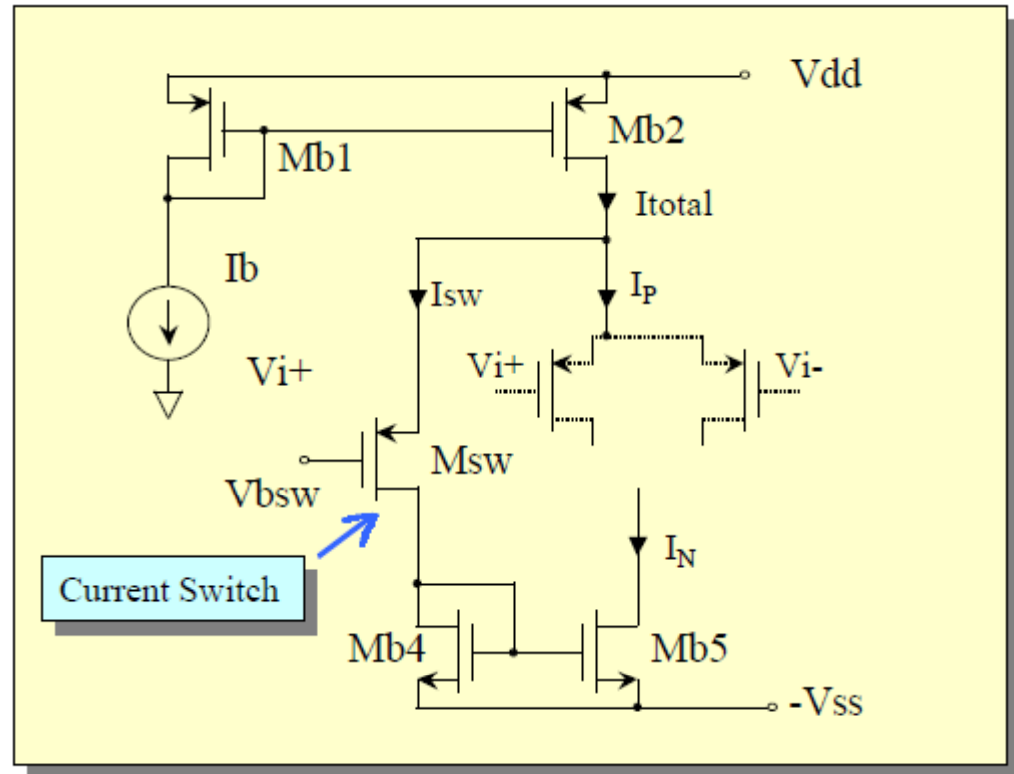
- Using a first order approximation, the following equation stands, $I_p + I_n = I_{tail} = const$

Weak Inversion

Strong Inversion

gm_N

gm_P

gm_{SUM}
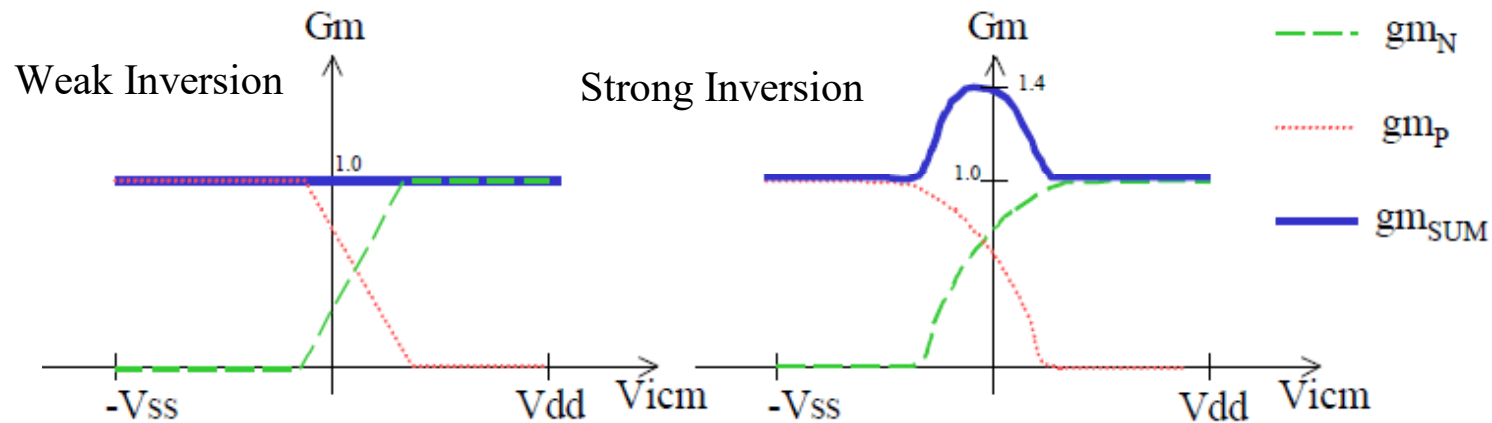
•The complete circuit
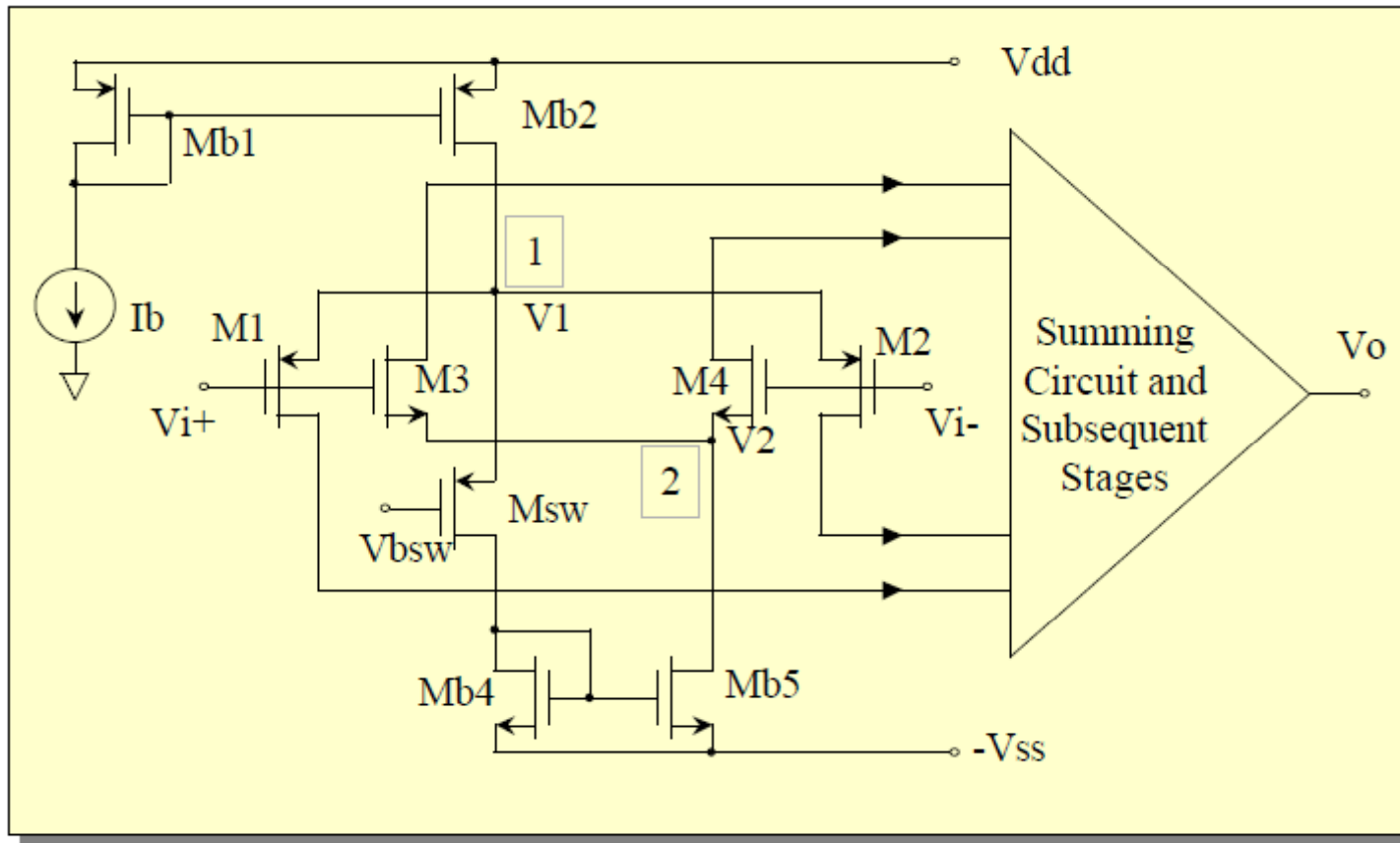
✓Rail-to-rail constant transconductance is only when the input pairs work in **weak inversion region**

✓If the input pairs are in **strong inversion region,** the transconductance will change by a factor of 1.4 (√2)

✓As working in weak inversion region is a requirement to get a rail-to-rail constant transconductance, this structure only applies to amplifiers with **low GBW.**

2. Using square root circuit to keep √Ip+ √In constant

Basic idea:

•For an input differential pair, using a 1st order approximation

$$gm = \sqrt{2K_P(W/L)I_D} = \sqrt{K_P(W/L)I_{TAIL}}$$

Where the I_{TAIL} is the tail current of the differential pair. We can change gm by altering the tail current of the differential pair!

•The total transconductance of the input stage is given by

$$gm_T = gm_N + gm_P = \sqrt{KP_N(W/L)_N I_N} + \sqrt{KP_P(W/L)_P I_P}$$

If $KP_N(W/L)_N = KP_P(W/L)_P = 2K$ $gm_T = gm_N + gm_P = \sqrt{2K}(\sqrt{I_N} + \sqrt{I_P})$

•To keep g_{mT} contant, we just need to keep √Ip+ √In constant

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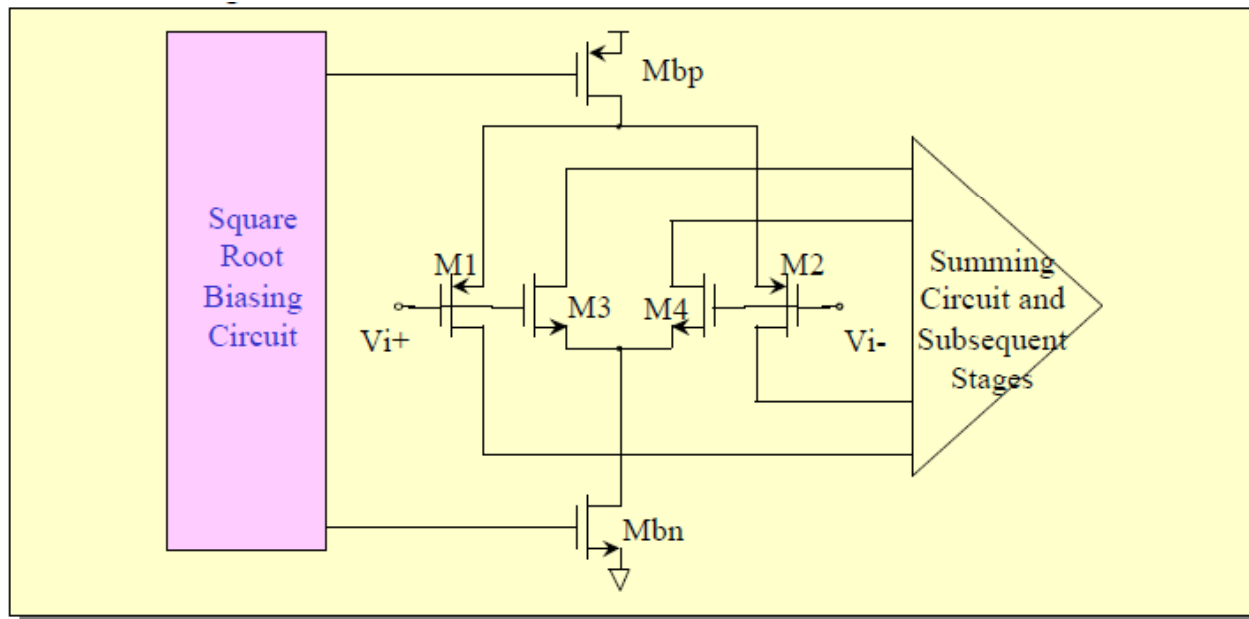
•We can utilize the square law characteristic of MOS transistors to implement the square root biasing circuit. The following is one implementation of the rail-to-rail input stage with square root biasing circuit.

Current Square Root Circuit
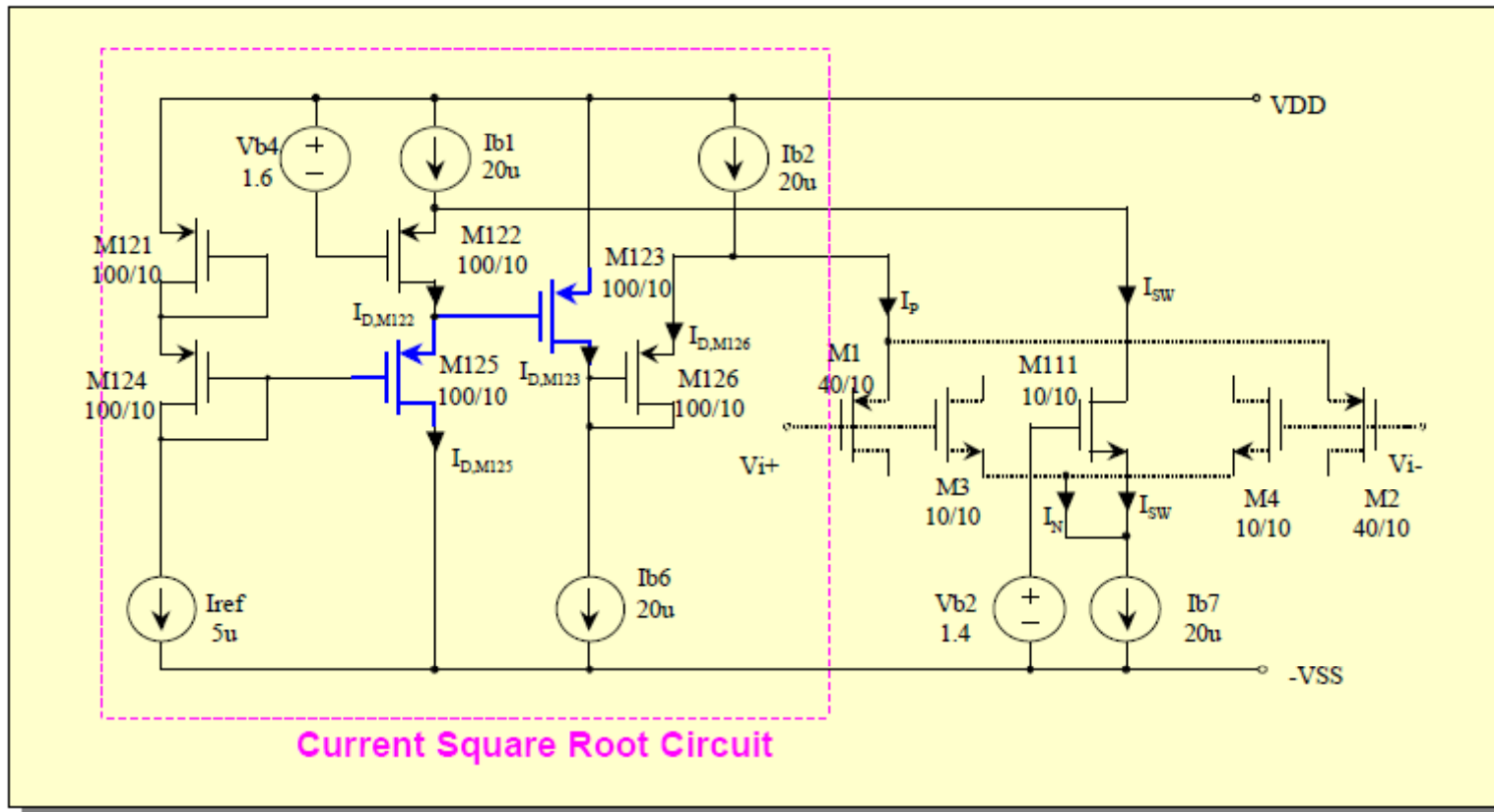
Analysis:

1. $V_{SG,M123} + V_{SG,M125} = V_{SG,M121} + V_{SG,M124} = const$,

$V_{SG} = \sqrt{\dfrac{2I_D}{KP_P(W/L)}} + |V_{TP}|$, as $(W/L)_{M125} = (W/L)_{M123} = (W/L)_{M125,123}$,

$$\sqrt{\frac{2I_{D,M123}}{KP_P(W/L)_{M123,125}}}+|V_{TP}|+\sqrt{\frac{2I_{D,M125}}{KP_P(W/L)_{M123,125}}}+|V_{TP}|=const$$

$$\sqrt{I_{D,M123}}+\sqrt{I_{D,M125}}=const_2$$

2. $I_N+I_{SW}=I_{b7}=I_b$, $I_{D,M122}+I_{SW}=I_{b1}=I_b$, and $I_{D,M122}=I_{D,M125}$ → $I_N=I_{D,M125}$

3. $I_{D,M123}+I_{D,M126}=I_{b6}=I_b$, $I_{D,M126}+I_P=I_{b2}=I_b$, → $I_P=I_{D,M123}$

From 1. to 3., we can obtain $\quad\sqrt{I_N}+\sqrt{I_P}=const_2$

If M121~M124 are with the same geometry, further calculation yields

$$\sqrt{I_N}+\sqrt{I_P}=2\sqrt{I_{D,M121,124}}=2\sqrt{I_{ref}}$$

Working Principle:
✓The input transistors work in strong inversion region
✓The square-root circuit M121-M125 keeps the sum of the square-roots of the tail currents of the input pairs and then the gm constant.
✓The current switch, M111, compares the common-mode input voltage with Vb3 and decides which part of the current Ib7 should be diverted to the square-root circuit.
✓In the common-mode input voltage range from Vdd to -Vss+1.8V only the N channel pair operates. The current switch M111 is off and thus the tail current of the N channel input pair IN equals Ib7=4Iref=20uA.
✓The sum of the gate-source voltages of M123 and M125 is equal to reference voltage which is realized by M121 and M124. Since the current through M125 equals IN and the current through M123 equals the tail current of the P channel input pair IP.

✓It can be calculated that the square-root of Ip is given by (M121-M125 matched)

$$\sqrt{I_P} = 2\sqrt{I_{ref}} - \sqrt{I_N}$$

✓In the common-mode input range from -Vss+1.2V to Vss only the P channel input pair operates. In this range the current Ib7=4Iref=20uA flows through the current switch to the square-root circuit. Thus, the current through M125 is nearly zero which means that its gate-source voltage is smaller than its threshold voltage.

✓If the current through M123 is larger than 4Iref=20uA, the current limiter M126 limits the current of M123 to 4Iref=20uA and directs it to the P channel input pair.

✓It can be calculated that the transconductance of the input stage, and therefore the unity-gain frequency, is constant within the rail-to-rail input common mode range. The gm is defined by

$$gm = 2\sqrt{2KIref} \quad \text{where} \quad K = \frac{1}{2}KP_N(\frac{W}{L})_N = \frac{1}{2}KP_P(\frac{W}{L})_P$$

✓The summing circuit adds the output signals of the complementary input stage, and forms the output voltage.

Discussion:

•The circuit is somewhat complex and the functionality relies on the square law of MOS transistors. For current sub-micron processes, the square law is not closely followed, which may introduce large error for the total transconductance.

3. Using current switches to change the tail current of input differential pairs

Basic idea

•We know that, by first order approximation, for a MOS transistor working in strong inversion and saturation region, square law applies, that is

$$I_D = K(V_{GS} - V_T)^2, \quad \text{and} \quad gm = 2\sqrt{KI_D}, \qquad K = \frac{1}{2}KP(\frac{W}{L})$$

•Suppose for the N and P input pairs,

$$KP_N(\frac{W}{L})_N = KP_P(\frac{W}{L})_P = 2K$$

and the tail currents of N and P pairs are equal, with the value of Itail

•When the input common mode voltage is in the mid-range, both of N and P pairs are conducting, so the total transconductance is

$$gm_T = gm_N + gm_P = 2\sqrt{2KI_{TAIL}}$$

•When the input common mode voltage is close to Vdd, the N pair operates. And when it is close to the -Vss, the P pair operates. In both cases, the total transconductance is only **half of that when both of N and P** pairs operate.

$$gm_T = gm_N = gm_P = \sqrt{2KI_{TAIL}}$$

•We can increase the tail current to **4 times of its original value to have the** same transconductance as that when both of N and P pairs operate.
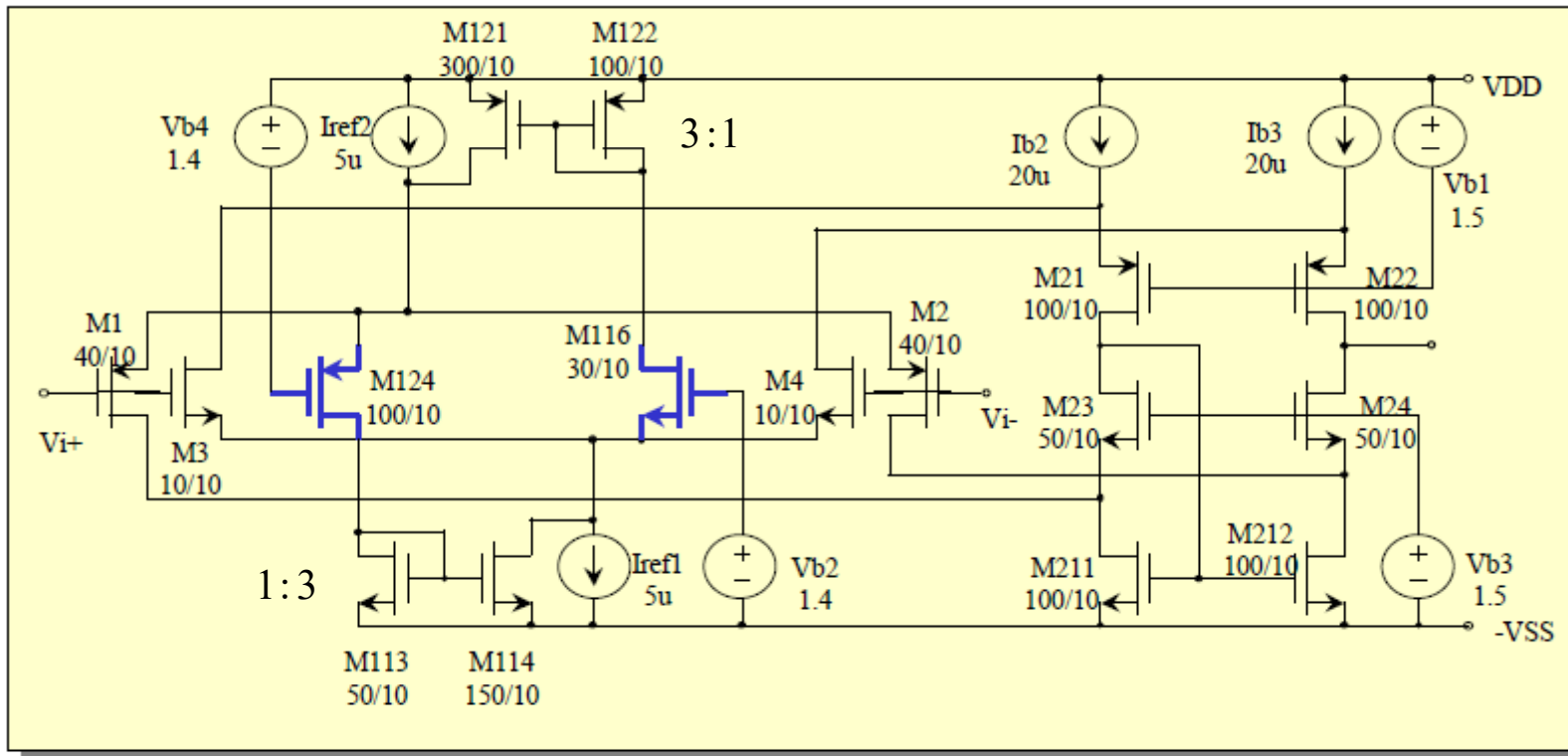
•Increase the bias current in the differential amplifier that is on when the other differential amplifier is off.

•Three regions of operation depending on the value of *Vicm:*

1) n-channel diff. amp. off and p-channel on

$$V_{icm} < V_{onn}, I_p = 4I_b$$

$$g_{meff} = \sqrt{k_p W_P / L_P}\, 2\sqrt{I_b}$$

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2) p-channel diff. amp. off and n-channel on

$$V_{icm} > V_{onp}, I_n = 4I_b$$

$$g_{meff} = \sqrt{k_n W_N / L_N}\, 2\sqrt{I_b}$$

3) p-channel diff. amp. on and n-channel on

$$V_{onp} < V_{icm} < V_{onn}, I_n = I_p = I_b$$

$$g_{meff} = \left(\sqrt{k_n W_N / L_N} + \sqrt{k_p W_P / L_P}\right)\sqrt{I_b}$$

$$g_{mn} = \sqrt{k_n W_N / L_N}\,\sqrt{I_b} = g_{mp} = \sqrt{k_p W_P / L_P}\,\sqrt{I_b} \Rightarrow$$

$$g_{meff} = \sqrt{k_n W_N / L_N}\, 2\sqrt{I_b}$$

$$k_p W_P / L_P = k_n W_N / L_N \Rightarrow$$

$$g_{meff} = 2g_m = g_{mn} + g_{mp} \neq f\left(V_{icm}\right)$$
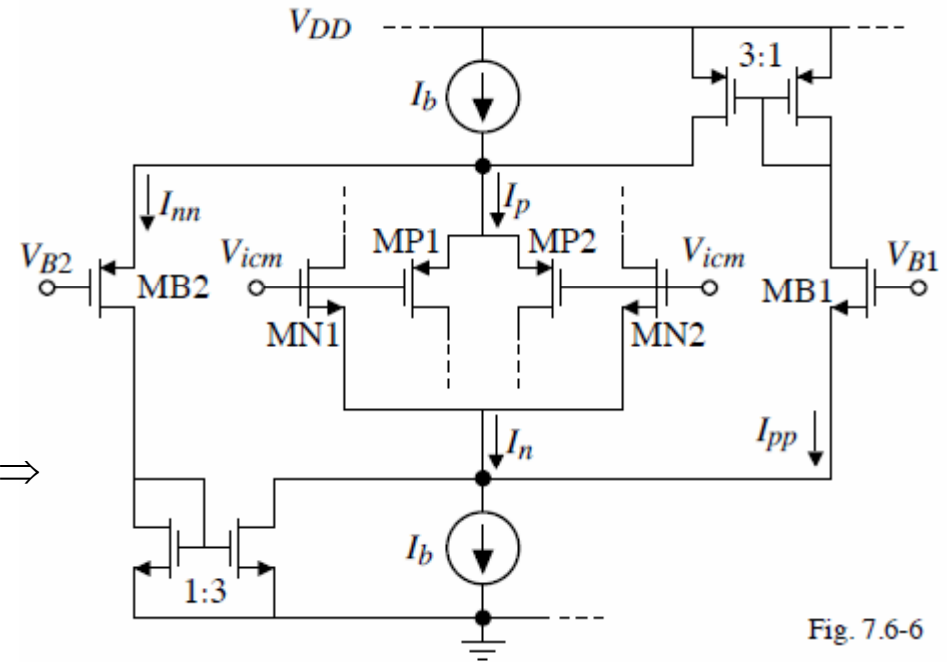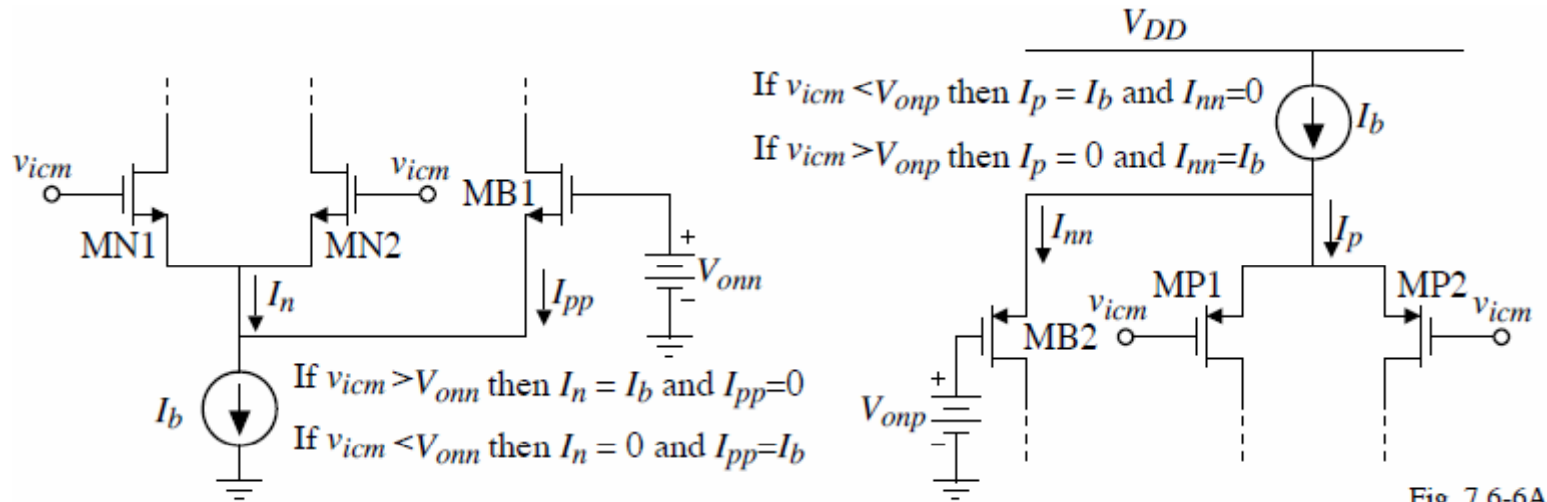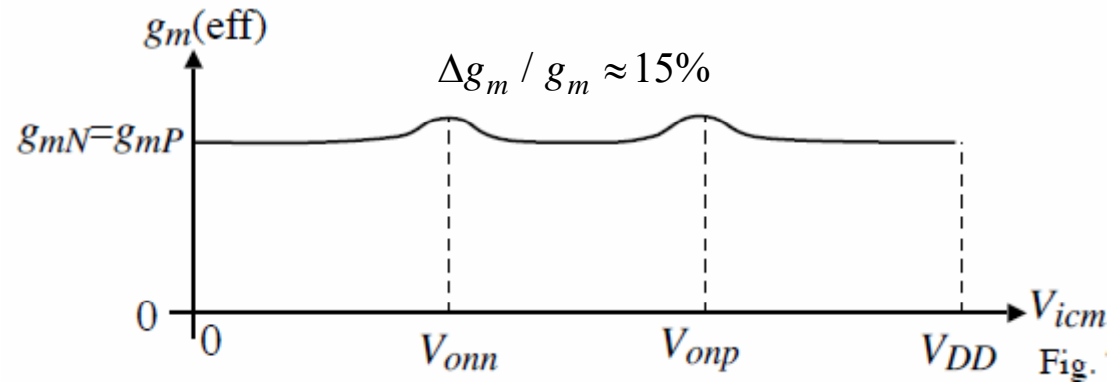

Fig. 7.6-6

If $v_{icm} < V_{onp}$ then $I_p = I_b$ and $I_{nn} = 0$

If $v_{icm} > V_{onp}$ then $I_p = 0$ and $I_{nn} = I_b$

If $v_{icm} > V_{onn}$ then $I_n = I_b$ and $I_{pp} = 0$

If $v_{icm} < V_{onn}$ then $I_n = 0$ and $I_{pp} = I_b$

Fig. 7.6-6A

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Result:

•If the common mode input voltage is between Vss+1.3V and Vss+1.5V, the M116 is partly conducting, and the rest of tail current flows through M3 and M4, which is assumed to be Ix here. So the tail current of the P pair is Iref+3(Iref-Ix).
•The total gm of the input stage is given by

$$gm_T = \sqrt{2K}\left(\sqrt{Ix} + \sqrt{Iref + 3(Iref - Ix)}\right)$$

•Calculate the maximum value of this equation, we can obtain that when Ix=(1/3)Iref, gmT has its maximum value. Which yields

$$gm_T = \sqrt{2KIref}\left(\sqrt{\frac{1}{3}} + \sqrt{3}\right) = 2.31\sqrt{2KIref} = 2\sqrt{2KIref}(1 + 15.5\%)$$

Which is about 15% larger than its nominal value $2\sqrt{2KIref}$.

R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing , A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries, IEEE Journal of Solid-State Circuits, vol. 29, pp. 1505 – 1513, Dec. 1994.

6.4 MHz / 10 pF

6.4 V/µs

31 nV/√ Hz

3.3 V
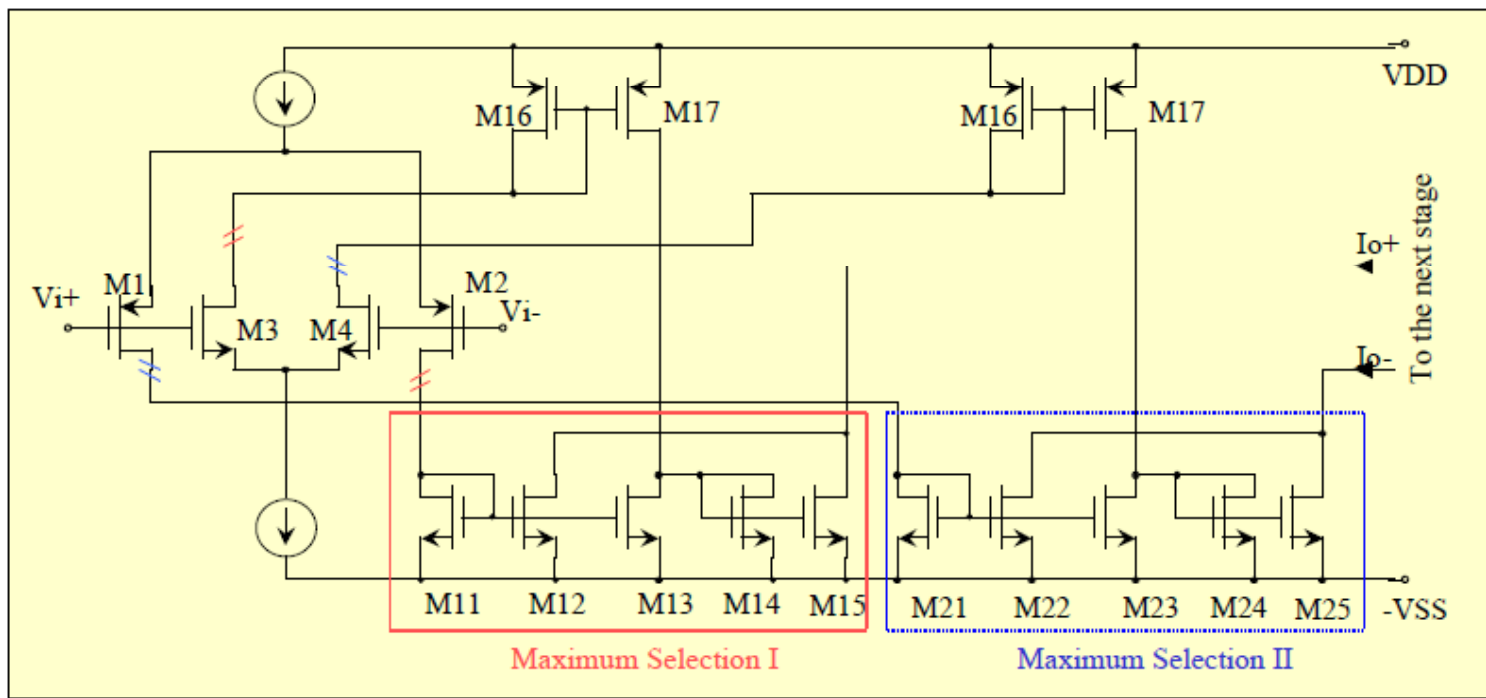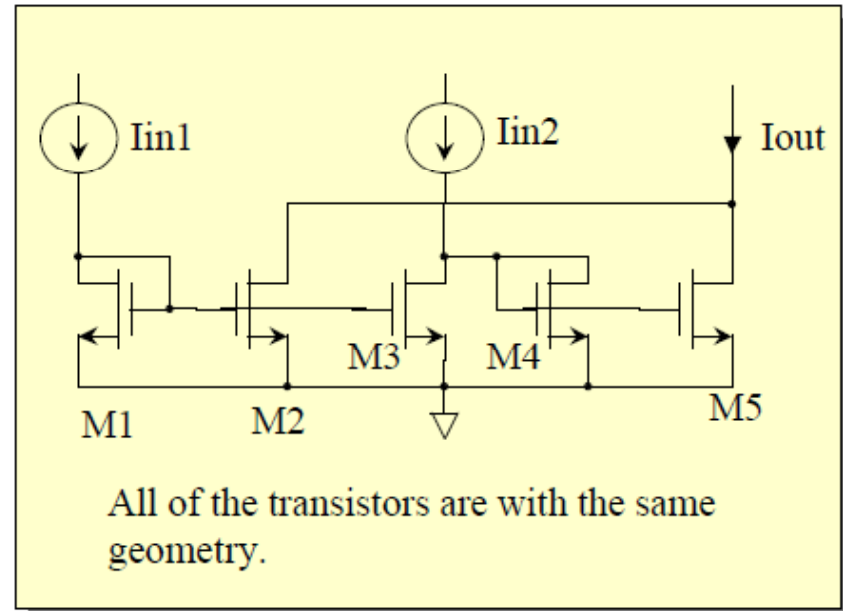0.18 mA
3 mApk
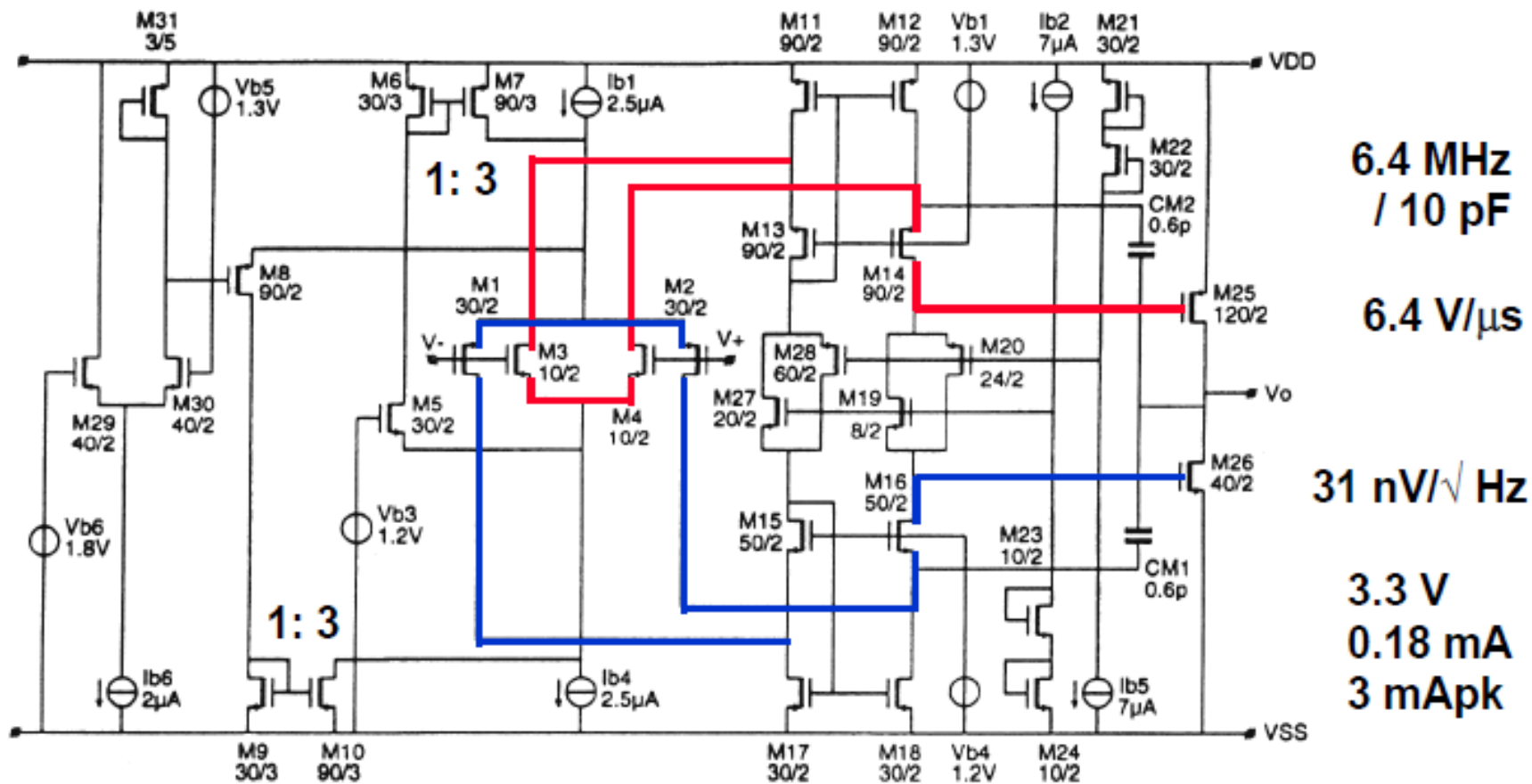
4. Using Maximum/Minimum selection circuit

The basic idea:

•From previous analysis, we know that, when the common mode voltage drives the tail current transistor out of saturation region, the tail current of a differential pair decreases dramatically with the common mode voltage.

•The differential pair, whichever it is N pair or P pair, with the larger current should be working properly. We just try to choose the pair with larger working current, and discard the output of another pair.


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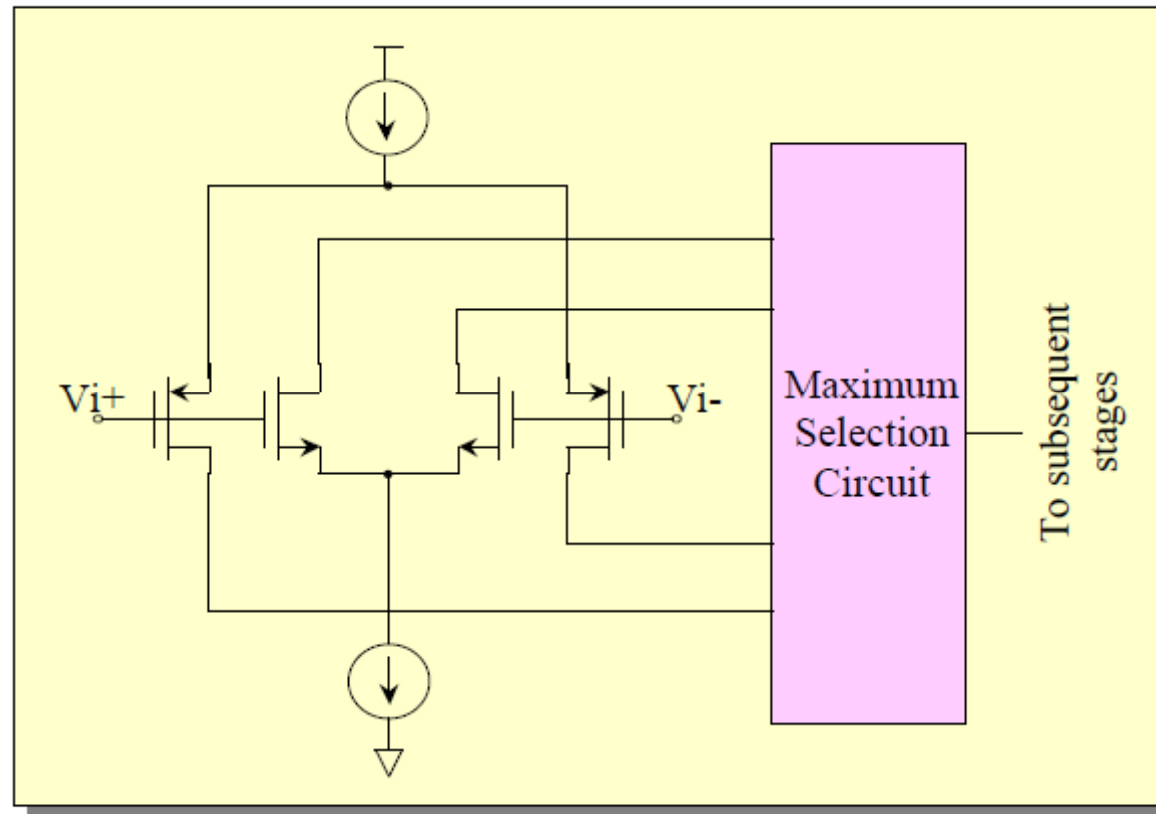
Maximum Current Selection Circuit:

•When Iin1>Iin2, M2 and M3 try to mirror Iin1, but as Iin2<Iin1, there is no enough current for M3 to sink, M3 will work in Ohmic region and its VDS is very small. M4 and M5 are off. So Iout = Iin1

•When Iin2>Iin1, $I_{D2}=I_{D3}=$Iin1, $I_{D4}=I_{D5}=$Iin2-Iin1. Iout $=I_{D5}+I_{D2}=$Iin1+(Iin2- Iin1)=Iin2

•The whole input stage

All of the transistors are with the same geometry.


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Working Principle:

•Please notice that if we apply a positive differential voltage to the inputs Vi+ and Vi-, the currents of M1 (P type) and M4 (N type) will decrease, and the currents of M2 (P type) and M3 (N type) will increase. We apply the current of M2 and mirrored current of M3 to Maximum Selection Circuit I, and current of M1 and the mirrored current of M4 to Maximum Selection Circuit II.

•When the common mode input voltage is close to Vdd, the tail current of the P input pair decreases, the maximum selection circuits conduct the drain currents of N pair to the outputs.

•When the common mode input voltage is close to -Vss, the tail current of the N input pair decreases, the maximum selection circuits conduct the drain currents of P pair to the outputs.

•At the outputs, we get the larger currents of the 2 input pairs, and hence the larger gm.

•Transconductance vs. input common mode voltage:
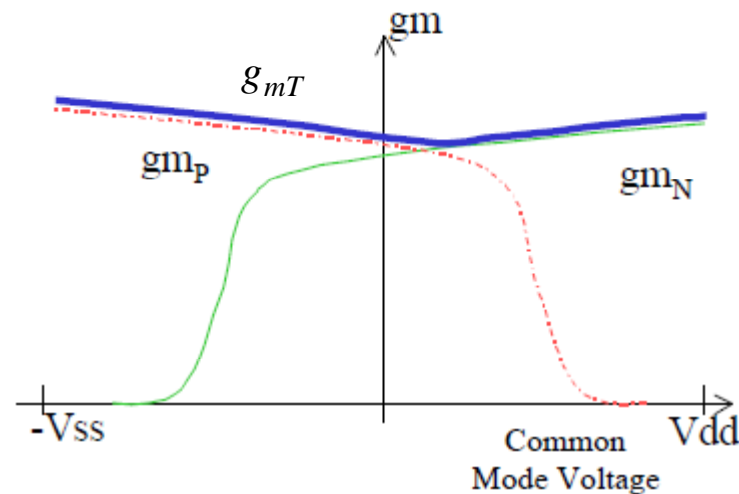
•There is another configuration which utilizes folded cacode circuit and minimum selection circuit to get the maximum gm.

•As in the folded cascoded shown in the next circuit , if Iin is at it maximum value, we will get a minimum Iout. So with this folded cascode circuit, we can not use maximum selection circuit, instead, we should use minimum selection circuit.
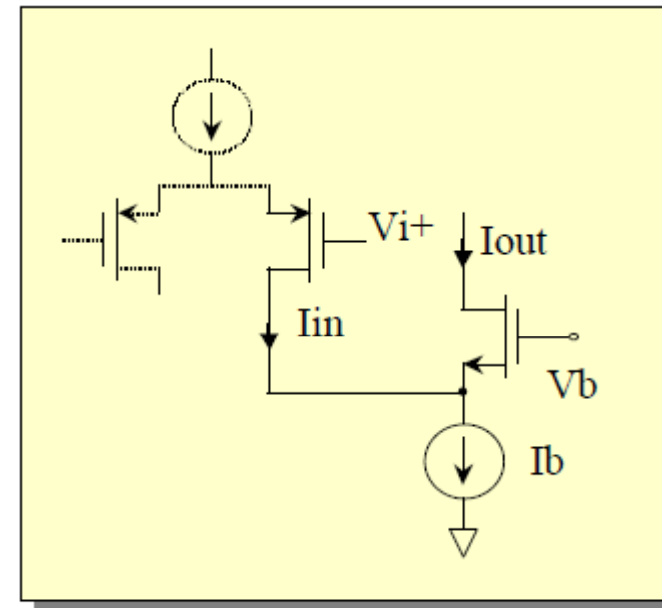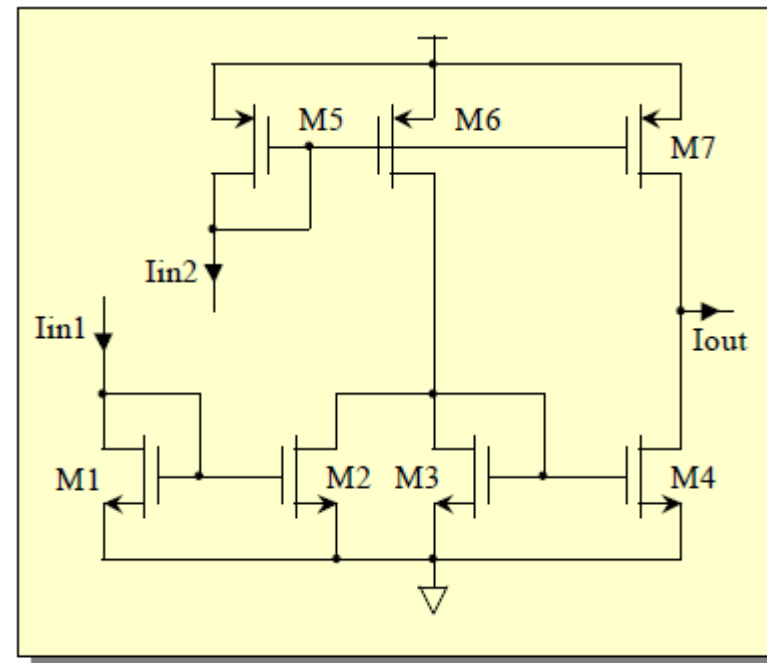

•The minimum selection circuit:
✓As shown in the right circuit, all N transistors are with the same geometry, and P transistors are with the same geometry.
✓If Iin2<Iin1, $I_{D5}=I_{D6}=I_{D7}$=Iin2, M2 works in ohmic region, and M3 and M4 are off. Iout= I_{D7}=Iin2.
✓If Iin1<Iin2, $I_{D5}=I_{D6}=I_{D7}$=Iin2, $I_{D1}=I_{D2}$=Iin1, $I_{D3}=I_{D4}$=Iin2-Iin1, Iout= I_{D7}-I_{D4}=Iin2-(Iin2-Iin1)=Iin1.

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•**The input stage with folded cascode and minimum selection circuit:**

Folded Cascode and Minimum Selection Circuit I