Dynamic Offset Compensated CMOS Amplifiers

F. Witte, K.A.A. Makinwa, J. Huijsing, Dynamic Offset Compensated CMOS Amplifiers, Springer, 2009.

•Offsets exist all of the CMOS design
• Offset Voltage in CMOS is larger when compared to BJT and BiCMOS
•But we can reduce offset “enough” by

1. Using “large” devices and good layout
2. Trimming
3. Dynamic offset-cancellation (DOC) techniques

•DOC Versus Trimming

Advantage:

- reduction of offset and 1/*f noise*
- excellent long term stability
- no additional costs for testing

Disadvantage

- reduced bandwidth
- increased circuit complexity
- aliasing & intermodulation issues

❑Auto-zero amplifiers (AZA)

➢1. Output offset storage

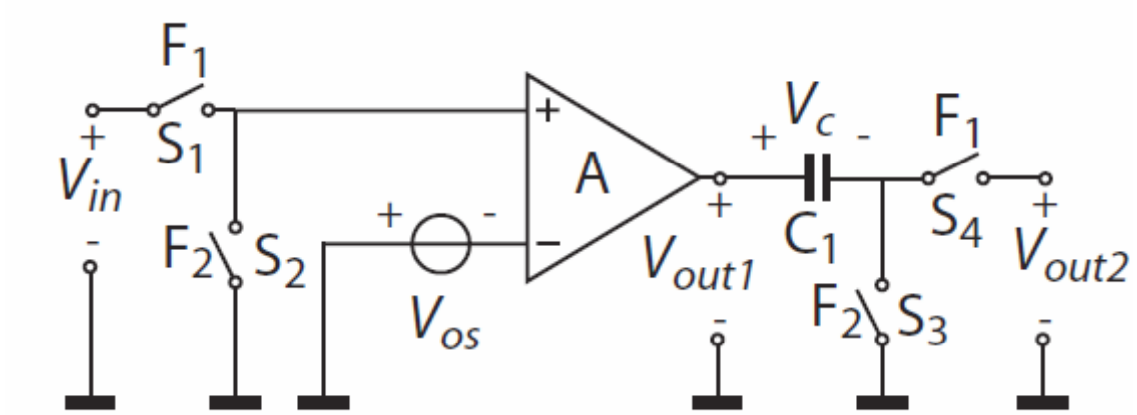
❖During auto-zeroing, two phases in time can be distinguished:

- •auto-zero phase in which the offset of a system is measured and stored
- •signal phase in which the signal is amplified and the offset is subtracted from the signal

❖Probably the simplest way to implement dynamic offset compensation is to place a capacitor at the output of an amplification stage, as shown in the next figure. The capacitor C_1 is used to store the output referred offset and subtract it from the signal.

❖During the sampling phase F_2, S_1 and S_4 are open and S_2 and S_3 are closed.

❖During the signal phase F_1, S_1 and S_4 are closed and S_2 and S_3 are open.



❖During the sampling phase F2 the voltage over the auto-zero capacitor C1 can be expressed as:

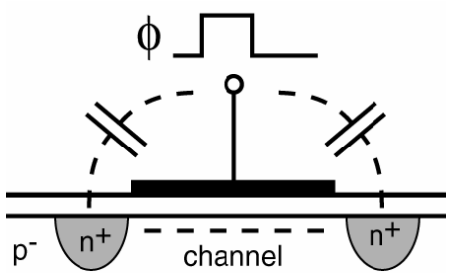
$$V_{out1} = V_c = AV_{os},$$

while during the signal phase F1 the output voltage can be expressed as:

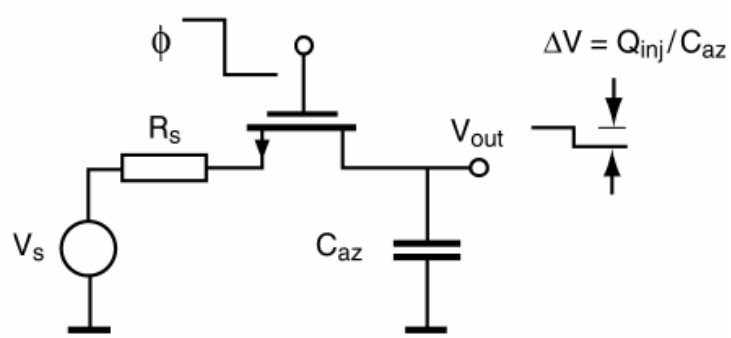
$$V_{out1} = (V_{in} + V_{os})A \text{ and } V_{out2} = V_{out1} - V_c = AV_{in}$$

❖This means that theoretically all offset is cancelled using this method.
❖However, when the switches are implemented with MOS transistors they will inject charge into the auto-zero capacitance C1.

Charge Injection



•Occurs when MOSFETs switch OFF
•Consists of two components
1.Channel charge, Qch= $WLC_{ox}(V_{GS}-V_{TH})$
2.Overlap capacitance between the gate and the source/drain diffusions



Error voltage depends on:
•Source impedance
•Transistor area (WL)
•Value of C_{az}
•Clock amplitude & slew rate

❖It can be assumed that a charge q_{inj} is produced by the switch each time it closes, and an equal negative charge $-q_{inj}$ each time it opens.
❖At the end of the auto-zero phase, switch S3 opens and switch S4 closes. Therefore, a charge injection mismatch $q_{inj3}-q_{inj4}$ is fed into the storage capacitor. Thus:

$$V_{out1} = V_c = \mathrm{A}V_{os} + \frac{(q_{inj3} - q_{inj4})}{\mathrm{C}_1}.$$

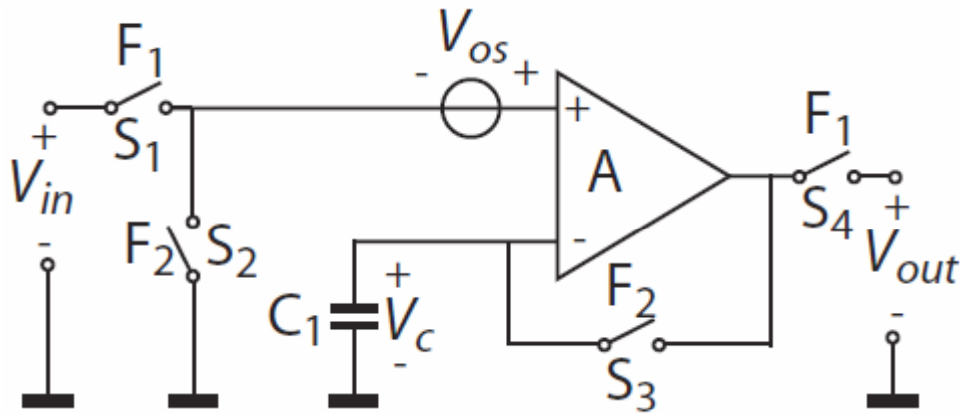
❖This results in a residual offset of:

$$V_{os,res} = \frac{(q_{inj3} - q_{inj4})}{\mathrm{AC}_1}.$$

❖The influence of this mismatch on the residual offset can be reduced by increasing the size of the capacitor. Since the auto-zero capacitor is at the output of the amplifier, these effects can be divided by the voltage gain when referred to the input.
❖Leakage from capacitor C1 during the amplification phase also causes residual offset. This effect can also be divided by the voltage gain.
❖A disadvantage of auto-zeroing with output offset storage is that the output range is reduced by $2AV_{os,max}$ where $V_{os,max}$ is the maximal input offset that can be expected of an uncompensated amplifier.
❖When the voltage gain is 40 dB and $V_{os,max}$ =10mV, then the output range is reduced by 2 V.

➢2. Input offset storage

❖This technique is also known as closed loop offset cancellation in the literature.
❖During the sampling phase F2, S1 and S4 are open while S2 and S3 are closed.
❖During the signal phase F1, S1 and S4 are closed while S2 and S3 are open.



❖During the sampling phase F2, the voltage over the auto-zero capacitor C1 can be expressed as:

$$V_c = \frac{A}{A+1} V_{os},$$

while during the signal phase F1 the output voltage can be expressed as:

$$V_{out} = (V_{in} + V_{os} - V_c)A = \left(V_{in} + \frac{1}{A+1} V_{os}\right)A$$

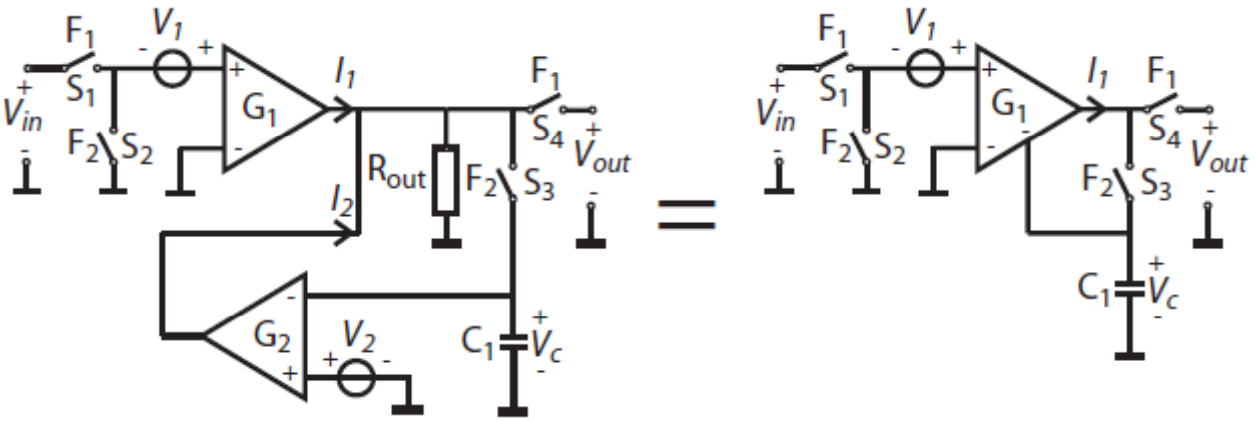
❖The channel charge of switch S3 will again cause a voltage step across the auto-zero capacitor C1

$$V_{os,res} = \frac{V_{os}}{A+1} + \frac{q_{inj3}}{C_1}.$$

❖The influence of S3 on the residual offset can be reduced by increasing the size of the capacitor.
❖In addition, the leakage of the capacitor C1 during the amplification phase can cause residual offset.
❖These two effects cannot be divided by the voltage gain because the auto-zero capacitor is already at the input.
❖In differential circuits, the residual offset due to charge injection will also be reduced.
❖This technique can be used to auto-zero a high gain operational amplifier. The residual offset is then dominated by the charge injection.

➢3. Auxiliary amplifier

❖Another technique for auto-zeroing which is less sensitive to charge injection is depicted in the next figure.
❖In many cases, an amplifier will consist of a transconductance G1 with an output impedance Rout.
❖This transconductance G1 has an offset voltage V1.
❖Phase F1 is the signal phase in which the input signal is applied to the amplifier and the output signal is useful.
❖Phase F2 shorts the inputs of G1 and its offset Vos causes an output current I1 to flow.
❖This output current is integrated on capacitor C1. This capacitor drives an auxiliary input transconductance G2, which causes an offset compensating current I2 to flow.



❖Auto-zeroing with an auxiliary input stage and an integrator. The right-hand schematic is commonly used.

❖The loop gain limits the offset reduction. In steady state during auto-zero phase F2 the following equation applies:

$$V_C = V_1 G_1 R_{out} + (V_2 - V_C) G_2 R_{out} \quad V_C = \frac{V_1 G_1 R_{out} + V_2 G_2 R_{out}}{1 + G_2 R_{out}},$$

❖while during the signal phase F1 the following equation applies:

$$V_{out} = (V_1 + V_{in}) G_1 R_{out} - V_C G_2 R_{out} = G_1 R_{out} V_{in} + \frac{V_1 G_1 R_{out}}{1 + G_2 R_{out}} + \frac{V_2 G_2 R_{out}}{1 + G_2 R_{out}}$$

❖The residual offset due to finite gain can be expressed by:

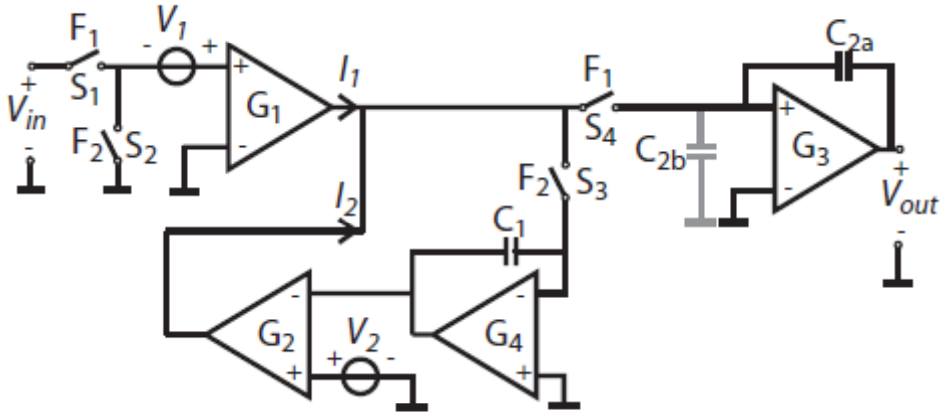
$$V_{os,res,gain} = \frac{V_1}{1 + G_2 R_{out}} + \frac{1}{G_1 R_{out}} \frac{V_2 G_2 R_{out}}{1 + G_2 R_{out}} \approx \frac{V_1}{A_2} + \frac{V_2}{A_1},$$

❖where A2 and V2 are the DC voltage gain and offset of G2, which acts as an auxiliary input of G1.

❖Except for the limited voltage gain, additional residual offset is also caused by the charge injection of switch S3 and the leakage of the capacitor C1 during the signal phase.
❖The charge injection causes the residual offset to become:

$$V_{os,res,inj} = \frac{G_2 q_{inj3}}{G_1 C_1}.$$

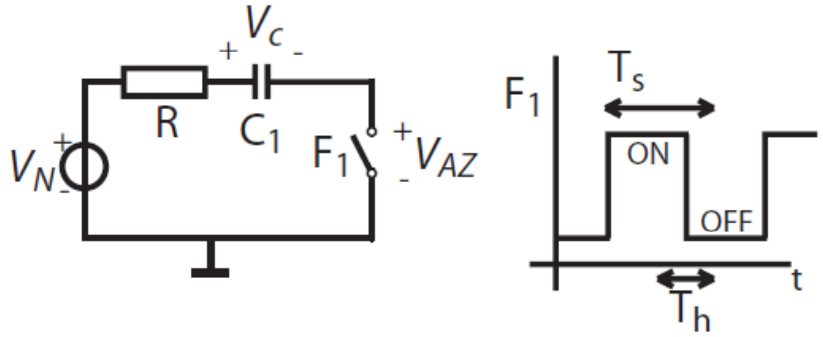
❖The output of G1 has to switch between the output voltage and the voltage VC over the compensation capacitor C1. This voltage step itself can cause settling problems, which cause voltage spikes.
❖To circumvent these problems another topology can be used in which C1 can be replaced with an active integrator.
❖This concept is shown in the next figure. The amplifier stage G4 used to implement the active integrator has the same input common-mode voltage as the output stage G3. The output voltage of G1 is bounded at this common-mode voltage. Capacitor C2b acts as a track-and-hold.



❖Because of the sampling action, auto-zeroing is a technique which is not suited for continuous time applications.
❖Auto-zeroing itself is mainly used in switched capacitor circuits, which are already sampled systems.

•Noise in auto-zero amplifiers

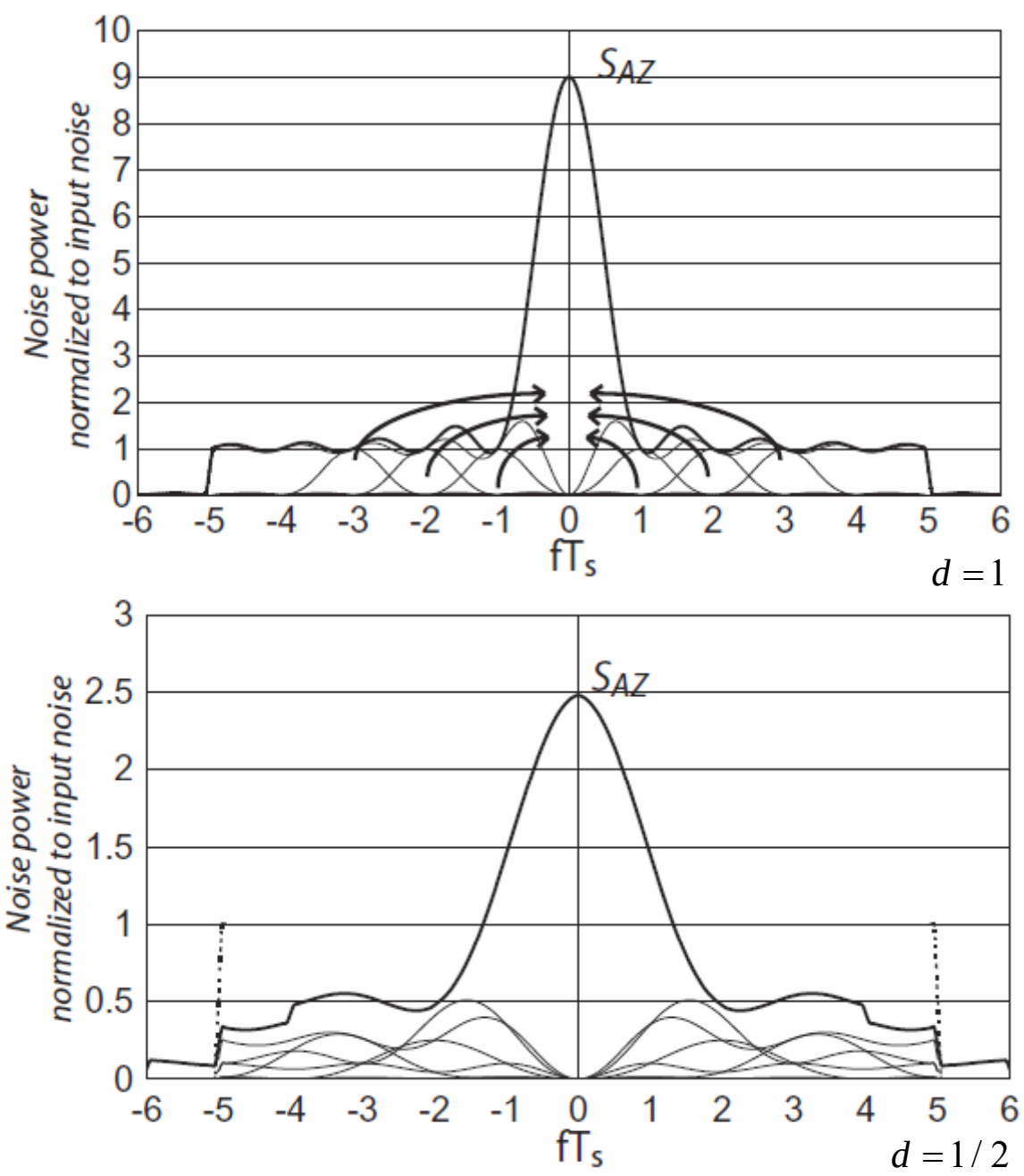
❖The auto-zero technique cannot distinguish low-frequency noise from offset. Therefore, the noise behaviour over frequency of an auto-zeroed amplifier is also affected.



❖The noise power spectral density (PSD) for the auto-zero voltage across the switch can expressed as:

$$S_{AZ}(f) = \sum_{n=-\infty}^{\infty} |H_n(f)|^2 S_N\left(f - \frac{n}{T_s}\right),$$

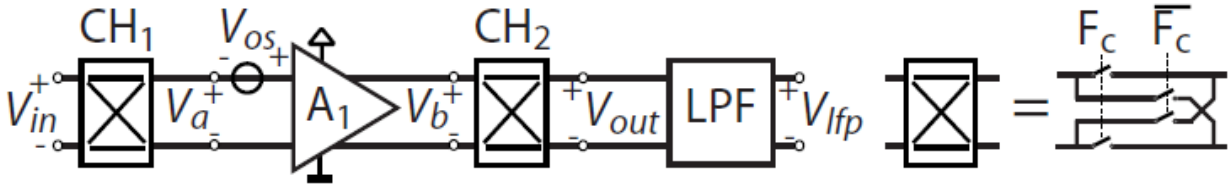
$$|H_n(f)|^2 = d^2\left\{\left[\frac{\sin(2\pi dn)}{2\pi dn} - \frac{\sin(2\pi f T_h)}{2\pi f T_h}\right]^2 + \left[\frac{1-\cos(2\pi dn)}{2\pi dn} - \frac{1-\cos(2\pi f T_h)}{2\pi f T_h}\right]^2\right\} \qquad \frac{T_h}{T_s} = d,$$


Noise power
normalized to input noise
S_{AZ}
fT$_s$
$d = 1$
Noise power
normalized to input noise
S_{AZ}
fT$_s$
$d = 1/2$

❑Chopper amplifiers

❖While in auto-zero amplifiers the offset and input signal are time-modulated, in chopper amplifiers they are frequency-modulated.

❖In chopper amplifiers the signal of interest and the offset signal are shifted to different frequencies.



❖This amplifier consists of a frequency modulator, or chopper CH1, a voltage amplifier A1, another chopper CH2, and a low-pass filter (LPF).

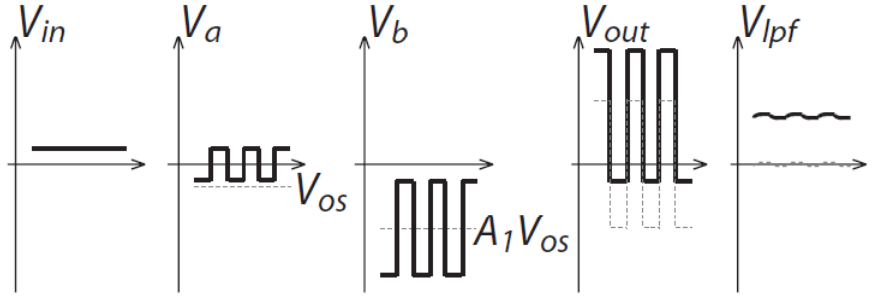
❖The chopper symbol is also depicted, which is a polarity switch driven by a square wave with a chopper frequency FC.

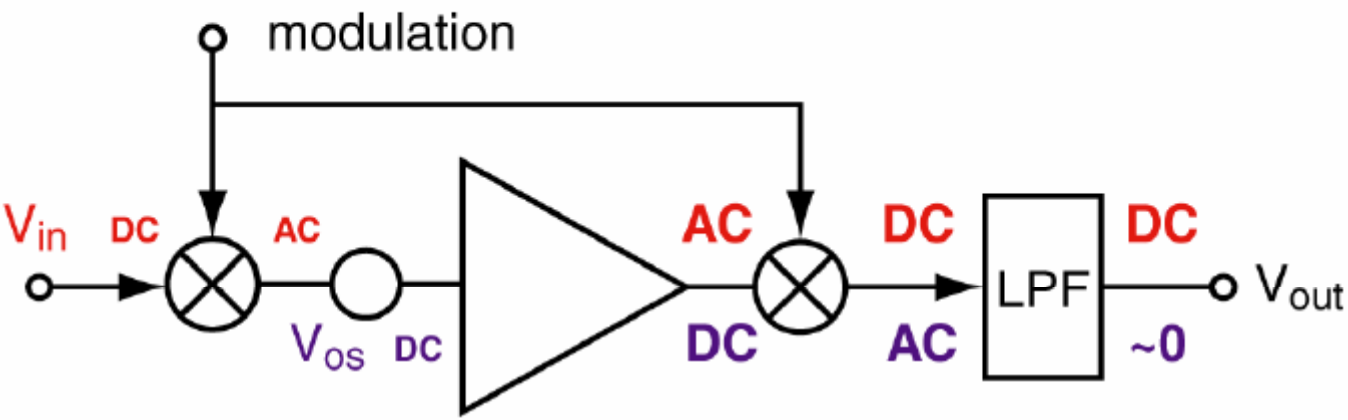
❖The idealised waveforms are depicted in the time domain in the next figure.

❖The first chopper is used to modulate the input signal to a higher frequency.

❖Then the amplifier amplifies the modulated signal superposed on its own input noise sources.

❖Lastly, the second chopper demodulates the amplified input signal, and also modulates the output noise and offset of the amplifier A1.

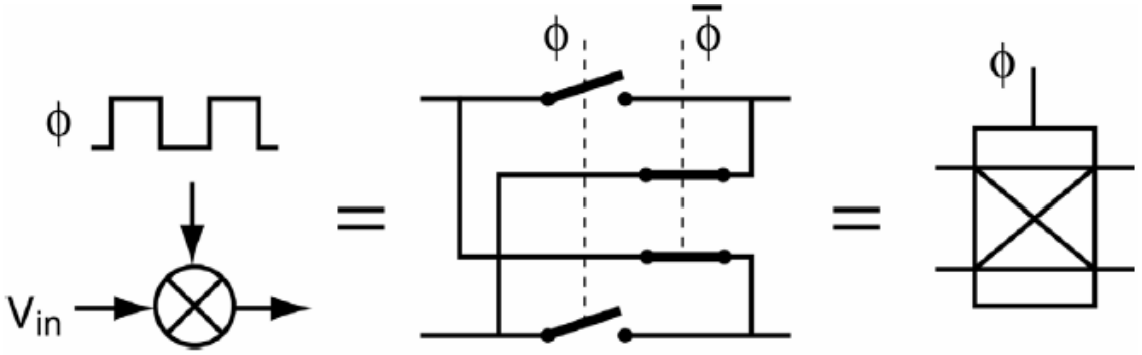




Easily generated modulating signal

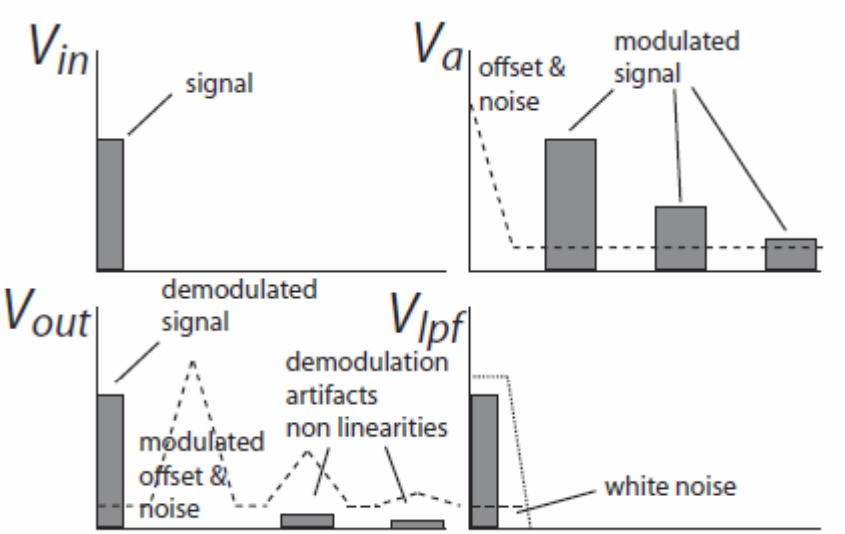
•The modulator is a polarity-reversing switch

•Switches are easily realized in CMOS



•1. Noise in chopper amplifiers

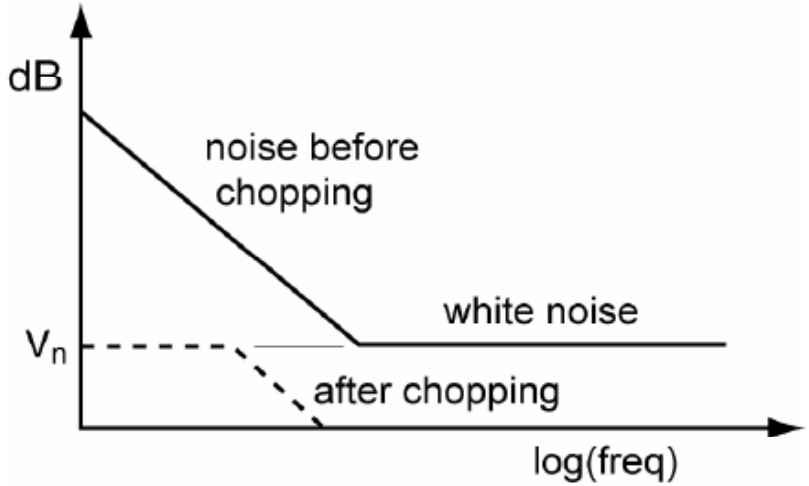
❖When a low-pass filter is used after the chopper amplifier, the chopper ripple and low-frequency noise can be filtered.
❖CMOS amplifiers usually have a high DC input offset voltage and 1/f noise.
❖To reduce the 1/f noise, the modulation or chopper frequency chosen should be higher than the 1/f corner frequency.
❖This is illustrated in the next figure. In this figure it is shown that the signal is modulated, and that noise and offset is superposed on this modulated signal. Afterwards the signal, noise and offset are modulated. This means that the signal is demodulated, after which the signal can be filtered out.



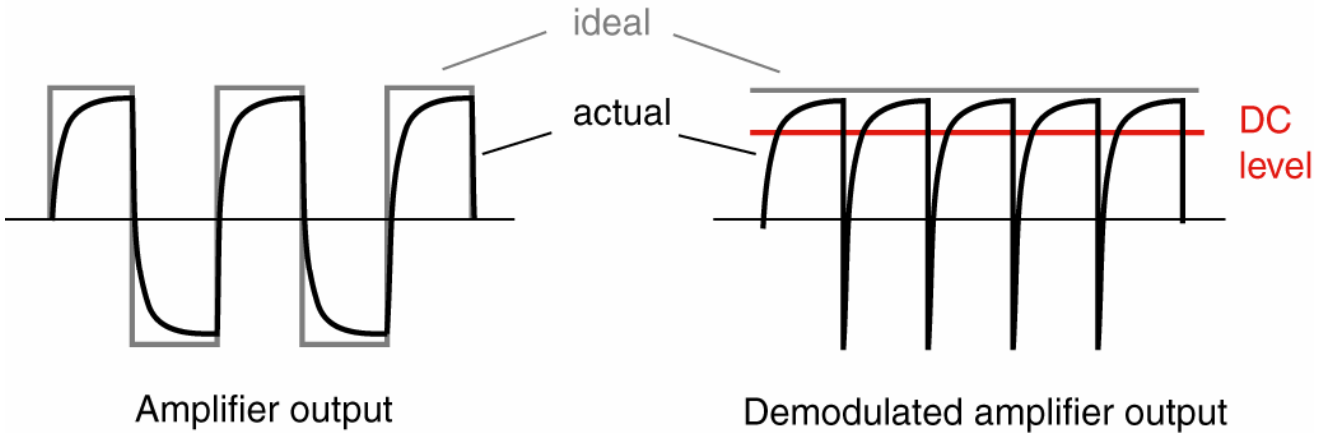
❖From this analysis it can be concluded that the chopper technique completely reduces the 1/f noise when the chopper frequency is higher than the corner frequency of the 1/f noise.
❖In practice the noise level of a chopper amplifier is slightly higher than the thermal noise level. However, the need to suppress the chopper ripple means that only a low bandwidth is obtainable with a chopper amplifier.

Residual Noise of Chopping

•1/fnoise is **completely removed provided fch> 1/f corner frequency**
•Significantly better than auto-zeroing!
•State-of-the-art is 8.5nV/√Hz
C. Menolfi, Q.Huang, "A fully integrated CMOS instrumentation amplifier with submicrovolt offset," IEEE JSSC, vol. 34, March 1999, p.p. 415-420.

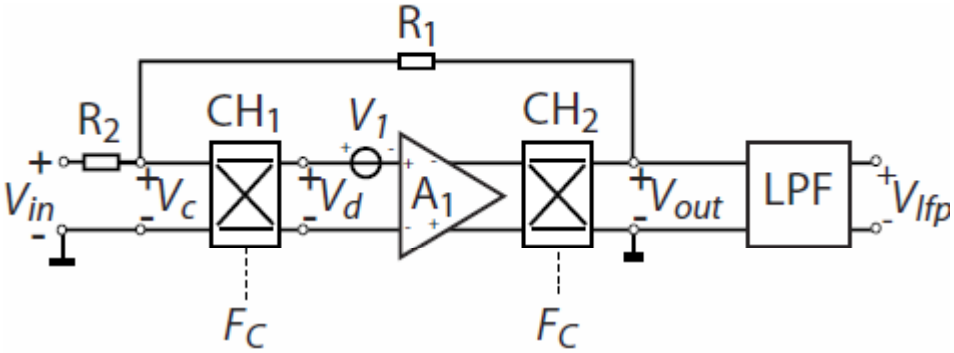


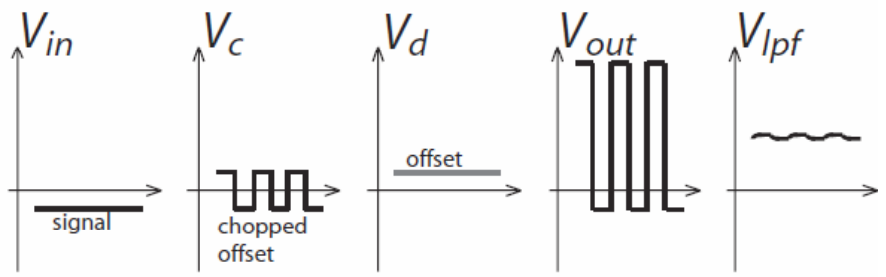
Bandwidth & Gain Accuracy



•Limited BW reduces effective gain
•$A_{eff} = A_{nom}(1-4\tau/T)$ for a 1st order LPF, where $f_{ch} = 1/(2\pi\tau)$ and $\tau << T$
•$T/\tau = 40 \Rightarrow$10% error!

➢2. Chopped operational amplifier in a feedback network





❖Idealised waveforms in the time domain of a chopped operational amplifier in a feedback network for (gain=3).

❖The output V_{out} of the chopper amplifier can now be expressed by:

$$V_{out} = V_c - \frac{V_{in} - V_c}{R_2} R_1 = -V_{in}\frac{R_1}{R_2} + V_c\left(1 + \frac{R_1}{R_2}\right).$$

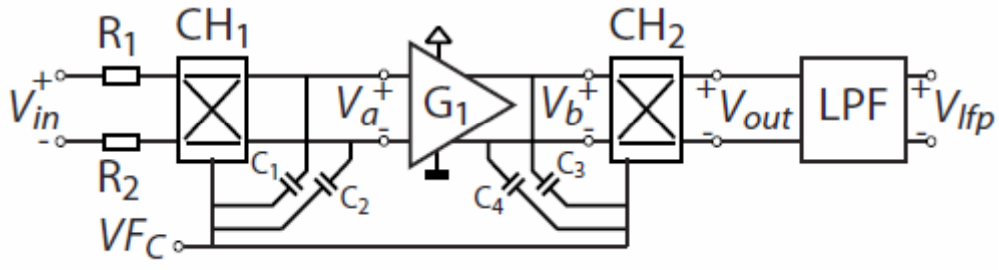
❖The conclusion which can be drawn from this analysis is that the chopper ripple of a chopped operational amplifier in a feedback network is visible at the input of the first chopper.

3. Charge injection effects in chopper amplifiers

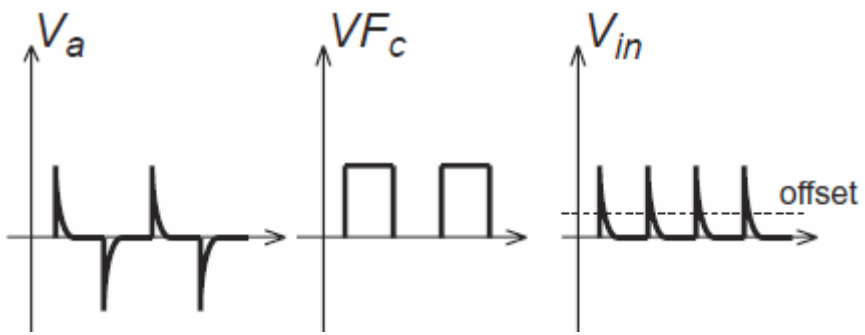
•In these amplifiers the residual offset is mainly caused by the charge injection mismatch from the clock lines to the input and output of the amplifier that is chopped.

•In the next figure this is modelled with cross talk capacitors C1 to C4. The resistors R1 and R2 model the on-resistance of the switches used in the chopper and the source resistance.

•When both lines are loaded with identical cross talk capacitors, no residual offset will occur since it will be a common-mode spike.



•However, if there is a slight mismatch between the two capacitors, a differential component will also appear at Va, which will translate into a residual offset, because these spikes are actually demodulated by the input chopper towards the input.



•Therefore, each time the chopper clock switches charge is being injected into the input, this differential charge can be expressed by:

$$q_{inj} = (C_1 - C_2)V_F$$

where VF is the driving voltage of clock VFC.

•This charge is applied two times the per clock period. This means that a current will run through the resistors R1 and R2. So the residual offset can be expressed by:

$$V_{os,res1} = 2(R_1 + R_2)(C_1 - C_2)V_F F_C$$

where FC is the chopper frequency.

•This means that the residual offset increases with increasing chopper frequency.

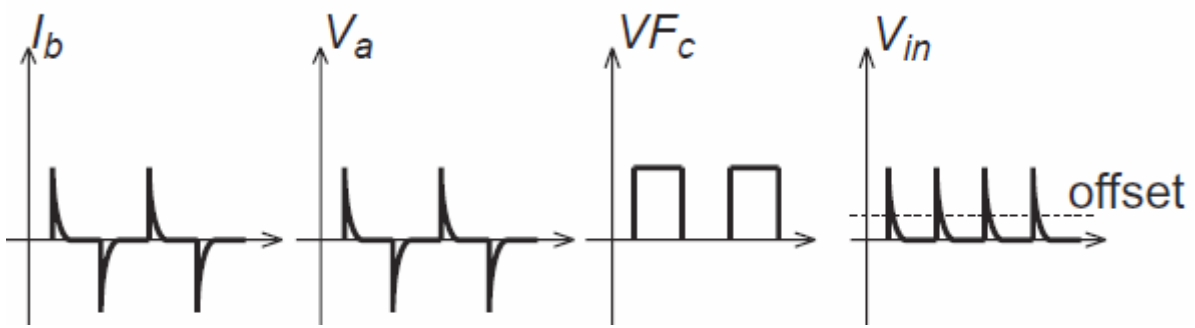
•However, the chopper frequency needs to be higher than the 1/*f* corner frequency to obtain optimal noise performance.

•For example the residual offset per unit of capacitance for a 20 kHz chopper frequency, an on-resistance of 5 kΩ with no source impedance and a 5 V driving voltage, would be 2 μV/fF.

•Secondly the effect of the mismatch between C3 and C4 will be analysed. Also the capacitors C3 and C4 can cause residual offset. When C3=C4 no residual offset will occur, since it will be a common-mode spike.

•However, if there is a slight mismatch between the two capacitors, a differential current spike will appear at *Vb,* and thus a differential voltage spike will appear at *Va,* which will translate into a residual offset, because these spikes are actually demodulated by the input chopper towards the input.

•This effect is illustrated in the next figure.



•This leads to an extra residual offset which can be expressed by:

$$V_{os,res2} = \frac{2(C_3 - C_4)V_F F_C}{G_1}$$

where G1 is the transconductance of the chopped amplifier.

•It can be seen that higher transconductance amplifiers will be less vulnerable to the mismatch of C3 and C4.

•For example for a 20 kHz chopper frequency, a 100 μA/V transconductance, and a 5 V driving voltage the residual offset per unit of capacitance would be 2 μV/fF.

•The residual offset caused by the charge injection can be expressed as:

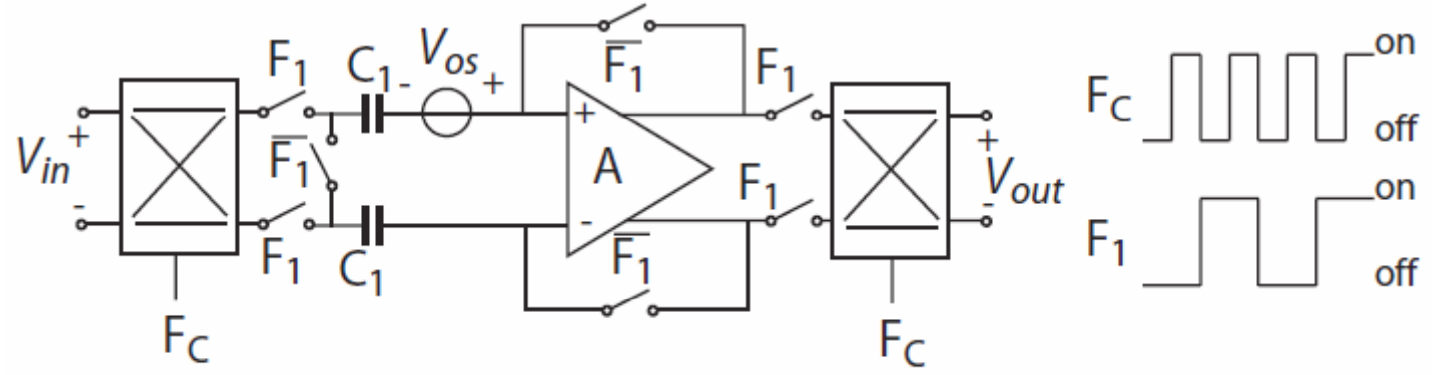
$$V_{os,res} = V_{os,res1} + V_{os,res2}$$

❑Chopped auto-zeroed amplifier

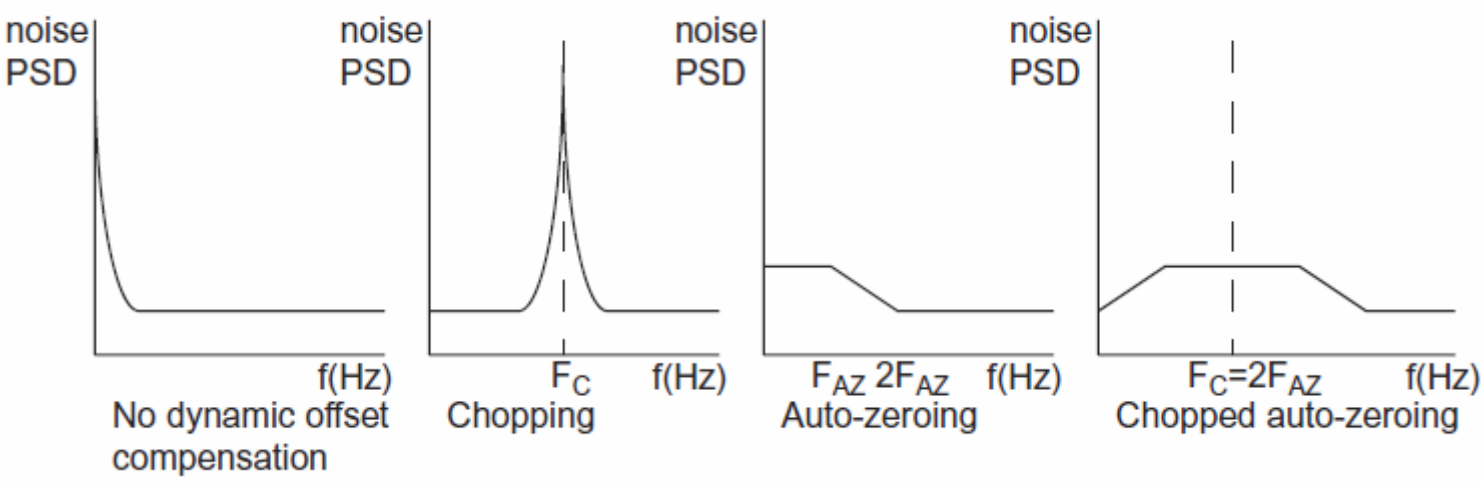
•Theoretically, the combination of auto-zeroing and chopping would have a better offset performance because the residual offset of the auto-zero amplifier is being chopped.

•Practically in some applications the charge injection of the chopper is the dominant source of residual offset, and auto-zeroing will only have a small effect on the residual offset.

•A chopped auto-zero amplifier, with an auto-zero duty cycle of 50% and a chopper frequency two times higher than the auto-zero frequency:



•However, there is also an effect of the noise, because the folded white noise can be modulated as well. This reduces the effect of folded white noise.
•This means that if an auto-zero amplifier running with a 50% duty cycle is chopper modulated with the double auto-zero frequency, that the noise around DC would then be optimal.
•The reduction in noise at low frequencies as well as the rise in noise towards the chopper frequency is sketched in the next figure.



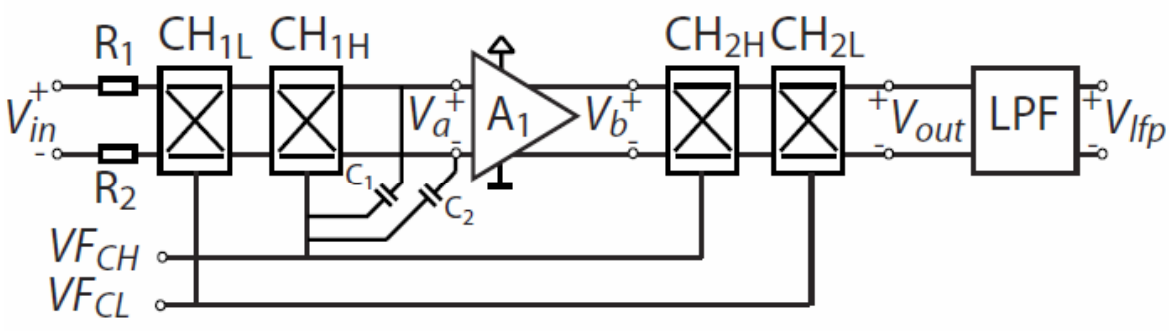
•The folded noise can be modulated to even higher frequencies by using a higher chopper frequency.
•During each signal phase the polarity of the chopper should be positive and negative for an equal time, to average out the noise contribution, that is sampled during each auto-zero phase.
•Therefore, optimal noise at low frequencies will be achieved when:

$$F_C = \frac{n}{d} F_1 \text{ and } n = 1,2,3 \ldots$$

❑Charge injection suppression circuits

➢Nested chopper

•The residual offset due to mismatch is proportional to the chopper frequency. In the nested chopper technique this residual offset is also chopped.



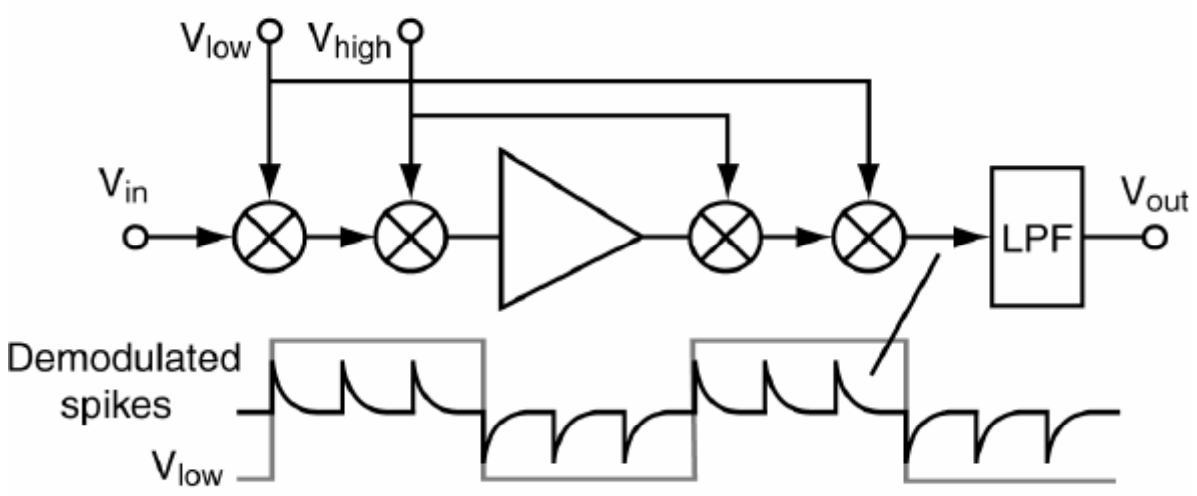
•The inner choppers CH_{1H} and CH_{2H} run at a frequency F_{CH}. This frequency can be chosen optimally for noise, i.e. F_{CH} should be chosen higher than the 1/*f* corner frequency. This high frequency will lead to a relatively high residual offset.

•The nested choppers CH_{1L} and CH_{2L} modulates this residual offset at a low frequency F_{CL}, which strongly reduces the offset. The frequency F_{CL} can be chosen optimal for the input signal.

•Thus, the nested choppers reduces the charge injection of the inner choppers.

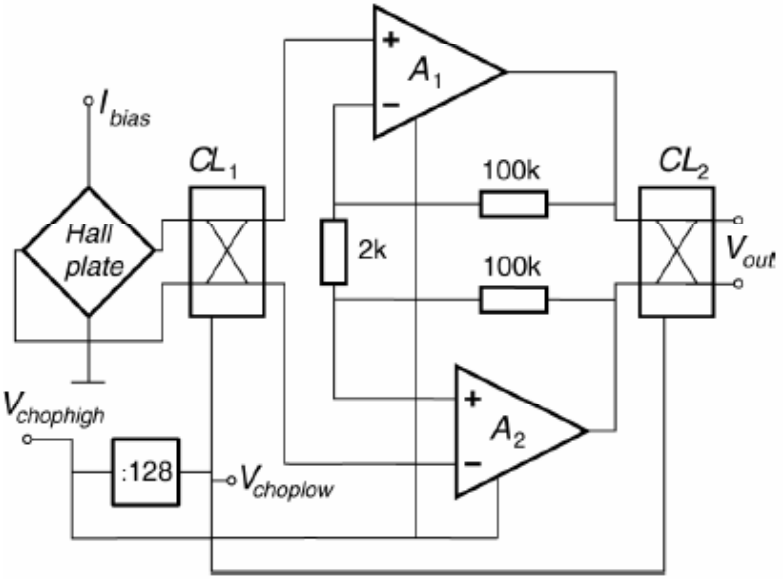
With this technique a 100 nV offset was obtained with FCH=2 kHz and FCL=15,6 Hz (A. Bakker, K. Thiele, J.H. Huijsing, “A CMOS nested-chopper instrumentation amplifier with 100-nV offset”, *IEEE JSSC, pp.* 1877–1883, Dec. 2000.)

•Inner chopper removes 1/fnoise, outer chopper removes residual offset



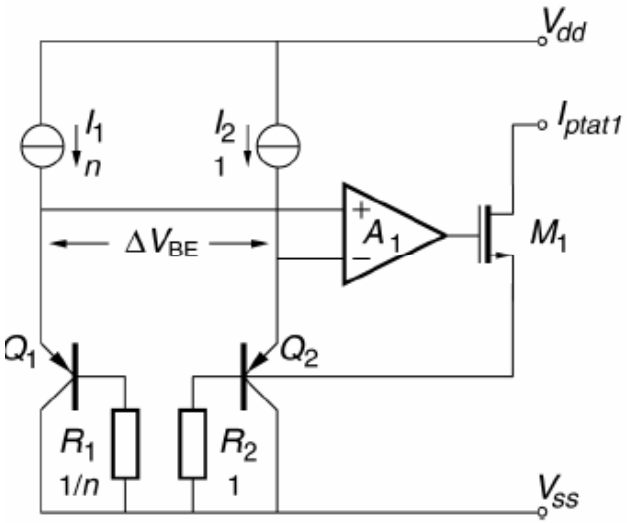
•This amplifier now has two ripples at the output. One ripple is caused by the offset of the amplifier A1, which is modulated with the frequency F_{CH}.
•The other ripple is caused by the residual offset, which is modulated at frequency F_{CL}. To filter this ripple a LPF is needed with a –3 dB frequency smaller than F_{CL}.
•This makes this technique useful in low frequency applications, like custom sensor read out electronics, such as implementations of fully integrated Hall-sensors and temperature sensors, but not for general purpose amplifiers.

A. Bakker, J.H.Huijsing, “Low-offset, low-noise 3.5mW CMOS spinning-current Hall-effect sensor with integrated chopper amplifier,”Proc. of Eurosensors XIII, Sept 1999, p.1045-1048.



•Hall-plate is read-out using spinning-current & nested chopper techniques

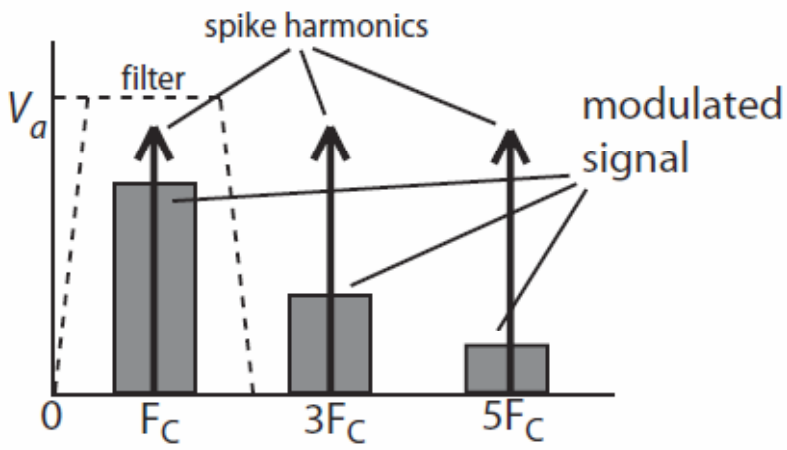
A. Bakker, “High-accuracy CMOS smart temperature sensors,” Kluwer Academic Publishers, Boston, 2000.



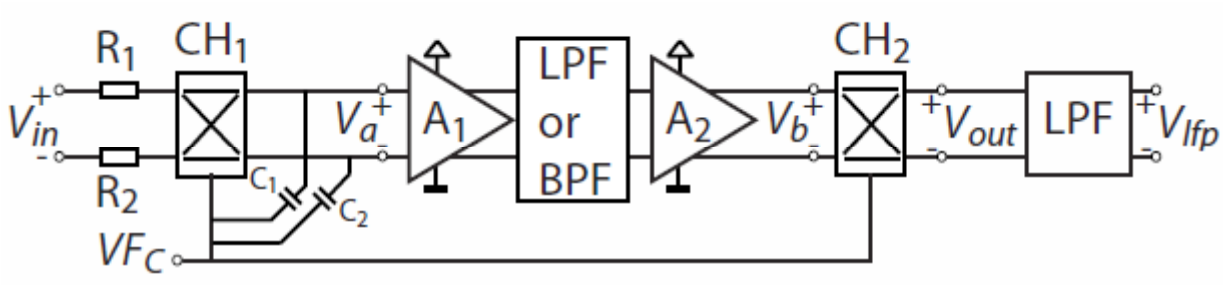
ΔVbe~ kT/q read-out using nested chopper technique
⇒±1°C uncalibrated accuracy

➢Spike filtering

•When it is assumed that charge injection causes residual offset, and that charge injection is an effect which occurs during the switching action of a switch, then it can also be assumed that the charge injection causes voltage spikes with high frequency.
•It can be assumed that the spikes have spectral components on the odd harmonics of the chopper frequency.

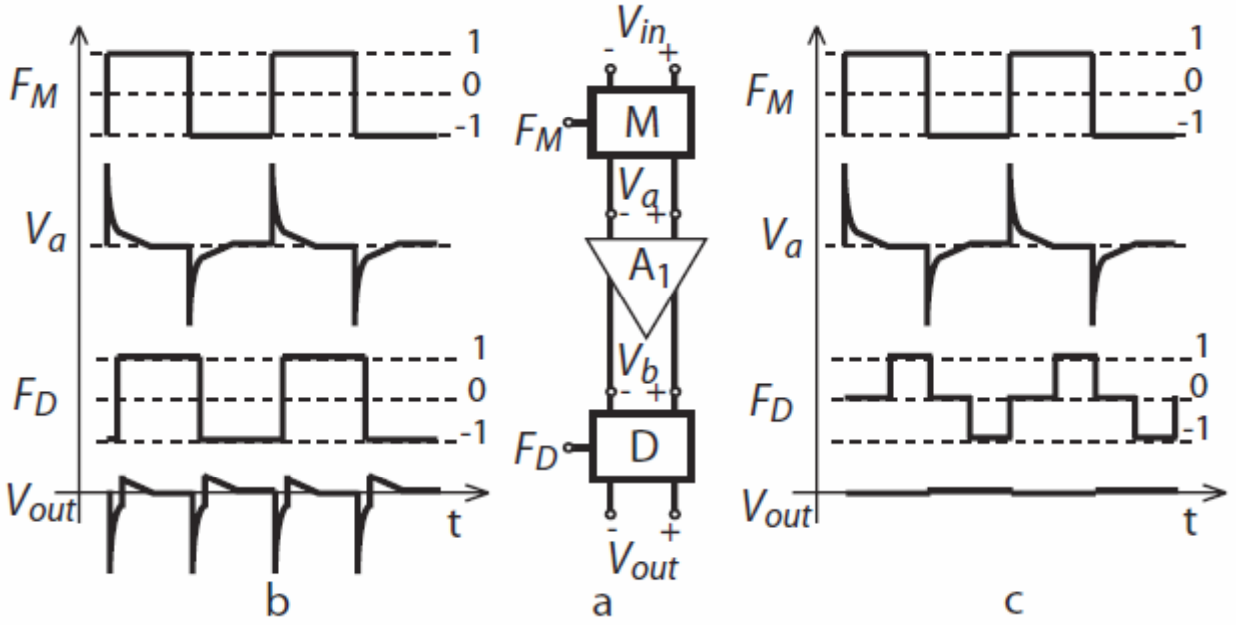


•An amplifier using this technique is illustrated in the next figure.

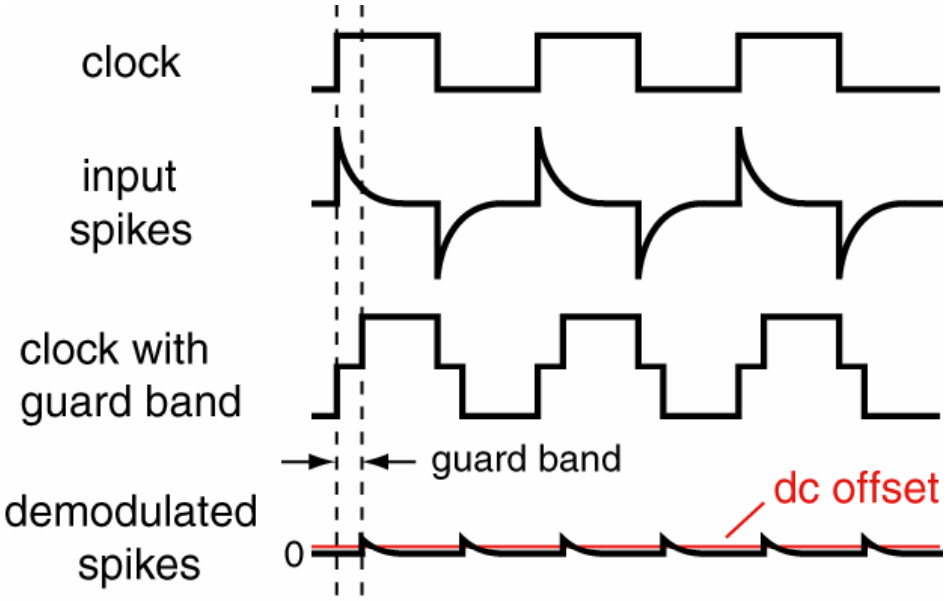


➢Delayed modulation and guard band

•Instead of putting effort into filtering the spikes in the frequency domain, it is also possible to filter the spikes in the time domain.
•In figure **a**, a modulated amplifier is shown consisting of a modulator M, amplifier A1, and demodulator D.
•In figure **b**, a delayed demodulation scheme is shown. The idea is that when the shape of the voltage spike is known, a fixed delay can be used to allow the demodulated spike to have an average value of zero. Thus, the spike is used to compensate for itself.
•However, a mismatch between the shape of the spike and the delay still causes residual offset.

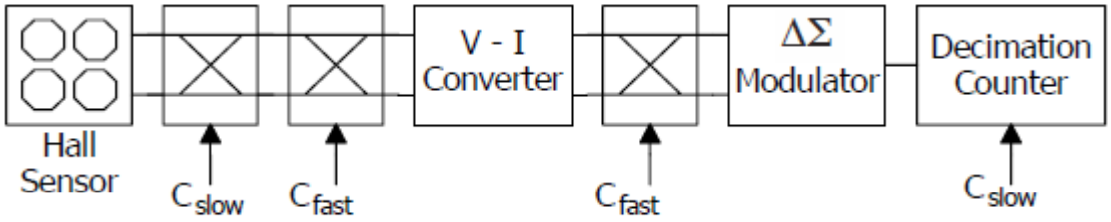


•Another approach, which is simpler to implement, is shown in figure c. In this dead-band or guard-band approach, the output voltage is not modulated while the spike is present.



•During guard-band, output is shorted or tri-stated.

J.C. van der Meer, F.R. Riedijk, E. van Kampen, K.A.A. Makinwa, J.H. Huijsing, “A fully integrated CMOS hall sensor with a 3.65μT 3σ offset for compass applications”, IEEE ISSCC, pp. 246–247, Feb. 2005.

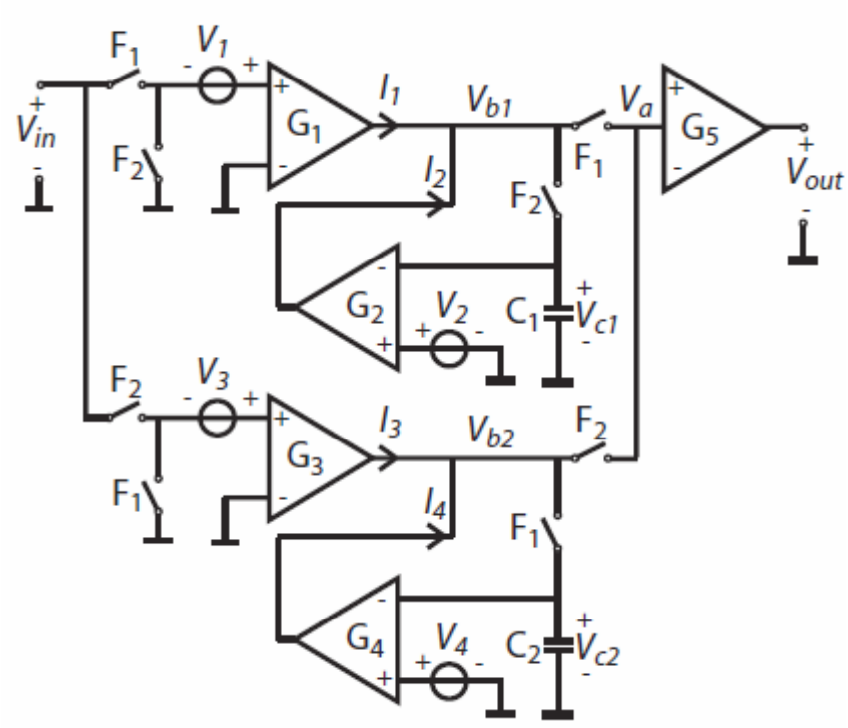


❑Dynamic Offset Compensated Operational Amplifiers

•Chopping is a frequency modulation technique, which requires low-pass filters in the signal path to filter chopper ripple out.
•Therefore, chopping alone is not suitable for broadband applications.
•Auto-zeroing is a time domain technique in which the offset is measured and afterwards subtracted from the signal. Therefore, this technique alone is not suitable for continuous-time operation.
•However, it will be shown that, by using these techniques in multi-path topologies, broadband continuous-time amplifiers can be realized.

➢Ping-pong auto-zero op amp

•Another way to make a continuous-time amplifier by using the auto-zero technique is the ping-pong technique.
•A ping-pong auto-zero operational amplifier uses two auto-zero amplifiers, which run in parallel to each other.
•While one is being auto-zeroed the other one is used to amplify the signal.
•This way a continuous-time broadband operational amplifier is created by time-domain multiplexing two auto-zero amplifiers.
•One of the amplifiers is always present to allow accurate and stable feedback.
•This technique was used to implement a rail-to-rail input.
•This technique was also implemented with a SAR ADC and digital offset storage



•A combination of this ping-pong technique together with the chopper technique has been used to obtain a 20 nV/√Hz noise PSD for <1 kHz operational amplifier.

•A disadvantage of the ping-pong technique is that spikes are caused because the voltages *Vb1* and *Vb2* at the output of the input amplifiers have to switch between the offset compensating voltages Vc1 and Vc2 and the voltage required at the input of the output amplifier Va.This results in spikes at the output.

•This effect can be reduced by replacing C1 and C2 with active integrators with the same input common-mode voltage as the output stage G5.

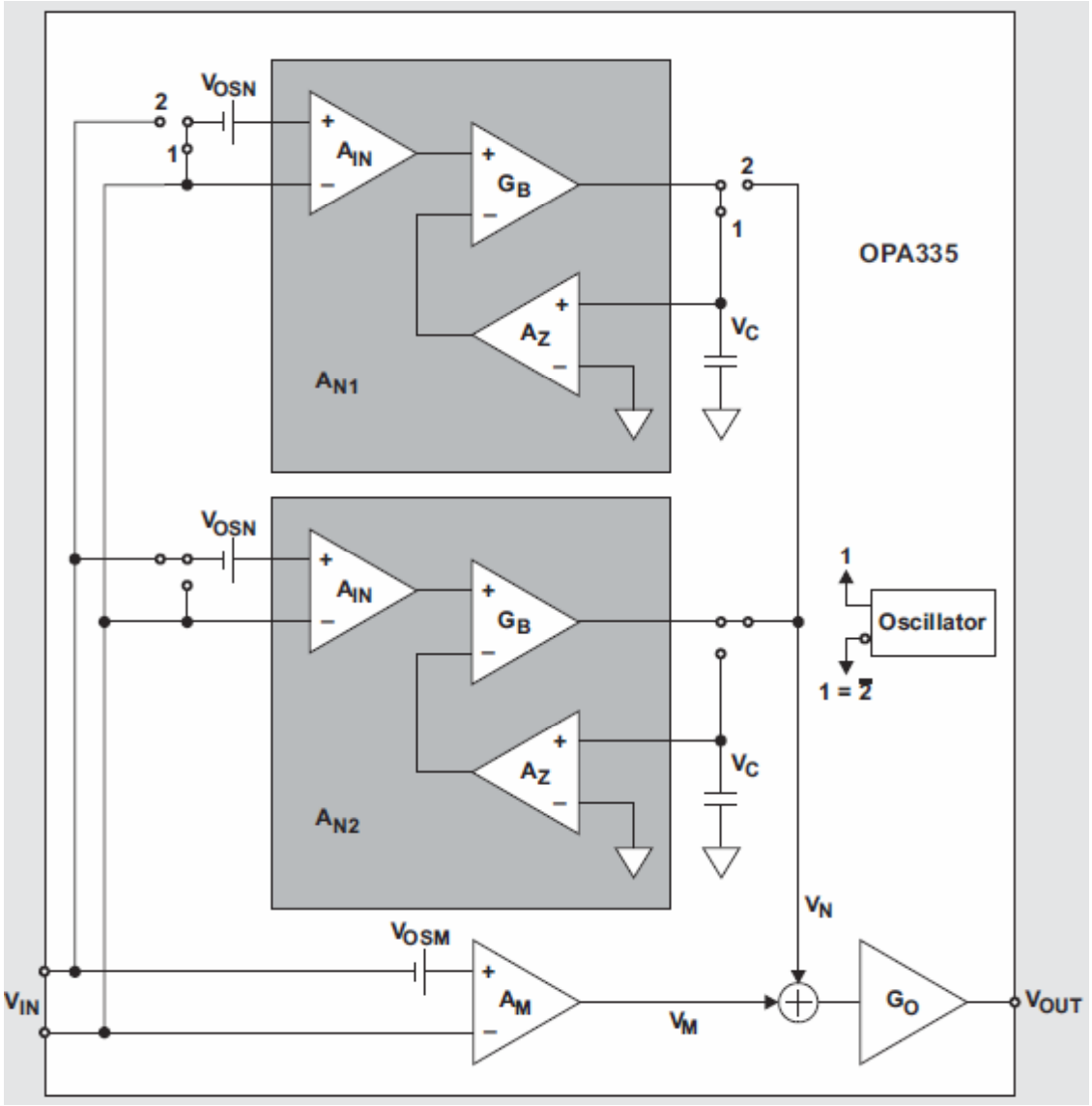
TI OPA335

•The two nulling amplifiers, AN1 and AN2, operate in an alternate mode in parallel with the main amplifier, AM. While AN1 nulls its offset during the auto-zero phase, AN2 is in the amplification phase, correcting the main amplifier's offset voltage and vice versa.

•The alternating operation of the nulling amplifiers minimizes output voltage ripple and intermodulation distortion (IMD) by keeping the amplifier's gain bandwidth constant during operation.

•Proprietary circuit design has made further improvements to the nulling amplifiers.

•Each amplifier consists of a multistage composite amplifier.



•The nulling amplifier, whose switches are in position 1, is in the autozero phase, thus charging its capacitor to

$$V_C = G_B(A_{IN}V_{OSN} - A_Z V_C) = V_{OSN}\left(\frac{G_B A_{IN}}{1+G_B A_Z}\right).$$

•During the amplification phase (with switches in position 2), the output voltage of the nulling amplifier, V_N, adds to the output voltage of the main amplifier, V_M. With

$$V_N = G_B\left[A_{IN}(V_{IN}+V_{OSN}) - A_Z V_C\right],$$

we can replace V_C to obtain

$$V_N = G_B A_{IN}\left(V_{IN} + \frac{V_{OSN}}{1+G_B A_Z}\right).$$

•The output of the main amplifier is simply

$$V_M = A_M\left(V_{IN} + V_{OSM}\right).$$

•The following output stage amplifies the summing signal by the factor G_O to

$$V_{OUT} = G_O(V_N + V_M).$$

$$V_{OUT} = G_O\left[A_M(V_{OSM}+V_{OSN}) + G_B A_{IN}\left(V_{IN} + \frac{V_{OSN}}{1+G_B A_Z}\right)\right].$$

•During the design process, the auto-zero structure is so optimized that $A_M = A_N$ and GB >> 1.

$$V_{OUT} = G_O G_B A_{IN}\left(V_{IN} + \frac{V_{OSM} + \frac{V_{OSN}}{A_Z}}{G_B}\right),$$

with $G_O G_B A_{IN}$ as the overall open-loop gain and

$$\frac{V_{OSM} + \frac{V_{OSN}}{A_Z}}{G_B}$$

as the effective input offset voltage of the complete AZA.

Auto-zeroed wideband amplifier: