CMOS Active Inductors

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CMOS ACTIVE INDUCTORS

Lossless Single-Ended Gyrator-C Active Inductors



Lossless Floating Gyrator-C Active Inductors



Floating gyrator-C active inductors offer the following attractive advantages over their singleended counterparts :

- (i) The differential configuration of the transconductors effectively rejects the common-mode disturbances of the network, making them particularly attractive for applications where both analog and digital circuits are fabricated on the same substrate.
- (ii) The level of the voltage swing of floating active inductors is twice that of the corresponding single-ended active inductors.

Lossy Single-Ended Gyrator-C Active Inductors



$$Y = \frac{I_{in}}{V_2} = sC_2 + G_{o2} + \frac{1}{s\left(\frac{C_1}{G_{m1}G_{m2}}\right) + \frac{G_{o1}}{G_{m1}G_{m2}}}$$



•This self-resonant frequency is typically the maximum frequency at which the active inductor operates. The self-resonant frequency of an active inductor is set by the cut-off frequency of the transconductors constituting the active inductor.

•The small-signal behavior of a gyrator-C active inductor is fully characterized by its RLC equivalent circuit.

•The RLC equivalent circuit of gyrator-C active inductors, however, can not be used to quantify the large-signal behavior, such as the dependence of the inductance on the dc biasing condition of the transconductors and the maximum signal swing of the gyrator-C active inductors.

Lossy Floating Gyrator-C Active Inductors



$$-G_{m1}(V_{2}^{+} - V_{2}^{-}) + \left(\frac{sC_{1} + G_{o1}}{2}\right)(V_{1}^{-} - V_{1}^{+}) = 0, \quad I_{in} + \left(\frac{sC_{2} + G_{o2}}{2}\right)(V_{2}^{-} - V_{2}^{+}) + G_{m2}(V_{1}^{+} - V_{1}^{-}) = 0$$

$$Y = \frac{I_{in}}{V_{2}^{+} - V_{2}^{-}} = s\frac{C_{2}}{2} + \frac{G_{o2}}{2} + \frac{G_{o2}}{2} + \frac{1}{s\left(\frac{C_{1}}{2G_{m1}G_{m2}}\right) + \frac{G_{o1}}{2G_{m1}G_{m2}}}$$

$$R_p = \frac{2}{G_{o2}}, \qquad C_p = \frac{C_2}{2}, \qquad R_s = \frac{G_{o1}/2}{G_{m1}G_{m2}}, \qquad L = \frac{C_1/2}{G_{m1}G_{m2}}.$$

Characterization of Active Inductors

□ Frequency Range

•A lossy gyrator-C active inductor, however, only exhibits an inductive characteristic over a specific frequency range. This frequency range can be obtained by examining the impedance of the RLC equivalent circuit of the lossy active inductor

$$Z = \left(\frac{R_s}{C_p L}\right) \frac{s\frac{L}{R_s} + 1}{s^2 + s\left(\frac{1}{R_p C_p} + \frac{R_s}{L}\right) + \frac{R_p + R_s}{R_p C_p L}}.$$
$$\omega_p = \sqrt{\frac{R_p + R_s}{R_p C_p L}}.$$
$$R_p \gg R_s,$$
$$\omega_p \approx \sqrt{\frac{1}{L C_p}} = \omega_o,$$
$$\omega_z = \frac{R_s}{L} = \frac{G_{o1}}{C_1}$$

Instantaneous Quality Factor

•The quality factor Q of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle

$$Q = 2\pi \times \frac{\text{Net magnetic energy stored}}{\text{Energy dissipated in one oscillation cycle}}.$$

•For a linear inductor, the complex power of the active inductor is obtained from

$$P(j\omega) = I(j\omega)V^*(j\omega) = \Re e[Z]|I(j\omega)|^2 + j\Im m[Z]|I(j\omega)|^2,$$

•The first term quantifies the net energy loss arising from the parasitic resistances of the inductor, whereas the second term measures the magnetic energy stored in the inductor

$$Q = \frac{\Im m[Z]}{\Re e[Z]}.$$

•Active inductors are linear when the swing of the voltages / currents of the inductors are small and all transistors of the active inductors are properly biased.

•The quality factor of a lossy gyrator-C active inductor can be derived directly

$$Q = \left(\frac{\omega L}{R_s}\right) \frac{R_p}{R_p + R_s \left[1 + \left(\frac{\omega L}{R_s}\right)^2\right]} \left[1 - \frac{R_s^2 C_p}{L} - \omega^2 L C_p\right]$$

Example: $R_s = 4\Omega$, $R_p = 1k\Omega$, $C_p = 140$ fF, and L = 1.6 nH

•Q1-the quality factor of the active inductor at low frequencies

•Q2-the effect of the finite output impedance of deep sub-micron MOSFETs

•It is seen that Q1 dominates the quality of the active inductor and is therefore widely used to quantify the quality factor of active inductors.

•To boost the quality factor of active inductors, Rs must be minimized. Four approaches can be used to reduce Rs:

•Approach 1:

$$R_s = \frac{G_{o1}}{G_{m1}G_{m2}}, \qquad R_s \downarrow \Rightarrow G_{01} \downarrow$$

Approach 2 :

•Rs can be lowered by increasing Gm1 and Gm2 directly.

•Since the transconductances of the transconductors are directly proportional to the dc biasing currents and the width of the transistors of the transconductors, Rs can be lowered by either increasing the dc biasing currents or increasing the transistor width.

•The former, however, increases the static power consumption of the active inductors whereas the latter lowers the self-resonant frequency of the active inductors.

•Another downside of this approach is that the inductance of the inductors L will also be affected.

Approach 3 :

•Reduce Go1 using advanced circuit techniques, such as cascodes.

•Cascodes are effective in lowering the output conductance and can be used here to reduce Go1.

| Transconductor | Min. V _{DD} | Output impedance |
|-------------------------|----------------------|---|
| Basic | $2V_{sat}$ | $G_o = \frac{1}{r_o}$ |
| Cascode | $3V_{sat}$ | $G_o = rac{1}{r_{o1}(r_{o2}g_{m2})}$ |
| Regulated cascode | $2V_T + V_{sat}$ | $G_o = \frac{1}{r_{o1}(r_{o2}g_{m2})(r_{o3}g_{m3})}$ |
| Multi-regulated cascode | $2V_T + V_{sat}$ | $G_o = \frac{1}{r_{o1}(r_{o2}g_{m2})(r_{o3}g_{m3})(r_{o4}g_{m4})}.$ |

Approach 4 :

•Use a shunt negative resistor at the output of the positive transconductor to cancel out the parasitic resistances, both series and parallel, of active inductors.

•In this case, a negative resistor of resistance $R_{comp} = -R_{total}$ can be connected in parallel with Cp to eliminate the effect of both Rp and Rs of the active inductor simultaneously.

•Note that the resistance of the negative resistor should be made tunable such that a total cancellation can be achieved.

•The quality factor of the compensated active inductor at ω_o is given by

$$Q(\omega_o) = (R_p || \hat{R}_p || R_{comp}) \sqrt{\frac{C_p + C_{comp}}{\hat{L}}},$$

•It should be noted that because Rs and Rp are frequency-dependent, Rcomp should be designed in such a way that a total resistance cancellation is achieved across the frequency range of the active inductor.

•It should also be noted that although the negative resistor compensation technique is widely used to improve the quality factor of spiral inductors, a total compensation in this case is difficult to achieve.

•This is because an active negative resistor is used to cancel out the largely skin-effect induced parasitic series resistance of spirals.

•Average Quality Factors

$$Q(\omega) = \frac{\omega_o}{2} \frac{\partial \phi(\omega)}{\partial \omega},$$

where $\varphi(\omega)$ is the phase of the tank impedance.

•The quality factor of a passive LC tank at a given frequency is independent of the current of the tank.

•Unlike passive LC tanks, the inductance of the active inductors varies with the current / voltage of the inductors. The effective quality factor defined as

$$\overline{Q(\omega)} = \frac{\omega}{2(I_{max} - I_{min})} \int_{I_{min}}^{I_{max}} Q(\omega, i) di,$$

where Imin and Imax are the minimum and maximum currents of the transconductors of active inductors, and $Q(\omega o, i)$ is the instantaneous quality factor at frequency ω and channel current i provides an effective mean to quantify the quality factor of active inductors, especially when active inductors are employed in circuits that are operated in a large-signal mode, such as LC tank oscillators.

Noise

•Active inductors exhibit a high level of noise as compared with their spiral counterparts.

•By assuming Vn1 and Vn2 are uncorrelated, we arrive at

 $\overline{V_n^2} = \overline{V_{n1}^2},$ $\overline{I_n^2} = \left| G_{o2} + j\omega C_2 \right|^2 \overline{V_{n1}^2} + G_{m2}^2 \overline{V_{n2}^2}.$

Linearity

•The preceding development of gyrator-C active inductors assumes that the transconductors of the active inductors are linear.

•This assumption is only valid if the swing of the input voltage of the transconductors is small.

•When the voltage swing is large, the transconductors will exhibit a nonlinear characteristic and the synthesized active inductors are no longer linear.

•The linearity constraint of active inductors sets the maximum swing of the voltage of the active inductors.

If we assume that the transconductances of the transistors of gyrator-C active inductors are constant when the transistors are biased in the saturation, then the maximum swing of the voltage of the active inductors can be estimated from the pinch-off condition of the transistors.
When the transistors of active inductors enter the triode region, the transconductances of the

transistors decrease from *gm* (*saturation*) *to gds* (*triode*) in a nonlinear fashion.

□ Stability

•Gyrator-C active inductors are negative feedback systems. The stability of active inductors is critical to the overall stability of systems employing active inductors.

$$Z = \frac{sC_1 + G_{o1}}{s^2 C_1 C_2 + s(C_1 + C_2) + G_{m1} G_{m2}},$$
$$p_{1,2} = \frac{C_1 + C_2}{2C_1 C_2} \left[-1 \pm \sqrt{1 - \frac{4C_1 C_2 G_{m1} G_{m2}}{(C_1 + C_2)^2}} \right]$$

•The poles of the gyrator-C active inductor are located in the left half of the s-plane and the gyrator-C active inductor is a stable system

•The degree of stability can be assessed by evaluating its damping factor, which is obtained by comparing the denominator with the standard form of the characteristic equation of second-order systems

$$s^{2} + 2\omega_{o}\xi s + \omega_{o}^{2} = 0,$$

$$\xi = \frac{1}{2\sqrt{G_{m1}G_{m2}}} \left(\sqrt{\frac{C_{2}}{C_{1}}} + \sqrt{\frac{C_{1}}{C_{2}}}\right).$$

•If C1 = C2 = C and Gm1 = Gm2 = Gm, we have

$$p_{1,2} = \frac{1}{C} \left(-1 \pm \sqrt{1 - G_m^2} \right),$$
$$\xi = \frac{1}{G_m}.$$

•An increase of Gm will lead to a decrease of ξ . This is echoed with a reduced level of damping.

•Because Re[p1,2] = -1/C, the absolute stability margin is set by the capacitance C and is independent of Gm.

•It should be noted that the preceding analysis is based on the assumption that active inductors are 2nd-order systems.

•When the parasitics of MOSFETs are accounted for, active inductors are no longer 2nd-order systems and their stability will deteriorate.

□ Supply Voltage Sensitivity

$$S_{V_{DD}}^{L} = \frac{V_{DD}}{L} \frac{\partial L}{\partial V_{DD}}.$$

$$L = \frac{C}{G_{m1}G_{m2}} \qquad \qquad \frac{\partial L}{\partial V_{DD}} = -L\left(\frac{1}{G_{m1}}\frac{\partial L}{G_{m1}} + \frac{1}{G_{m2}}\frac{\partial L}{G_{m2}}\right)$$

The normalized supply voltage sensitivity

$$S_{V_{DD}}^{L} = -\left(S_{V_{DD}}^{G_{m1}} + S_{V_{DD}}^{G_{m2}}\right)$$

Parameter Sensitivity

•The minimum feature size of MOS devices in modern CMOS technologies has been scaled down more aggressively as compared with the improvement in process tolerance such that the effect of process variation on the characteristics of circuits becomes increasingly critical.

•For example, the resistance of poly resistors in a typical $0.18\mu m$ CMOS process has an error of $\pm 20\%$ approximately and that of n-well resistors has an error of $\pm 30\%$ approximately.

•The normalized sensitivity of the inductance of an active inductor to a parameter *xj of the* inductor defined as

$$S_{x_j}^L = \frac{x_j}{L} \frac{\partial L}{\partial x_j}$$

•By assuming that the parameters of the active inductor are Gaussian distributed and uncorrelated, the overall effect of the variation of the parameters of the active inductor on the inductance of the inductor is obtained from

$$\sigma_L^2 = \sum_{j=1}^N \left(\frac{\partial L}{\partial x_j}\right)^2 \sigma_{x_j}^2$$

•For a gyrator-C active inductor:

•There are two ways in which circuit designers can analyze the effect of parameter spread on the inductance of active inductors, namely worst-case analysis, also known as corner analysis, and Monte Carlo analysis

•The former determines the inductance of active inductors at process corners while the latter quantifies the degree of the spread of the inductance of active inductors around the nominal inductance of the inductors.

•The accuracy of Monte Carlo analysis increases with an increase in the number of simulation runs and is therefore extremely time consuming.

•Corner analysis, on the other hand, is time-efficient but the results obtained from corner analysis are typically over conservative.

•Despite of this, corner analysis is the most widely used method to quantify the effect of process spread.

□Signal Sensitivity

•When an active inductor is used in applications where the voltage of the active inductor experiences a large degree of variation, such as active inductor LC oscillators, the transconductances of the transconductors of the active inductor vary with the signal swing. As a result, the inductance, parasitic resistances, and quality factor of the active inductor all vary with the signal swing.

Power Consumption

•Spiral inductors do not consume static power. Gyrator-C active inductors, however, consume dc power, mainly due to the dc biasing currents of their transconductors.

•The power consumption of gyrator-C active inductors themselves is usually not of a critical concern because the inductance of these inductors is inversely proportional to the transconductances of the transconductors constituting the inductors.

Basic Gyrator-C Active Inductors

$$Q \approx \frac{R_p}{\omega L} = \frac{\omega_{t2}}{\omega} \qquad \omega_{tj} = \frac{g_{mj}}{C_{gsj}}, i = 1, 2$$
SRF:
$$\omega_o \approx \frac{1}{\sqrt{LC_p}} = \sqrt{\omega_{t1}\omega_{t2}}, \qquad Q(\omega_o) = \sqrt{\frac{\omega_{t2}}{\omega_{t1}}}.$$

•The frequency of the zero of the active inductor, which is the lower bound of the frequency range of the active inductor

$$\omega_z = \frac{g_{o1}}{C_{gs2}}.$$

•In order to maximize the frequency range of the active inductor, ω_z should be minimized. This can be achieved by reducing g_{o1} or increasing C_{gs2} . The former is usually preferred as the latter lowers ω_o .

•Because the output impedance of deep sub-micron MOSFETs is small. The detrimental effect of Rp = 1/gm1, on the quality factor of the active inductor can not be neglected. The effect of Rp, however, can be eliminated by connecting a negative resistor of resistance $Rp^{\circ} = -Rp$ in parallel with Rp. •Single-ended negative impedance networks:

•Differential negative impedance networks

•Minimum supply voltage:

| Active inductor | Fig.2.27(a) | Fig.2.27(b) |
|--|---|---|
| Max. input voltage Min. input voltage Min. V _{DD} | $V_{DD} - V_T - V_{sat}$ V_{sat} $V_T + 2V_{sat}$ | $V_{DD} - V_T - V_{sat}$ V_T $2V_T + V_{sat}$ |

Wu Current-Reuse Active Inductors

•The quality factor of Wu active inductors can be estimated by neglecting the effect of Rs and only focusing on Rp as Rp is small

 $\omega_o = \sqrt{\omega_{t1}\omega_{t2}}, \qquad Q(\omega_o) \approx \sqrt{\frac{\omega_{t2}}{\omega_{t1}}}.$

$$Q \approx \frac{R_p}{\omega L} = \frac{\omega_{t2}}{\omega}.$$

•At the self-resonant frequency

•It is seen from the preceding analysis that to increase ωo , both ω_{t1} and ω_{t2} need to be increased.

•Increasing ω_{t1} , however, lowers Q(ωo). Increasing ω_{t1} should therefore be avoided.

•To boost ω_{t2} without increasing ω_{t1} , the dc biasing current of M1 is kept unchanged while that of M2 is increased by injecting an additional current J2 into M2.

•The additional current source J2 is used to boost the transconductance of M2 such that the upper frequency bound can be increased without lowering the quality factor.

In practical design, *J2* is provided by the stage preceding to the inductors and the active inductors are known as Wu current-reuse active inductors

Lin-Payne Active Inductors

Ngow-Thanachayanont Active Inductors

Hara Active Inductors

 $(a)\,nMOS$

SRF:
$$\omega_o = \sqrt{\frac{g_m}{RC_{gs}C_{gd}}} = \sqrt{\omega_t \omega_z}, \quad \omega_z = \frac{1}{RC_{gd}}, \quad \omega_t = \frac{g_m}{C_{gs}}$$

$$R_{s} = \frac{g_{m} + \omega^{2} C_{gs}^{2} R}{g_{m}^{2} + \omega^{2} C_{gs}^{2}} \qquad \qquad L = \frac{C_{gs}(g_{m}R - 1)}{g_{m}^{2} + \omega^{2} C_{gs}^{2}} \qquad \qquad g_{m}R > 1$$

$$g_m R \gg 1. \qquad R_s = \frac{\frac{1}{g_m} + \left(\frac{\omega}{\omega_t}\right)^2 R}{1 + \left(\frac{\omega}{\omega_t}\right)^2} \approx \frac{1}{g_m} \qquad L = \frac{R}{\omega_t \left[1 + \left(\frac{\omega}{\omega_t}\right)^2\right]} \approx \frac{R}{\omega_t}$$
$$L = F(R)$$

TSMC 0.18u:

✓ Dependence of Z of nMOS Hara active inductors on the width of the transistor. W is varied from 5µm to 25µm with step 5µm, R = 1kΩ. DC biasing current 0.5mA.

Dependence of Z of nMOS Hara active inductors on R. R is varied from 0.5 k Ω to 2.5 k Ω with step 0.5 k Ω , W = 10 μ m. DC biasing current 0.5mA.

Wu Folded Active Inductors

$$Y_{in} = \frac{sC_{gs} + g_m}{sRC_{gs} + 1} = \frac{1}{R} + \frac{1}{\frac{RC_{gs}}{g_m - \frac{1}{R}} + \frac{1}{\frac{1}{g_m - \frac{1}{R}}}}$$

$$R_p = R \qquad L = \frac{RC_{gs}}{g_m - \frac{1}{R}} \qquad R_s = \frac{1}{g_m - \frac{1}{R}}$$

Careto-Castro Active Inductors

Hsiao Feedback Resistance Cascode Active Inductors

$$\begin{split} C_p &= C_{gs3}, \\ R_p &= \frac{R_f g_{o2} + 1}{2g_{o2} + R_f g_{o2}^2}, \\ R_s &= \frac{g_{m1} g_{o2} g_{o3} + \omega^2 [g_{m2} C_{gs1}^2 - g_{m1} C_{gs1} C_{gs2} (R_f g_{o2} + 1)]}{g_{m1}^2 g_{m2} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2}, \\ L &= \frac{g_{m1} g_{m2} C_{gs1} + \omega^2 C_{gs1}^2 C_{gs2} (R_f g_{o2} + 1)}{g_{m1}^2 g_{m2} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2}. \end{split}$$

 $C_p = C_{gs3},$

$$R_p \approx \frac{1}{g_{o2}},$$

$$R_s \approx \frac{g_{o2}g_{o3}}{g_{m1}g_{m2}g_{m3}},$$

$$L = \frac{C_{gs2}}{g_{m1}g_{m2}}.$$

*****Active Inductors with Low Supply-Voltage Sensitivity

•Simplified schematic of Wu current reuse active inductor (nMOS) with replica biasing

Implementation of Differential Active Inductors

$$Z = \frac{2[s(C_{gs1} + C_{gs3}) - g_{m1} + g_{ds5}]}{g_{ds5}[g_{m1} + g_{m3} + s(C_{gs1} + C_{gs3})]}.$$

$$R_p = \frac{2}{g_{ds5}},$$

$$R_s = \frac{2(g_{ds5} - g_{m1})}{g_{ds5}(2g_{m1} + g_{m3} - g_{ds5})},$$

$$L = \frac{2(C_{gs1} + C_{gs3})}{g_{ds5}(2g_{m1} + g_{m3} - g_{ds5})}.$$

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Class AB Active Inductors

 $V_T + V_{sat} \leq v_{in} \leq V_{DD} - (V_T + V_{sat}),$

Configuration of Bandpass Filters with Active Inductors

•The tuning of the center frequency of the bandpass filters is attained by varying the inductance of the active inductor while the quality factor is adjusted by varying the resistance of the compensating negative resistor.

•The output buffer provides both an adequate driving current and a matching output impedance to the load. The output buffer must also have a large bandwidth so that its impact on the performance of the filter is minimum. Source-follower configurations are typically used in realization of the output buffer due to their low and tunable output impedance and large bandwidth.

•Wu Bandpass Filters

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•Simplified schematic of Wu fully differential active inductor bandpass filter

OSCILLATORS WITH ACTIVE INDUCTORS

Ring OscillatorsWith Active Inductors

Voltage-controlled ring oscillators offer many attractive advantages over their LC counterparts including full compatibility with standard CMOS processes, a large frequency tuning range, a large number of complementary phases, a low level of power consumption, and a low silicon consumption.
The stringent timing jitter constraint of high-speed data communications require that these ring oscillators be configured in a fully differential way such that the common-mode noise generated

•The output voltage of ring VCOs should be designed to have fast rising and falling edges such that the transition window during which circuit noise contributes the most to the timing jitter of the oscillators is minimized.

- 1. Bias the active load transistors M3,4 in the triode region by keeping V_{c2} low and control their resistance by varying the gate voltage V_{c2} .
- 2. Because M3,4 behaves as voltage-controlled resistors only when they are in the triode, the swing of the output voltage of the delay cell must be kept small.
- 3. This can be achieved by keeping the number of the delay stages small such that $v_{SD3,4} < V_{sat}$.
- 4. A key advantage of this approach is that the total current drawn by the delay cell from the power supply is constant and is set by the tail current source. As a result, the switching noise generated by the delay cell is minimized.
- 5. Bias the active load transistors M3,4 in the saturation and control their channel currents by varying the gate voltage V_{c2} . Similar to the case in which M3,4 are in the triode, the total current drawn by the delay cell is constant and is set by the tail current source.
- 6. Vary the gate voltage V_{c1} of the tail transistor M5. Because $g_{m1,2}$ vary with V_{c1} in this case, the delay of the delay stage experiences a large variation, echoed with a large frequency tuning range.

•The delay of the preceding source-coupled delay cell is set by the *RC time* constant of the output nodes.

•To further reduce the delay, active inductors can be used to replace the active loads of the delay cell, as shown in the next Figure where Hara active inductors are used as the loads of the delay cell .

•The time constant of the output nodes of the delay cell is now determined by the RLC networks at the output nodes.

•In addition to the time constant reduction obtained from the inductive peaking, the added Hara active inductors further improve the performance of the delay cell in the following aspects :

 \checkmark Although Hara active inductors employ two transistors with the pMOS transistor biased in the triode and behaving as a voltage-controlled resistor, only the nMOS transistor of the active inductors is connected to the output nodes of the delay cell. As a result, the output capacitance of the delay cell is approximately the same as that of the delay cell with the active loads.

✓ The low impedance looking into Hara active inductors given by 1/gm5,6 lowers the time constant of the output nodes of the delay cell from $\tau_o \approx C_o(r_{o1,2}||r_{o3,4})$ to $\tau_o \approx \frac{C_o}{\tau_o}$

✓ A nMOS-latch formed by M7,8 can also be employed to further improve the performance of the delay cell

•Approach 1 - Vary the gate voltage of M3,4. Because M3,4 are in the triode and behave as voltage-controlled resistors, a change of Vc2 will change the resistance of the resistor of Hara active inductors.
•Approach 2 - Vary the gate voltage of the tail biasing transistor M9. A large frequency tuning range can be obtained in this way. As pointed out earlier that a downside of this approach is that the total current by the delay cell injected to the ground rail and drawn from the power supply is no longer constant. This is echoed with an increase in the switching noise generated by the delay cell.

•Schematic of source-coupled ring VCO delay with Hara active inductor loads and a pull-up pMOS latch.

Cross-Coupled Ring VCOs

•A main drawback of the preceding source-coupled delay cells is the need for a biasing tail current source.

•The flicker noise of the tail current source of the delay stage of a ring oscillator will be up-converted to the vicinity of the oscillation frequency of the ring oscillator, deteriorating the phase noise of the oscillator.

•Also, the output voltage swing of the oscillator is limited by the voltage drop across the tail current source.

•The cross-coupled delay cell shown in the enxt Figure removes the need for a tail biasing current source. It operates in a full rail-to-rail swing mode.

•Frequency tuning is achieved by varying V_c that controls $r_{ds3,4}$ when M3,4 are in the triode or $i_{DS3,4}$ when M3,4 are in the saturation.

•A drawback of cross-coupled ring VCOs is waveform asymmetry.

•As shown the rise time of the cross-coupled VCOs varies with the control voltage while the fall time remains unchanged.

•As a result, the duty cycle of the waveform varies with the control voltage.

•Another drawback is the timing-varying current injected into the ground rail, increasing the level of switching noise.

•To reduce the time delay of the cross-coupled delay cells, the active loads can be replaced with Hara active inductor loads.

•Schematic of cross-coupled ring VCO delay cell with Hara active inductor loads and a pull-down nMOS latch.

•Schematic of cross-coupled ring VCO delay cell with Hara active inductor loads and a pull-up pMOS latch.

✓ Simulated output voltage of a 4-stage cross-coupled ring VCO with Hara active inductor loads.

•It is seen that the oscillation frequency of the VCO with Hara active inductor loads is approximately twice that of the VCO with the resistor loads.

•The loss of the swing of the output voltage of the VCO with Hara active inductor loads is also evident

✓ Simulated output voltage of a 4-stage cross-coupled ring VCO with resistor loads

•Simulated output voltage of a 4-stage cross-coupled ring VCO with Hara active inductor loads and a pull-up pMOS latch

•It is observed that the swing of the output voltage of the VCO is rail-to-rail. Also, the added pMOSlatch improves the slew rate of the output voltage, reflected by the increased time duration of the Logic-0 and Logic-1 stages of the output voltage.

LC VCOs with Wu Current-Reuse Active Inductors

The silicon area of the VCO implemented in a 0.35μm 3V CMOS technology was only 100μm×120μm.
Frequency tuning range of the VCO was from 100 MHz to 900 MHz with phase noise of approximately -95 dBc/Hz at 500 kHz frequency offset.

•The high level of the phase noise is mainly due to the use of the active inductors and the tail current source of the negative resistor.

•Note that the phase noise can be improved by removing the tail current source of the negative resistor with the downside that the resistance of the negative resistor will not be variable.