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A CMOS Voltage Comparator with Rail-to-Rail Input-Range

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Abstract. A simple new continuous-time CMOS comparator circuit with rail-to-rail input common-mode range and rail-to-rail output is presented. This design uses parallel complementary decision paths to accommodate power-supply-valued inputs. The 2 decision results are combined at a current summing node, converted to a voltage, and buffered to drive voltage loads. The circuit has been realized in an area of 416 μm × 221 μm in a MOSIS 2-micron CMOS technology. Average delay of about 63 ns has been measured at 3 V (1.3 mA), and about 89 ns at 5 V (1.1 mA).

Key Words: CMOS continuous-time voltage comparator, rail-to-rail input range

Introduction

The reliability of an electronic system realized as a VLSI chip can be greatly enhanced by the inclusion of redundant subcircuit blocks that can replace one that malfunctions [1]. This approach has been successfully used in many digital circuits; DRAM, for example. Switching replacement subcircuits into a digital system is straightforward. Redundant amplifiers have been used in analog products in which the replaceable function is not used continuously [e.g. 2]. During the off-line period in which the signal path of the analog function is not in use, the analog subcircuit in the signal path may be replaced with its redundant subcircuit substitute with no disruption of service. However, when the signal path and thus the analog subcircuit is in use continuously, replacement with a substitute subcircuit without disruption of the signal path and without the introduction of switching noise is much more difficult. In our companion paper [3] is described a new generally applicable design approach for improving the yield, reliability, accuracy, and testability of analog ICs by the direct self-calibration and built-in self-test (BIST) of off-line replacement (redundant) subcircuits for an analog function block, and the commutation of replacement subcircuits into the active signal path without disruption of the analog functionality or the analog signal path. The commutation scheme connects the replacement subcircuit in parallel with the replaced subcircuit before its removal. The commutation control signal switching edge is carefully designed to minimize ''clock'' feedthrough noise. Although individual parts of this scheme have been used or proposed, we present [3] the first successful combination of these features into a useful design approach for analog VLSI system maintenance. This approach is applicable to any moderately complex analog function. Depending on the system requirements, various degrees of this design approach can be implemented to achieve desired performance improvement. The cost is a moderate die area increase. In [3], the CMOS operational amplifier is the function used for demonstration of this design approach. Experimental measurements confirm its advantages.

Important in this chip maintenance design approach is the capability for direct self-calibration and BIST of off-line replacement subcircuits. A library of analog and digital function blocks for test support were developed for use in this design scheme. Given that the signals involved in BIST usually originate on-chip and thus usually lie within well defined ranges of values, these test support cells do not require the level of protection at the signal terminals common on standard products. Thus, these test function cells may sometimes be simplified. Continuous-time analog comparators are required for the BIST capabilities provided with this design scheme. Two standard comparator cells that resolve inputs at opposite power supply rails may be

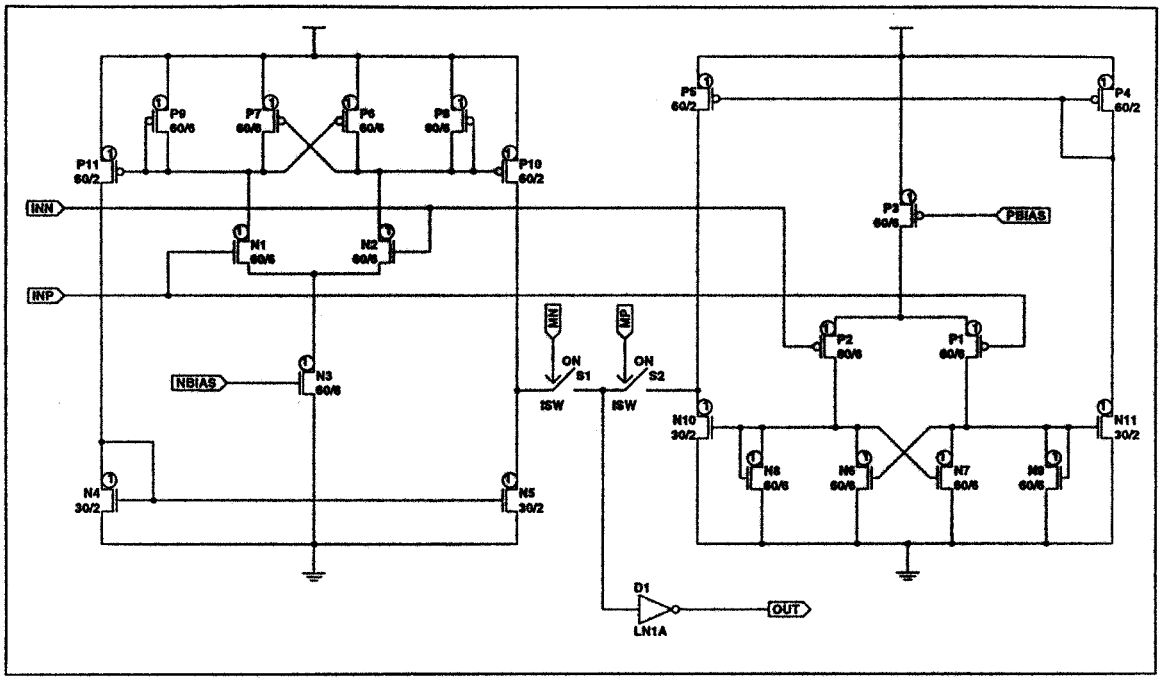

Fig. 1. Comparator schematic.

coalesced to provide a new realization of the rail-to-rail input common-mode range CMOS voltage comparator.

In this paper is presented a simple new continuous-time CMOS comparator circuit with rail-to-rail input common-mode range. This design uses parallel complementary decision paths to accommodate power-supply-valued inputs. The two decision results are combined at a current summing node, converted to a voltage, and buffered to drive voltage loads. The circuit has been realized in an area of 416 μm $\times$ 221 μm in a MOSIS 2-micron CMOS technology. Average delay of about 63 ns has been measured at 3 V (1.3 mA), and about 89 ns at 5 V (1.1 mA).

Comparator Circuit Operation

The full supply, rail-to-rail, common-mode input range of this simple new CMOS comparator is achieved by paralleling two complementary 2-stage continuous-time comparators; one with NMOS and one with PMOS differential input pairs. The second stage outputs of these two individual comparators are combined to drive a CMOS inverter third gain stage. The schematic of this new comparator is shown in Fig. 1. Device sizes are shown in Table 1. The common-mode input range of each comparator's first stage is limited to roughly one transistor V_t plus two $V_{ds,sat}$ away from the respective power supply but includes the other supply voltage. Coalescing comparators with complementary input stages, we create a combined

Table 1. Comparator device sizes.

Device	W/L (μm)	Device	W/L (μm)
N1	60/6	N2	60/6
N3	60/6	N4	30/2
N5	30/2	N6	60/2
N7	60/6	N8	60/6
N9	60/6	N10	30/2
N11	30/2	P1	60/6
P2	60/6	P3	60/6
P4	60/2	P5	60/2
P6	60/6	P7	60/2
P8	60/6	P9	60/6
P10	60/2	P11	60/2

comparator with full supply-to-supply common-mode input range. The basic topology of the first and second stages of each comparator is identical to the other except their transistor types are complemented.

The input source-coupled pair (N1-N2, P1-P2) is loaded by diode-connected transistors (P8-P9, N8-N9) and cross-coupled feedback transistors (P6-P7, N6-N7) of the same size. The purpose of this cross-coupled feedback is to effectively cancel out the 1st-stage load transistor output resistance and thus increase first stage voltage gain. One first-stage differential voltage output is used directly to drive a transistor (P10, N10) of the common-source second-stage amplifier. The other first stage output voltage is converted into current and then back to voltage through a current mirror (P11, N11) with diode-connected transistor load (N4, P4). The resultant voltage is then used to drive a second-stage common-source transistor (N5, P5) that is in a push-pull arrangement with P10, N10. Without DC loading, the large-signal behavior of the first two gain stages can be viewed as a differential voltage-to-current converter when all related transistors are biased in the forward saturation region. Thus, each of the two second-stage output points (MN, MP) can be viewed as a current summing node. The currents at node MN-MP combine and drive the third-stage, a CMOS inverter gain stage, shown as INV on the schematic, that provides further voltage gain and the drive capability for this combined comparator. The output may swing from rail-to-rail for small current loads. In the schematic, switches labeled S1 and S2, which are normally shorted, are included in prototype test ICs to allow independent characterization of the half-comparators.

When the input common-mode voltage is too close to a supply voltage to provide proper bias for one of the input stages, its biasing current is reduced and its load transistors are forced into the sub-threshold region. When this happens, the second stage current is effectively reduced to zero, as is the differential current. At the current merging point, the other comparator's output, its differential output current, is not affected. Thus, the combined comparator can still function properly because of the 2 parallel decision paths. Within the extremes of the input range, both of the merged comparators are biased properly, output differential currents add to provide additional output drive. Due to input DC offset differences, current contention at this merged point is possible. That is, the two sections of the merged comparator may try to drive this merging node with differential currents of different polarity. With the merged comparator sections biased with identical currents, in the worst case, the differential current will cancel out each other. This contention can and will exist for a small differential input range during merging-node transients, and contribute to slightly increased delay times and slightly reduced accuracy.

This comparator and its bias generation circuits were fabricated in MOSIS 2-micron pwell and nwell CMOS technologies. Comparator layout is shown in Fig. 2. The comparator is 416 μm $\times$ 221 μm.

Comparator Circuit Performance

Simulated comparator performance with $V_{DD} = 5$ V and switching voltage overdrive of ± 8 mV is summarized in Table 2. Observing the propagation delay results when the common-mode input value is near one of the power supply voltages, the first, second and last data rows, the combined comparator propagation delay is slightly slower than just one properly biased half-comparator driving the current merging node alone. This speed degradation is due to the extra loading presented by the non-functioning half of the combined comparator. When the combined comparator is properly biased, such as when the common-mode inputs are 2 and 3 volts, the combined output is slightly faster than each of the comparator halves. These observations agreed well with our analysis.

The delays observed for the 4-volt common-mode input row of Table 2 are interesting. The PMOS-input-only half-comparator became very slow under this

Table 2. Summary of simulation results.

Comparator	Merged		P-input only		N-input only	
Common-mode (volts)	t_{Phl} (ns)	t_{Phl}	t_{Phl} (ns)	t_{Phl}	t_{Phl} (ns)	t_{Phl}
0	49.9	55.4	47.9	53.6	—	—
1	61.7	59.2	48.5	55.1	—	—
2	41.9	42.1	46.6	51.6	47.8	43.3
3	46.0	41.8	49.9	53.5	54.2	41.6
4	57.8	46.2	134.8	138.1	52.5	38.9
5	52.0	34.2	—	—	48.3	33.3

$V_{DD} = 5$ V, Switching voltage overdrive ± 8 mV

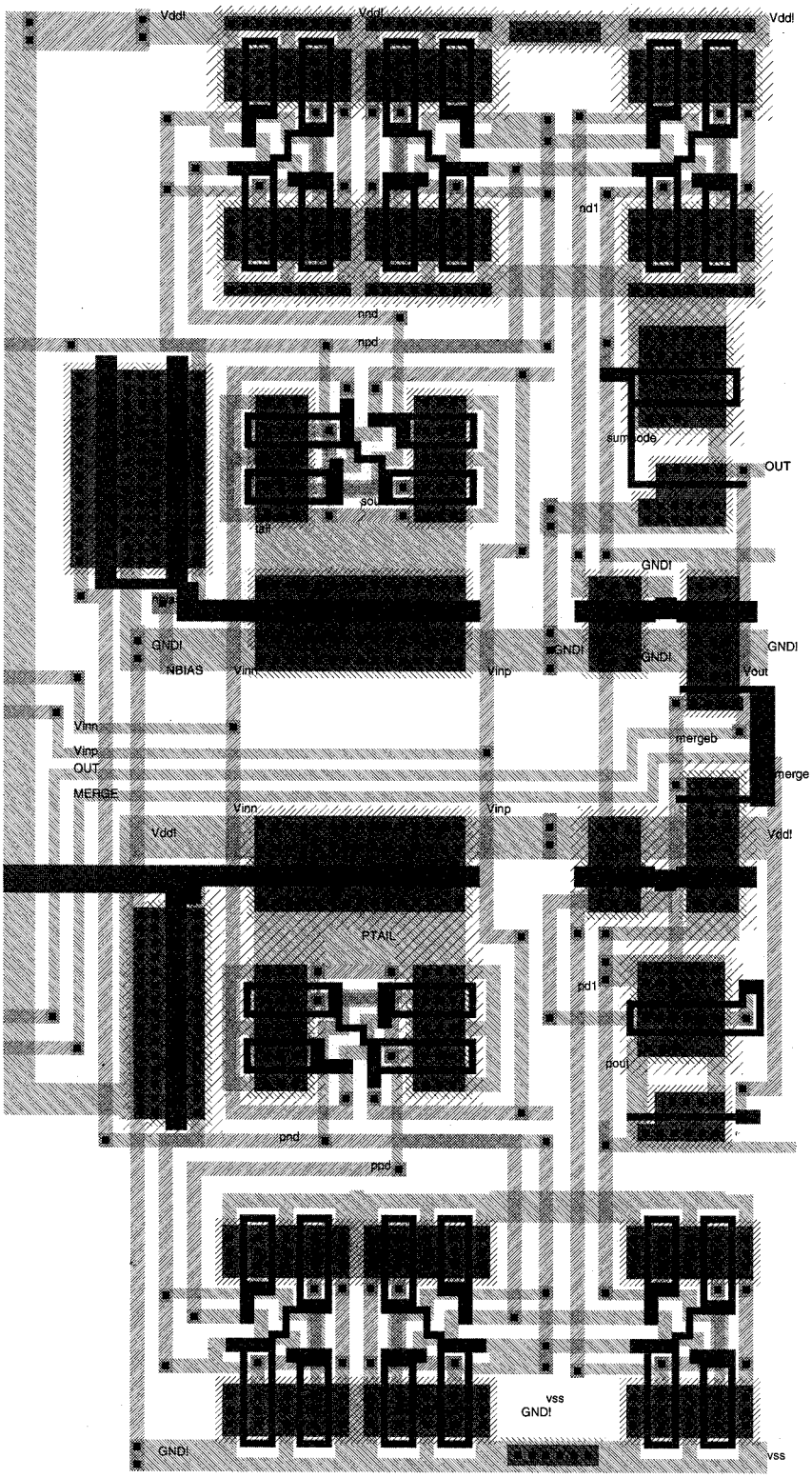

Fig. 2. Comparator layout.

common-mode condition and the merged comparator is slower than the NMOS-input-only implementation. The slowing of the PMOS-input-only half-comparator is caused by its input stage transistors which are biased in the linear region. Thus, the bias currents are much smaller than the nominal design value, producing the longer propagation delay. The slowing of the merged comparator can be explained as caused by the contention problem discussed earlier. While the NMOS-input half-comparator changed output differential current polarity, the differential output current polarity of the PMOS-input half-comparator has not changed, thus reducing the combined differential output current.

Prototype circuits realized in 2-micron nwell and pwell CMOS technologies have been characterized. Experimental data taken from 2-micron nwell technology prototypes given in Table 3 for power supply values of 3 and 5 volts and switching voltage overdrive of $\pm$ 8 mV show the same trend and current contention effects observed in the simulations. Delays of between 54 and 282 ns and supply currents of between 0.5 and 1.3 mA have been measured.

Conclusion

In this paper is presented a simple new continuous-time CMOS comparator circuit with rail-to-rail input common-mode range and a rail-to-rail output. This design uses parallel complementary decision paths to accommodate power-supply-valued inputs. The two decision results are combined at a current summing node, converted to a voltage, and buffered with a CMOS inverter stage to drive voltage loads. The circuit has been realized in an area of 416 μm $\times$ 221 μm in a MOSIS 2-micron CMOS technology. Average delay of about 63 ns has been measured at 3 V (1.3 mA), and about 89 ns at 5 V (1.1 mA). Rail-to-rail input range capability is important in analog BIST. This new comparator circuit can provide this capability in a modest area with good accuracy and good speed.

Table 3. Experimental data (2-micron, nwell).

V_{DD} (volts)	V_{CM} (volts)	t_{Phl} (ns)	t_{Plh} (ns)	I_{DD}(max) (mA)
3	0	282	60	0.52
	1	134	80	1.0
	2	56	70	1.3
	3	36	54	1.3
5	0	104	110	1.0
	1	144	135	1.1
	2	93	86	1.2
	3	92	86	1.1
	4	121	112	1.1
	5	111	100	1.0

Switching voltage overdrive $\pm$ 8 mV

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