Continuous-Time Sigma–Delta Modulator With an Embedded Pulsewidth Modulation

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***Abstract*—A new Continuous-Time (CT) sigma–delta modulator (SDM) based on the well-known asynchronous SDM is proposed in this paper. To this end, the flash quantizer and the digital-to-analog converter (DAC) in a multibit (MB) CT-SDM clocked at a rate $f_{\max}$ are replaced by a single-bit (SB) comparator with hysteresis clocked at a higher rate f_s and a SB-DAC, respectively. By proper selection of the hysteresis in the comparator and the ratio $F = f_s/f_{\max}$, the performances of both modulators are shown to be equivalent. The comparator with hysteresis and the loop filter produce, in the modulator output, a limit cycle of frequency $f_{\max}$ which is modulated by the input signal. Therefore, the modulator output can be considered to be a pulsewidth (PW) modulated signal with a frequency approximately equal to $f_{\max}$, and the proposed modulator is called a PW-SDM. Despite the high sampling rate of the comparator output, the integrators and the SB-DAC of the proposed modulator have the same speed requirements as those of the equivalent conventional MB-SDM. On the other hand, in the proposed modulator there are not MB (analog-to-digital or digital-to-analog) converters. Therefore, for a given set of specifications, the proposed PW-SDM is expected to consume less power and area than its equivalent conventional MB modulator.**

***Index Terms*—Analog-digital conversion, continuous-time (CT) sigma–delta modulators (SDMs), low-power SDMs, multibit (MB)-SDMs, oversampling data converters, pulsewidth (PW) modulators.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADCs) based on sigma–delta (SD) modulation have been traditionally used in low frequency applications such as instrumentation or audio systems. Nevertheless, present wired and wireless communication systems demand resolutions greater than 12 bits with a signal bandwidth of several megahertz. Fortunately, recent advances in CMOS technology allow to achieve a high frequency operation so that SD modulators (SDMs) are being used in the design of high-speed transceivers. Discrete-time (DT) or continuous-time (CT) SDMs can be implemented using switched-capacitor or CT filtering, respectively [1], [2]. The integrators in DT-SDMs require several time constants to settle, imposing severe bandwidth requirements to the amplifiers. Therefore, CT-SDMs are preferred for large bandwidth applications as they can be clocked at a higher data rate [3].

In order to achieve a high resolution in a large signal bandwidth, low oversampling ratios (OSRs) in high-order or MB modulators are required. Single-bit (SB) high-order modulators have been extensively used in the past due to their inherent linearity and simplicity. The stability problems of high-order modulators can be alleviated using multibit (MB) quantizers. Despite their higher complexity, MB-SDMs can implement more aggressive noise transfer functions (NTFs) than their SB counterpart. On the other hand, MB modulators require a flash quantizer in the forward path, and a MB digital-to-analog converter (DAC) in the feedback path whose linearity is required to be as good as that of the whole modulator. In practice, some kind of trimming or dynamic element matching (DEM) [4]–[6] has to be used, which further increases the complexity of the MB modulator.

Apart from SD modulation, other schemes, such as pulsewidth (PW) modulation, have been used for power converters [7] and class-D amplifiers [8]. The well-known asynchronous SDM in Fig. 1(a) generates a PW modulated signal using the structure of a SDM where the DAC and the sampler have been removed and the flash quantizer has been replaced by a comparator with hysteresis. In Fig. 1, w_1 is the integrator unity-gain frequency. Although the asynchronous SDM has been used to implement a class-D power amplifier for audio applications [9], it cannot be applied for data conversion due to the lack of sampling.

In this paper a new modulator called PW-SDM is proposed for data conversion. To this purpose, the MB flash quantizer in the forward path of a CT-SDM clocked at the rate $f_{\max}$ [Fig. 1(b)] is replaced by a SB comparator with hysteresis clocked at the rate f_s, where f_s is greater than $f_{\max}$ (Fig. 1(c)). With a proper design both modulators have similar performances.

The output $y(t)$ of the proposed modulator is a binary signal and the DAC in its feedback path is SB. SB-DACs are inherently linear so that no trimming or DEM technique is required. Like in an asynchronous SDM, the presence of a comparator with hysteresis in the proposed modulator produces a limit cycle in its output, whose frequency (with a proper design) is approximately equal to $f_{\max}$. Therefore, the modulator output is a square waveform whose frequency $f_{\max}$ is modulated by the modulator input so that its mean value is approximately equal to the instantaneous value of the input signal. In spite of the higher frequency rate of the comparator, the integrators in the proposed modulator can be shown to have the same speed requirements as those of its equivalent conventional MB-SDM. Note that in both architectures the unity-gain frequency of the integrators has the same value w_1. Furthermore, the complexity of the m-bit flash quantizer (2^m-1 comparators) in the MB-SDM is much greater than the complexity of a single comparator with hysteresis.

Authors would like to remark that this is not the first time an asynchronous SDM has been used for data conversion. In [10]

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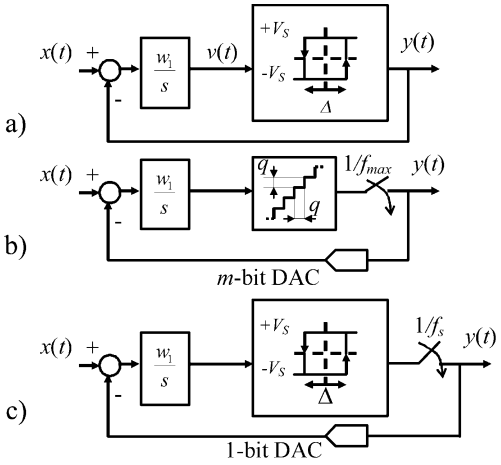

Fig. 1. (a) Asynchronous SDM. (b) CT MB-SDM. (c) Proposed PW-SDM.

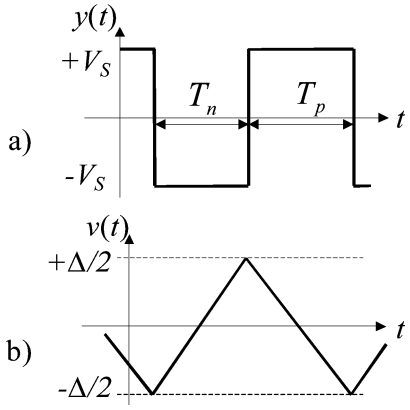

Fig. 2. Asynchronous SDM waveforms. (a) Comparator output. (b) Integrator output.

a sampler was placed outside the SD loop leading to an architecture which is rather different to a PW-SDM. In the authors knowledge, only in [11] the sampler was placed inside the loop, so that it can be considered to be the first PW-SDM. However, in [11] a complex poly-phase implementation of the sampler was proposed and the potential for this architecture to favourably replace MB SD modulators was not understood. This potential was addressed for the first time in [12], where the first implementation of a PW-SDM was presented (using discrete components). In parallel to this work, Ouzounov *et al.* reported an innovative research showing that the PW-SDM is a SDM operating at a limit cycle, and studying the properties of this limit-cycle [13]. Also in [13] it is shown that a hysteresis in the comparator is not strictly necessary to produce a limit cycle in high-order loops, although the presence of hysteresis allows a good control of the limit-cycle frequency.

II. Asynchronous SDM

The asynchronous SDM in Fig. 1(a) is briefly reviewed in this section. For the sake of simplicity a first-order architecture is considered. Analytical results can be easily obtained when the input signal is a dc value $x(t) = X$. A more comprehensive study of this architecture can be found in [10]. Assuming the system to be stable with a well defined solution, the waveforms at the outputs of the integrator $v(t)$ and modulator $y(t)$ are depicted in Fig. 2. The signal $v(t)$ is a triangular signal with a rising slope of $w_1 \cdot (X + V_S)$ and a falling slope of $w_1 \cdot (X - V_S)$. The rectangular wave $y(t)$ takes the value V_S during a time interval T_p, and the value $-V_S$ during a time interval T_n, with

$$T_p = \frac{\Delta}{w_1 \cdot (V_S - X)} \text{ and } T_n = \frac{\Delta}{w_1 \cdot (V_S + X)}. \quad (1)$$

The frequency at the comparator output is given by

$$f(X) = \frac{1}{T_p + T_n} = \frac{w_1}{2} \cdot \frac{V_S^2 - X^2}{\Delta \cdot V_S} \quad (2)$$

and its maximum value is

$$f_{\max} = f(0) = \frac{1}{T_{\min}} = \frac{w_1}{2} \cdot \frac{V_S}{\Delta}. \quad (3)$$

The mean value of $y(t)$ is given by

$$\bar{y} = V_S \cdot \frac{T_p - T_n}{T_p + T_n} = X. \quad (4)$$

The output $y(t)$ is a binary signal and the information is contained in the time intervals T_p and T_n. Since there is no sampling, in the ideal case, T_p and T_n have infinite resolution, so that the input dc value X can be extracted without error from $y(t)$ using a low-pass filter. This result can be extended to a slowly varying input signal $x(t)$. In this case, a low-pass filter can extract $x(t)$ from $y(t)$ with a high accuracy. For instance, if $x(t)$ is a low frequency sinusoidal signal, the signal $y(t)$ will be only corrupted by (usually a small amount of) harmonic distortion [10]. Note that quantization does indeed take place. The nonlinearity, however, does not spread the energy as it is does in a SD loop, and hence the quantization effects manifest themselves as discrete spurs.

III. Proposed PW-SDM

In order to apply the asynchronous SDM of the Fig. 1(a) to data conversion, a sampler and a feedback DAC are required, [10], [11]. The resulting modulator, called a PW-SDM, uses a single sampler (operated at a high frequency f_s) placed inside the loop, as depicted in Fig. 1(c) [12]. In the proposed PW-SDM the error produced by the sampling process is shaped by the modulator NTF. Like the modulators in [10] and [11] [but unlike the asynchronous SDM in Fig. 1(a)], the input signal cannot be extracted from the output signal without error (even more, in the ideal case with a dc input signal in an irrational relationship with V_s, there will be a nonperiodic limit cycle. Due to the sampler in Fig. 1(c), the time intervals T_p and T_n have now a finite resolution, as $T_p = p \cdot T_s$ and $T_n = r \cdot T_s$ are integer multiples of the sampling period $T_s = 1/f_s$ [Fig. 3(a)].

In order to make the analysis of the proposed PW-SDM in Fig. 1(c) tractable, two simplifying assumptions are made. Firstly, the sampling frequency is assumed to be large when compared to the value $f_{\max}$ given in (3) (i.e., $f_s \gg f_{\max}$). Note that the PW-SDM becomes the asynchronous modulator when $f_s \to \infty$. Secondly, the amplitude of the slowly varying input signal is assumed to be small when compared to V_S (i.e., $|x(t)| \ll V_S$). This second condition is held for a wide range of

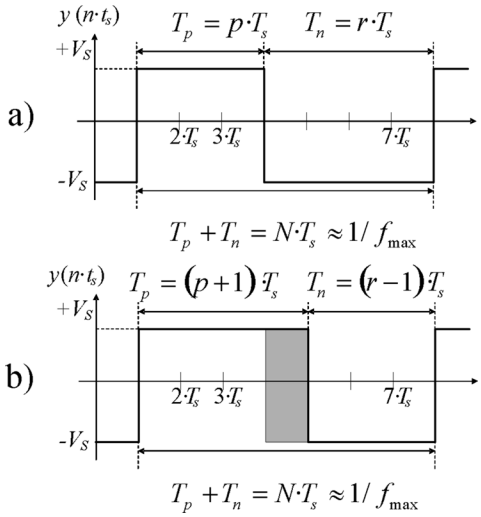

Fig. 3. PW-SDM output showing two successive quantization steps.

modulator inputs. Under these conditions it can be shown that the modulator output frequency is approximately constant and equal to $f_{\max}$ (i.e., $T_p + T_n \approx T = 1/f_{\max}$). In the same way, the sum of the integer numbers p and r (denoted by N) is approximately constant. Due to sampling, a quantization error has to be added to (4), so that the mean value of $y(t)$ over a period T is now the instantaneous value of $x(t)$ plus a quantization error.

The mean value of $y(t)$ is the difference between the areas in the time intervals with the positive and negative amplitudes of the rectangular output signal. The minimum output amplitude resolution q_{out} is proportional to twice the area of one time slot T_s [shaded area in Fig. 3(b)]

$$\begin{aligned} q_{\text{out}} &= \min\{|V_S \cdot p \cdot T_s - V_S \cdot r \cdot T_s|/(1/f_{\max})\} \\ &= V_S \cdot T_s \cdot f_{\max} \cdot \min\{|p - r|\} \\ &= \frac{2 \cdot V_S \cdot f_{\max}}{f_s} = \frac{V_S}{\Delta} \cdot \frac{w_1 \cdot V_S}{f_s}. \end{aligned} \tag{5}$$

One unit increment in the integer number p (reciprocally, one unit decrement in r) corresponds to a change in the comparator input given by:

$$q_{\text{in}} = w_1 \cdot V_S \cdot T_s = \frac{w_1 \cdot V_S}{f_s} \tag{6}$$

Therefore, the PW-SDM in Fig. 1(c) is equivalent to a conventional CT-SDM clocked at the rate $f_{\max}$, with an output quantization step q_{out} and a separation of the input threshold levels q_{in}. A modulator with this type of quantizer achieves the same SNR as a conventional modulator [Fig. 1(b)] with a unity-gain quantizer and a quantization step given by

$$q = q_{\text{in}} = \frac{w_1 \cdot V_S}{f_s}. \tag{7}$$

Although this result has been obtained under a set of simplistic assumptions, it has been also shown by simulation results and by experimental measurements obtained from a prototype built using commercial components. Furthermore, the same equivalence can be extended to high-order modulators. Some of these results will be presented in the forthcoming sections.

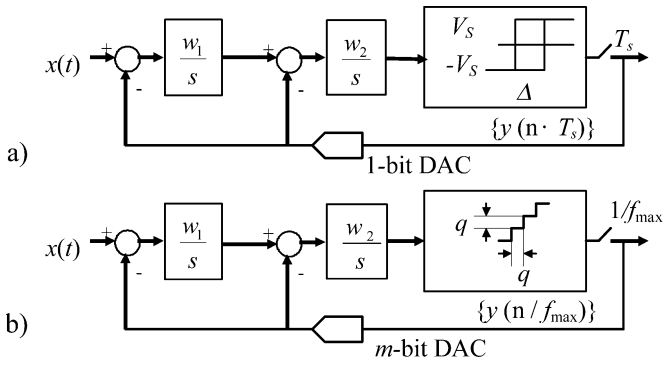

Fig. 4. (a) Second-order PW-SDM. (b) Its equivalent MB modulator.

IV. Second-Order PW SDM

A. Architecture

The proposed second-order PW-SDM modulator is shown in Fig. 4(a), where w_1 and w_2 are the unity-gain frequencies of integrators 1 and 2, respectively. The equivalent asynchronous SDM can be obtained from this modulator by removing the DAC and the sampler. When a zero input signal ($x(t) = 0$) is used (see Appendix) the asynchronous modulator can be shown to produce a limit cycle with a frequency

$$f_{\max} = \frac{w_2}{2} \cdot \frac{V_S}{\Delta} \tag{8}$$

Extending the results obtained in the last section to the second-order case, under the same assumptions, the proposed PW-SDM is equivalent to the conventional MB-SDM in Fig. 4(b) with sampling frequency $f_{\max}$ and quantization step (referred to a full scale $2V_S$)

$$q = \frac{w_2 \cdot V_S}{f_s}. \tag{9}$$

The signal-to-noise ratio (SNR) is given by the well-known expression for the MB-SDM [1], replacing the quantization q by the expression (9)

$$\text{SNR} = \frac{60}{\pi^4} \cdot \underbrace{\frac{w_1^2 \cdot w_2^2}{f_{\max}^4}}_{\text{Integrator gains}} \cdot \frac{A^2}{2} \cdot \underbrace{\left(\frac{f_S}{V_S \cdot w_2}\right)^2}_{1/q^2} \cdot \text{OSR}^5. \tag{10}$$

In order to show the equivalence between both architectures the following parameters have been chosen: $w_1 = 32 \cdot 10^6$ rad/s, $w_2 = 64 \cdot 10^6$ rad/s, $V_S = 1$ V and $\Delta = 1$ V. As a consequence, $f_{\max} = 32$ MHz. Let us define the oversampling factor of the proposed PW-SDM as $F = f_s/f_{\max}$, and let us define the OSR in the usual way as $\text{OSR} = f_{\max}/(2 \cdot f_b)$, where f_b is the bandwidth of the input signal $x(t)$.

The power-spectral density (PSD) of both modulators is depicted in Fig. 5 for $F = 8 (f_s = 256\,\text{MHz})$ and $\text{OSR} = 16 (f_b = 1\,\text{MHz})$. The quantization step of the equivalent MB modulator is $q = 0.25$ V (referred to a full scale of 2 V) leading to a m-bit DAC in Fig. 4(b) with $m = 3$. The input amplitude has been chosen to be -10 dB over the full scale $\pm V_S$. As it can be seen, both modulators have a similar output spectrum inside

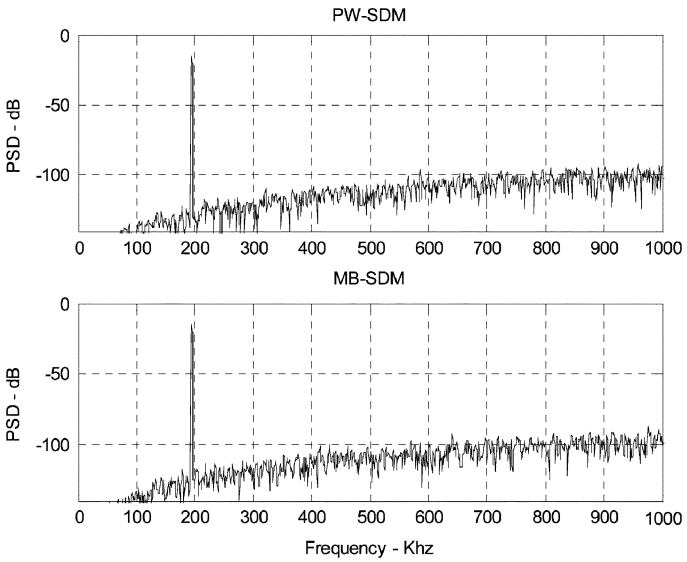

Fig. 5. PSD of the proposed PW-SDM and its equivalent MB-SDM for an input amplitude of -10 dB.

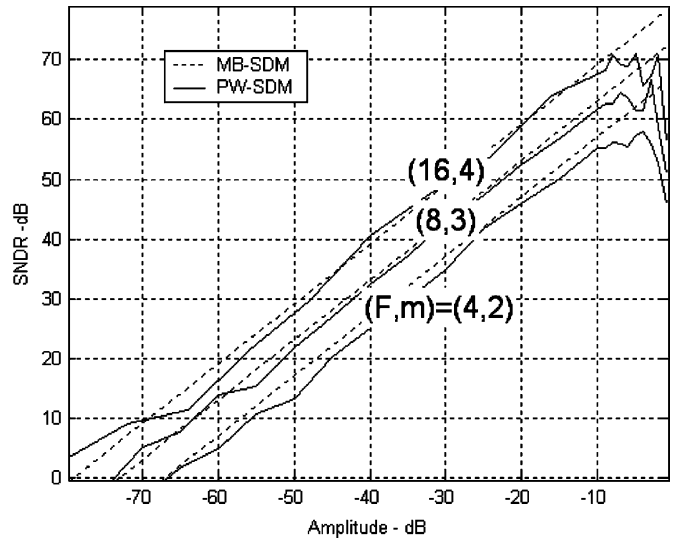

Fig. 6. SNDR versus input signal amplitude for the second-order PW-SDM (obtained from simulation and shown in solid line) and the equivalent conventional m-bit modulator (obtained from expression (10) and shown in dashed line) for different values of the oversampling factor F (and corresponding number of bits m).

the signal bandwidth. Due to sampling, the output signal $y(t)$ is corrupted by quantization noise but the harmonic distortion typical of asynchronous modulators [10] is not observed here, as the quantization noise has a dithering effect.

The signal-to-(noise plus distortion) ratio (SNDR) of the proposed PW-SDM (solid line) is shown in Fig. 6 for different values of the oversampling factor F and a signal frequency of 195.3 kHz. The theoretical SNR of the equivalent MB modulator, computed from expression (10), is also shown (dashed line). As it was expected, both families of curves reasonably match, especially for large values of F.

One interesting feature of the PW-SDM is that doubling the sampling frequency f_s (i.e., doubling F) the SNDR increases by 6 dB as shown in Fig. 6. This property is common to sampled-data modulators, because the NTF is scaled by the same factor as the sampling frequency. Nevertheless, the NTF in CT-SDMs does not depend on the sampling frequency, as it only depends on the unity-gain frequency of the integrators (w_1 and w_2 in Fig. 4), the feedback coefficients (1 in this case) and the waveform at the DAC output. This property can be used as an additional degree of freedom in the design of ADCs for multi-standard receivers.

Finally, the digital filter at the modulator output operates with a SB input at the high clock rate f_S in the PW-SDM case, and with a m -bit input at a low clock rate $f_{\max}$ in the MB-SDM case. This could affect the power consumption of the digital filter. It will be discussed later.

B. Comparison to a Conventional SB Modulator

In order to design a SB CT-SDM with the same SNDR as the second-order PW-SDM, and the same signal bandwidth f_b, it is necessary to scale the equivalent sampling frequency $f_{\max}$ and the integrator unity gain frequencies in Fig. 4 by a factor α. Then, the SNR of the SB-SDM will be given by

$$\mathrm{SNR}_{sb} = \frac{60}{\pi^4} \cdot \frac{(\alpha^2 \cdot w_1 \cdot w_2)^2}{(\alpha \cdot f_{\max})^4} \cdot \frac{A^2}{2} \cdot \frac{1}{q_{sb}^2} \cdot (\alpha \cdot \mathrm{OSR})^5 \quad (11)$$

where $q_{sb} = 2 \cdot V_S$ is the quantization step of the SB modulator ($\mathrm{OSR} = 16$ and $f_b = 1$ MHz in the last example). The value α can be derived by equating (10) and (11)

$$\alpha = \left(\frac{2 \cdot f_s}{w_2} \right)^{2/5}. \quad (12)$$

For the above example with $F = 8, \alpha = 2.3$. Hence, the conventional single bit modulator requires integrators $\alpha = 2.3$ times faster than the proposed one to achieve the same SNR. Furthermore, this value of α has been obtained from a linear analysis, but a real implementation would require a larger value of α. Firstly, the SB-SMD is more prone to harmonic distortion than a MB modulator. Secondly, due to stability reasons, the NTF of a MB modulator can be designed to be more aggressive than that of a SB one. As a matter of fact, the modulator in Fig. 4(b) becomes unstable when the quantizer is SB.

C. Decimation Filter

It is a common practice in conventional SD ADCs to carry out the decimation process by using a multistage filter [1] as shown in Fig. 7. In the first stage the sampling rate is reduced to four times the Nyquist frequency (f_N). The aliasing produced in the M-down sampler is rejected by means of a simple nth-order *comb* filter. It has been shown elsewhere that selecting $n = (k + 1)$ trades off complexity and in-band quantization noise in the downsampled signal, where k is the order of the SDM. The last two stages consist of a Low-Pass filter with normalized cutoff frequency $\pi/2$ followed by a 2-downsampler [14]. Simulation results show that this architecture of the decimator is also convenient for the PW-SDM.

The main difference between the decimation filters of the PW-SDM-based-converter (PWC) and its equivalent MB-SDM-based-converter (MBC) is in the first stage, as shown in Fig. 7. For the example above and $F = 8$, the first stage filter

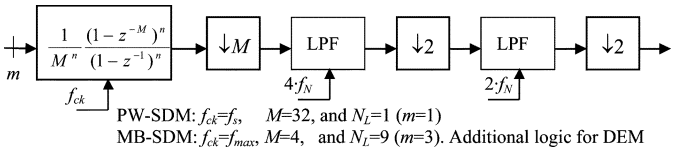

Fig. 7. Decimation filter for the PW-SDM and the MB-SDM (F = 8). The main difference is in the first stage *comb* filter.

of the PWC is clocked at the rate f_s, with a down-sampling rate of 32 and a 2-level input signal, while the first stage filter of the MBC is clocked at the rate $f_{\max} = f_s/8$, with a down-sampling rate of 4 and a 9-level input signal. The output resolution of the *comb* filter can be approximately estimated from the resolution of the input signal (given by the number of levels N_L) and the dc gain, $\log_2(M^n)+\log_2(N_L)$. This expression leads to 15 and 9 bits of output resolution for the *comb* filter of the PWC and MBC, respectively. In general, the increase of resolution (difference in the number of bits required at the output of the *comb* filters) is given by $n*\log_2(F)-\log_2(2\cdot F\cdot f_{\max}/w_{\text{last}}+1)\approx (n-1)^*\log_2(F)+\log_2(w_{\text{last}}/f_{\max})-1$, where w_{last} is the gain of the last integrator.

The required resolution at the output of the first stage filter not only influences the complexity of the *comb* filter, it also determines the complexity of the last two stages of the decimation filter. Fortunately, the electronic realization of the *comb* filter is not complex. Note that the FIR section $(1-z^{-M})^n$ can be implemented as $(1-z^{-1})^n$ at the low rate $4\cdot f_N$ and that only the recursive function has to be implemented at the higher rate by means of a cascade of accumulators. As explained in [15], there is an efficient implementation based on module arithmetic to avoid overflow in the accumulators.

Although 15 bits of resolution at the output of the first stage filter in the PWC seems to be a severe drawback, in practice it is possible to reduce this resolution without a significant degradation in the SNDR of the converter. The architecture of Fig. 7 has been simulated for the PWC modulator adding a n_b-bit quantizer at the output of the *comb* filter. In our example, the SNDR degradation, calculated as the difference between the SNDR at the modulator output minus the SNDR at the decimation filter output, is depicted in Fig. 8(a). It can be observed that 11 bits of resolution at the *comb* filter output leads to a SNDR degradation smaller than 2 dB. It could be argued that a similar conclusion could be obtained for the MBC, but this is not the case. The same simulations have been done for the MBC [Fig. 8(b)] showing that it is much more sensitive to a reduction in the resolution of the *comb*-filter output. A reduction of only 1 bit leads to a SNDR degradation larger than 15 dB.

As a conclusion, although the decimator is more complex in the PWC than in the MBC, a fair comparison between them should also take into account the complexity and power consumption in the modulator. Therefore, other penalties in the MBC should be considered, such as the MB quantization in the forward path and the linearization technique (like dynamic element matching) required in the MB DAC at the backward path. It is not easy to determine the best solution in a general case, so that the designer should select the best option in a case by case basis.

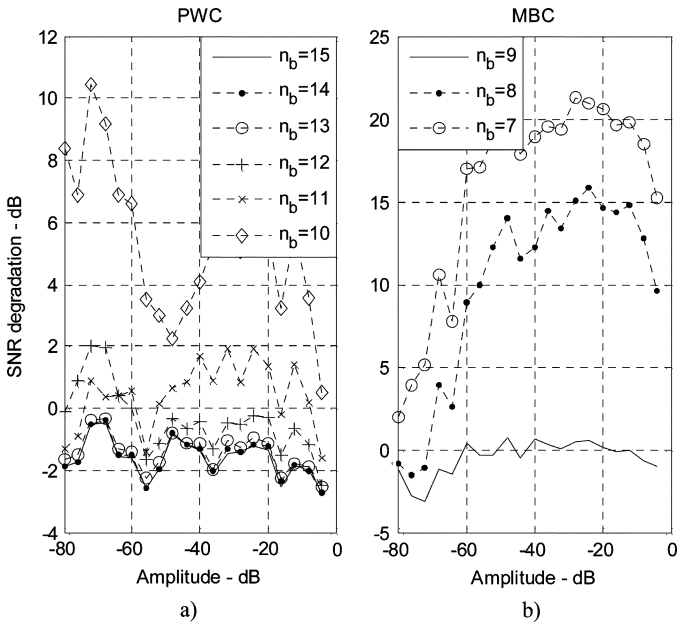

Fig. 8. SDNR degradation for different resolutions at the comb filter output (given in number of bits n_b) for: (a) PWC and (b) MBC.

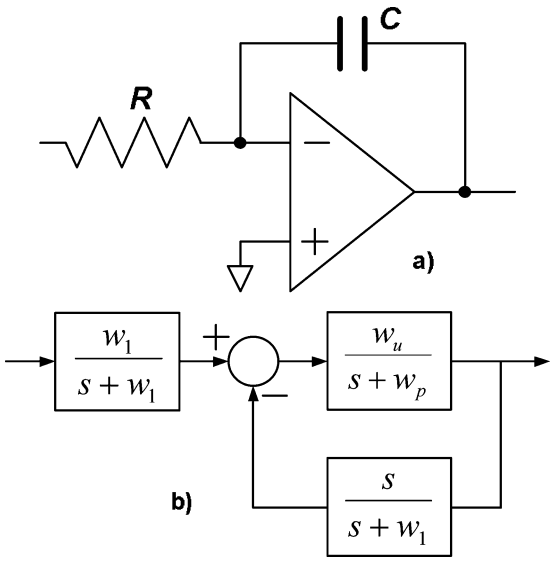

Fig. 9. (a) *RC* integrator and (b) model used in simulations.

V. Nonidealities in the PW-SDM

A. DC Gain and Gain-Bandwidth of the Amplifiers

Noise and linearity of the entire modulator are mainly determined by the first integrator. Integrator requirements decrease from the first stage to the last one because, when referred to the modulator input, any nonideality in one integrator is shaped and attenuated by the transfer function of the preceding stages. There are two main technologies to implement a CT integrator in CMOS technologies, the active *RC* and the $g_m - C$ ones [16]. In this paper, an active *RC* implementation will be considered. A similar analysis can be made for the $gm - C$ case.

The schematic of an active *RC* integrator is shown in Fig. 9(a). The model of the entire integrator is shown in Fig. 9(b) where the amplifier has been modeled as a first-order system. The parameters w_u and w_p correspond to the gain-bandwidth product

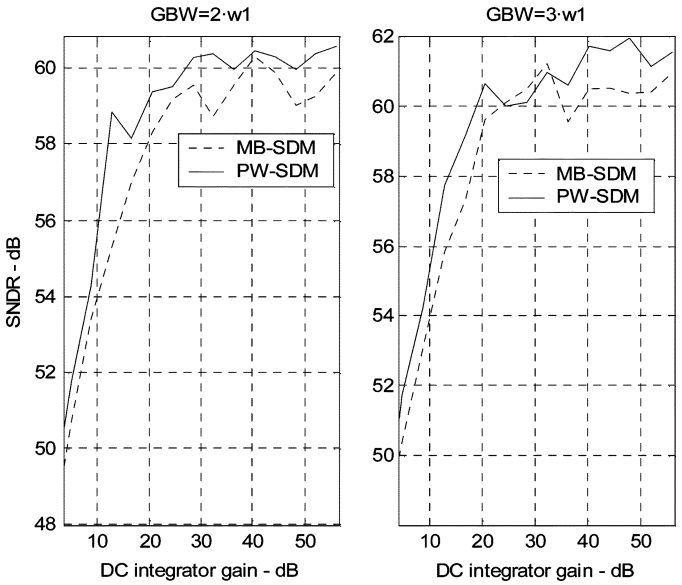

Fig. 10. SNDR of the MB-SDM and PW-SDM versus amplifier dc gain for two different values of GBW. The input amplitude is -10 dB.

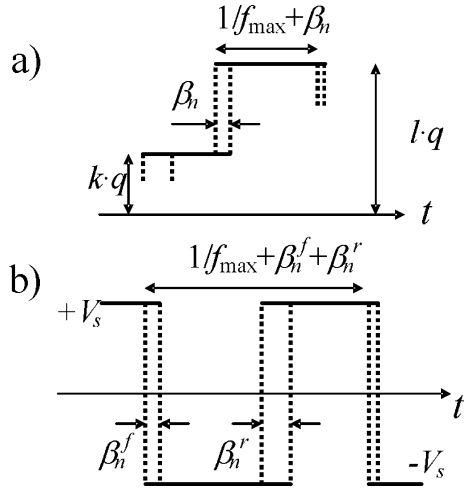

Fig. 11. Jitter effect at the DAC output for: (a) MB-SDM with quantization step q and (b) equivalent PW-SDM.

(GBW) and the -3-dB cutoff frequency of the amplifier in radians per second, respectively. The parameter w_1 is the integrator unity-gain frequency $w_1 = 1/RC$.

The integrator model has been used for the first stage of the modulators in Fig. 4. The parameters have been chosen as in Section IV-A and the oversampling factor F is equal to 8. The results are shown in Fig. 10 with solid line for the PW-SDM, and with dashed line for the equivalent MB-SDM. The SNDR is represented against the amplifier dc gain (w_u/w_p) for two different values of the GBW (w_u). The performance degradation is similar in both architectures and the same constraints (speed and dc gain) are required for the amplifiers in both modulators.

The amplifiers have to be designed with a slew-rate (SR) large enough to follow their output variations. For the modulator in Fig. 4(a), in the unfavourable case of an input signal amplitude $A_p = 0.59$ (-5 dBFS), the maximum value at the first integrator input is $V_S + A_p$. With the parameters of Section IV-A, under the assumption that the input signal frequency $f_p < f_{\max}$, the maximum change rate at the first integrator output is $w_1^*(V_S + A_p) = 50$ V/μs, which determines the minimum slew-rate for the first integrator. Regarding the second integrator, for the asynchronous case (i.e., $t_s \to 0$) the maximum value at the output of the first integrator is given by $A_p + \Delta \cdot w_1/(2 \cdot w_2)$ [see (18) in Appendix], so that the maximum change rate at the output of the second integrator is given by $w_2.[A_p + \Delta \cdot w_1/(2 \cdot w_2) + V_S] = 118$ V/μs. Assuming once again that $t_s \ll 1/f_{\max}$, this value is considered to be a good estimation for the minimum SR required to the second integrator of the modulator in Fig. 4(a). These values of Slew Rate have been shown to a produce negligible degradation in the SNDR curve, by means of simulation.

B. Clock Jitter

Jitter is due to random fluctuations in the sampling instants due to the phase noise that corrupts the system clock [17]. The amount of charge that is transferred during a sampling period exponentially decrease with the time in DT-SDM. At the end of the period almost the whole charge has been transferred and the error produced by the time deviation of the next sampling instant is very small, so that jitter is not an issue in DT-SDMs [18]. In CT-SDMs, the effects of the clock jitter at the internal ADC are significantly suppressed by the high gain of the integrators that precede it. Nevertheless, the jitter effects at the feedback DAC severely affect the performances of the modulator.

Usually the current provided by the DAC is converted into voltage by injecting charge in the integrating capacitor during the sampling period. Therefore, any deviation in the duration of the DAC pulse from its nominal value produces an error which is added to the modulator input. The error sequence for modulators with nonreturn-to-zero (NRZ) output can be represented by [18] $e(n) = [y(n) - y(n-1)] \cdot \beta_n/T$, where $y(n)$ is the digital output of the modulator, T is the nominal sampling period, and β_n is the time deviation of the nth DAC pulse edge. β_n can be considered to be an independent random variable with variance σ_β and white spectrum. As β_n is uncorrelated to $y(n)$

$$\sigma_e = \sigma_y \cdot \frac{\sigma_\beta}{T} \tag{13}$$

where σ_y is the standard deviation of $y(n) - y(n-1)$. For a sinusoidal input signal with amplitude A

$$\mathrm{SNR}_{\mathrm{jitter}} = \frac{A^2/2}{\sigma_e^2} \cdot \mathrm{OSR} = \frac{T^2 \cdot A^2}{2 \cdot \sigma_y^2 \cdot \sigma_\beta^2} \cdot \mathrm{OSR} \tag{14}$$

where $\mathrm{SNR}_{\mathrm{jitter}}$ is the SNR of a modulator when jitter is the only source of noise.

The expression in (14) is valid for the MB-SDM in Fig. 4(b) when $T = 1/f_{\max}$. Unlike the conventional modulator, in the equivalent PW-SDM two state transitions occur in the period $T = 1/f_{\max}$ (Fig. 11). Under the conditions described in Section III ($f_s \gg f_{\max}$ and $|x(t)|/V_S \approx 0$), and for small values of time deviation β_n^r and β_n^f, the time intervals T_p and T_n can be represented as $T_p = p \cdot T_s + \beta_n^r$ and $T_n = r \cdot \mathrm{T_s} + \beta_n^f$.

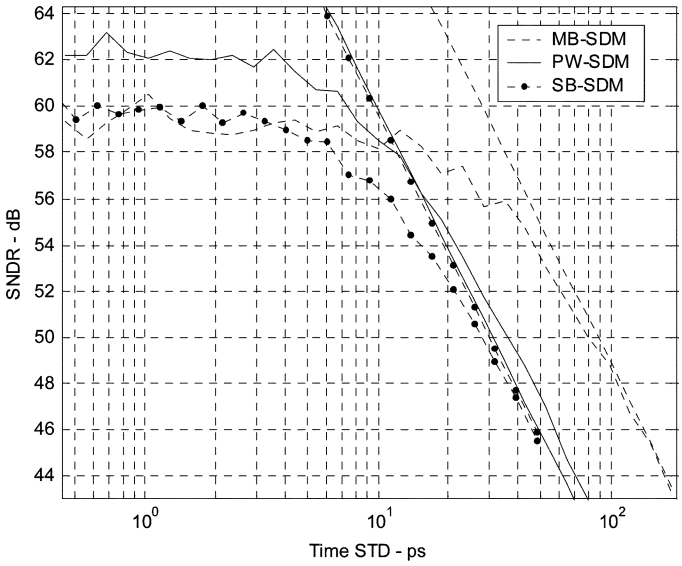

Fig. 12. SNDR versus the standard deviation of jitter (σ_β) for three modulators with an input amplitude of -10 dB. The theoretical SNR curve without quantization noise is also drawn.

The mean value of $y(t)$ in the period $1/f_{\max}$ can be shown to be

$$\bar{y} = V_S \cdot \frac{T_p - T_n}{T_p + T_n} = V_S \cdot \frac{p \cdot T_s - r \cdot T_s}{p \cdot T_s + r \cdot T_s} + V_S \cdot \frac{\beta_n^r - \beta_n^f}{p \cdot T_s + r \cdot T_s}. \quad (15)$$

The first and second terms correspond to the signal plus quantization noise and the jitter noise, respectively. The common denominator in both terms is (like in the MB-SDM case) $p \cdot T_s + r \cdot T_s \approx T = 1/f_{\max}$. As β_n^r and β_n^f are mutually uncorrelated, the effective standard deviation of the PW-SDM is given by $\sigma_{\beta,\mathrm{PW}} = 2 \cdot \sigma_\beta$. Therefore, the SNR of the PW-SDM is

$$\mathrm{SNR}_{\mathrm{jitter,PW}} = \frac{T^2 \cdot A^2}{4 \cdot \sigma_{y,\mathrm{PW}}^2 \cdot \sigma_\beta^2} \cdot \mathrm{OSR}. \quad (16)$$

Both modulators in Fig. 4 have been simulated using the models proposed in [19] and the results are shown in Fig. 12 for $F = 8$ and an input amplitude of -10 dB. The same random distribution has been chosen for β_n in both modulators. The theoretical values given in (14) and (16) have also been computed and they also shown in the figure. It can be seen that the MB modulator is more robust than the proposed one, and not only by the different factors which appear in the denominators of (14) and (16): 2 and 4, respectively. It is well known that MB modulators that use NRZ pulses in the feedback path are more robust against jitter than their SB counterpart [16]. In this particular case simulations reveal that $\sigma_y \approx V_S$ in (14) and $\sigma_{y,\mathrm{PW}} = 2 \cdot V_S$ in (16). As a consequence, in the region of Fig. 12 where the jitter dominates, the difference in the SNR of both modulators is approximately $10 \cdot \log_{10}(8) = 9$ dB.

In fact, concerning jitter, the proposed PW-SDM behaves like a SB conventional modulator with a similar SNR. As it was said above, a SB modulator with the same integrator unity-gain frequencies as in Fig. 4 is not stable. The modulator can be stabilized if w_1 is divided by two. In order to achieve a SNR similar to that of the PW-SDM is necessary to carry out a frequency scaling following the procedure described in the Subsection IV.B. In this case, the required scaling factor is greater than the value given in (12) due to the reduction in the unity-gain frequency of the first integrator. The resulting sampling frequency of the equivalent SB-SDM is approximately 3 $f_{\max}$. The new values in (14) are $T = 1/(3 \cdot f_{\max}), \mathrm{OSR} = 3 \cdot 16$, and $\sigma_y \approx 1.68 \cdot V_S$, and the expected difference in the SNR of the SB and the PW modulators is $10 \cdot \log_{10}((2 \times 4)/(3 \times 1.68^2)) = -0.25$ dB.

This SB-SDM has also been simulated in presence of jitter and the simulation and theoretical (14) results are also shown in Fig. 12.

As shown in Fig. 12, the SNDR degradation is negligible for jitter values smaller than 10 ps. Although several modulators have been reported which require a clock jitter smaller than 10 ps [21], [22], it is difficult to achieve. Low-jitter crystal oscillators or low-noise voltage controlled oscillators (VCOs) have to be used and the layout has to be carefully designed to avoid substrate coupling and jitter degradation [20].

C. DAC Pulse Weveforms

In order to study the sensitivity of the PW-SDM to DAC pulse waveforms, the DAC transitions have been modeled as exponential waveforms. The time constants are defined as τ_r and τ_f for the rising and falling edges, respectively. Simulation results are shown in Fig. 13 for $F = 8$ and $F = 16$ with a signal amplitude of -10 dB. Both time constants are chosen to be equal ($\tau_r = \tau_f = \tau$). Fig. 13 shows that the SNDR of the MB-SDM sharply drops for time constants approximately larger than $1/(8f_{\max})$ while the SNDR of the PW-SDM smoothly decreases with the time constant.

Despite both edges are symmetrical, the error depends on the output signal [3]. For instance, in a conventional modulator, the error caused by the DAC when the output consists of two consecutive pulses of the same value is different to the error caused by the DAC when there is a transition at the modulator output [Fig. 14(a)]. On the other hand, in the PW-SDM, rising and falling edges are alternately repeated within each time period with a duration approximately equal to $1/f_{\max}$ [Fig. 14(b)]. Hence, the errors caused by both edges are cancelled by the PW-modulation like the RZ technique does in a conventional modulator [3].

Nevertheless, when both edges have different time constants, the SNDR decreases at the same rate in both modulators as shown in the upper graph of Fig. 15 for $F = 8$. In fact, when the time constants are different, the errors produced by the asymmetrical edges do not fully cancel and a new effect is observed in the PW-SDM. Unlike the conventional modulator with RZ pulses where the pulses are generated at a fixed rate given by the sampling frequency of the system, the sequence of alternating rising and falling edges in the PW-SDM output is generated at a variable rate slightly different to $f_{\max}$ [Fig. 14(b)]. Because $f_{\max}$ approximately depends on the square of the input signal (2), second-order distortion is observed as shown in Fig. 16.

An interesting effect can be observed in Fig. 16. In practice, the limit cycle frequency is an integer fraction of the clock

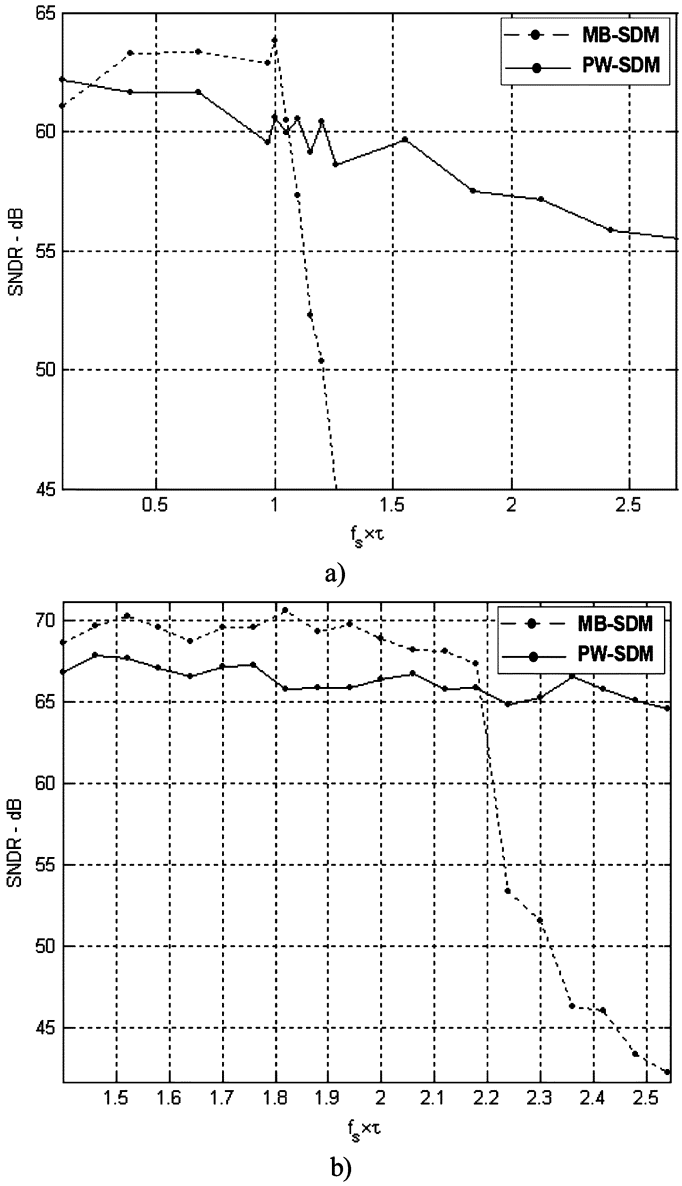

Fig. 13. SNDR degradation due to exponential (and symmetrical) rising and falling edges at the DAC output in the proposed PW-SDM and its equivalent MB-SDM. (a) $F = 8$. (b) $F = 16$.

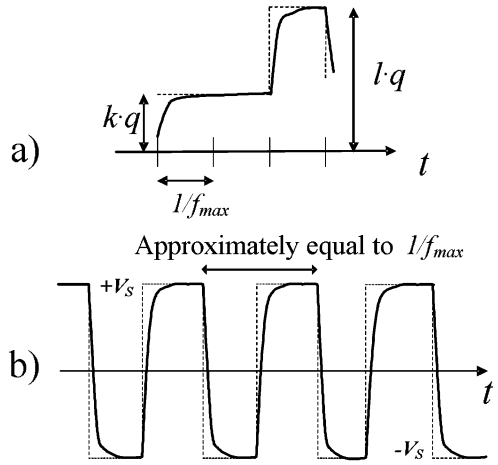

Fig. 14. DAC output waveforms in: (a) MB-SDM with NRZ pulses. (b) Proposed PW-SDM.

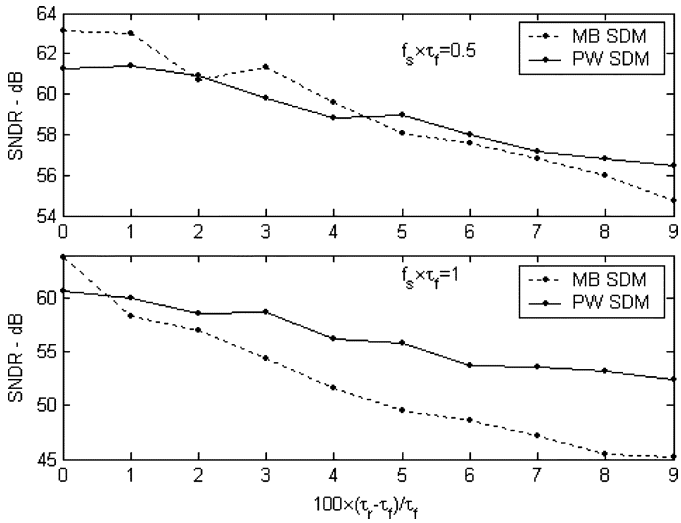

Fig. 15. SNDR degradation due to asymmetrical edges at the DAC output in the PW-SDM and its equivalent MB-SDM for deviations in the time constants around the values $\tau_f = 1/(2 \cdot f_s)$ and $\tau_f = 1/f_s$.

frequency. This limit cycle frequency can even jump between several integer fractions of the clock frequency [13]. This is for example visible for the PW-SDM by the spectral bumps in Fig. 16. However, these limit cycle frequencies are far from the signal band, so that the PW-SDM performances are not affected.

Finally, when the time constants take values in the region where the SDNR abruptly goes down in the MB-SDM with symmetrical DAC pulse edges (Fig. 13), the PW-SDM is again less prone to degradation as shown in the lower graph of Fig. 15. Fortunately, in fully differential systems, the rising and falling edges of the differential output pulses are intrinsically symmetrical [23]. Furthermore, as shown in Figs. 11 and 13, despite its higher clock rate, the DAC speed requirements in the PW-SDM are similar to those of its equivalent conventional MB-SDM.

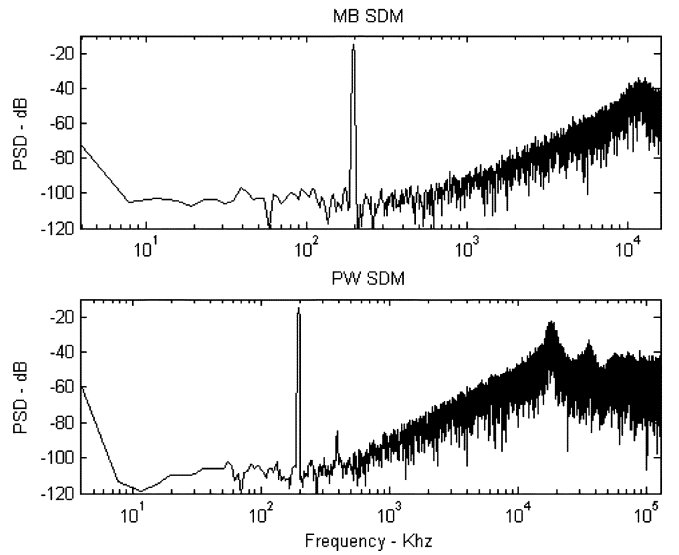

Fig. 16. PSD of the PW-SDM ant its equivalent MB-SDM for time constants around $1/(2 \cdot f_s)$ with a 3% deviation in the time constants.

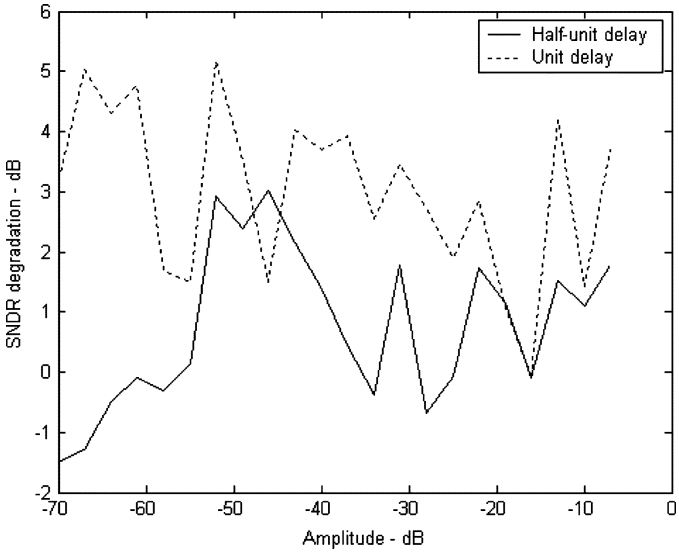

Fig. 17. SNDR degradation due to a constant delay between the internal ADC and the DAC.

D. Excess Loop Delay in the PW-SD

The response time of the internal ADC and DAC are not instantaneous. Particularly, the ADC delay is signal-dependent causing distortion. In high speed CT modulators, the sum of the ADC and DAC delays can take values comparable to the sampling period. This excess loop delay severely affects the performances of the modulator, increasing noise and distortion. In the worst case, the modulator becomes unstable. Techniques to overcome these drawbacks have been developed [24] and extensively used [16], [19], [23]. One of such techniques: 1) Places a latch between the internal ADC and the DAC in order to avoid a signal dependent delay; and 2) Draws a new feedback path from the ADC output to the quantizer input in order to maintain the performances and to guarantee the stability of the modulator. This latch can have a half-unit or a full-unit delay of the sampling frequency because it can be clocked with any of the clock edges.

In the proposed PW-SDM the modulator integrators are specified for an output frequency $f_{\max}$ despite the output clock rate f_s is much higher, as only the sampler operates at the high frequency. Hence, it is possible to place a half-unit or a full unit delay of the sampling frequency f_s, which is a small fraction of the time period $1/f_{\max}$, with negligible effects on modulator performances. For instance, when the frequency of the input signal is 195.3 kHz and $F = 8$, the SNDR degradation is shown in Fig. 17 for two cases: A half-unit and a full-unit delays between the ADC and the DAC. In the first case the SNDR degradation is never greater than 3 dB, and in the second one, never greater than 5 dB. Let us note that these results are even better for $F = 16$ and that a half-unit delay for the case $F = 8$ is equivalent to a full-unit delay for the case $F = 16$.

VI. Stability and High-Order Modulators

High-order modulators are concerned with stability problems. In order to study the robustness of the proposed PW-SDM, a third-order architecture has been designed (Fig. 18). The parameters in Table I have been chosen in order to implement an aggressive Chebyshev type II NTF with a stopband ripple of 45 dB and a stopband edge frequency of 1 MHz.

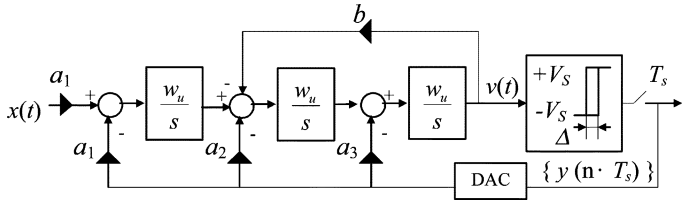

Fig. 18. Third-order PW-SDM.

TABLE I
Parameters of the Third-Order PW-SDM

Parameter	Value
a_1	0.336529
a_2	0.929472
a_3	1.363431
b	0.028915
w_u	32×10^6 rad/s
Δ	1 V
V_S	1 V

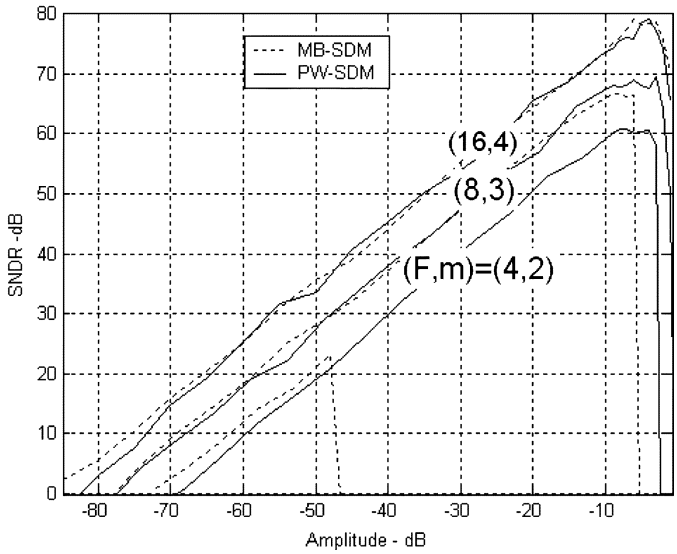

Fig. 19. SNDR curves for the third-order proposed PW-SDM (with parameters in Table I) ant its equivalent MB-SDM.

The frequency of the limit cycle in the corresponding asynchronous modulator with zero input signal can be obtained in a direct, but tedious, way (see Appendix). In this case, $f_{\max} = 21.6$ MHz $\approx a_3 \cdot w_u \cdot V_S/(2 \cdot \Delta)$ and $\mathrm{OSR} = 10.8$. The PW-SDM is equivalent to a MB-SDM with the same coefficients (Table I), sampling frequency $f_{\max}$, and quantization step $q = a_3 \cdot w_u \cdot V_S/f_s$.

Both modulators have been simulated for different values of the oversampling factor F and the results are shown in Fig. 19. For small values of F, the quantization step of the equivalent m-bit-SDM is not low enough ($q = 0.5$ for $F = 4$, and $q = 0.25$ for $F = 8$) to guarantee the stability of the MB-SDM for a wide range of amplitudes. Only for $F = 16(m = 4)$ the equivalent MB modulator becomes stable in the entire range of amplitudes.

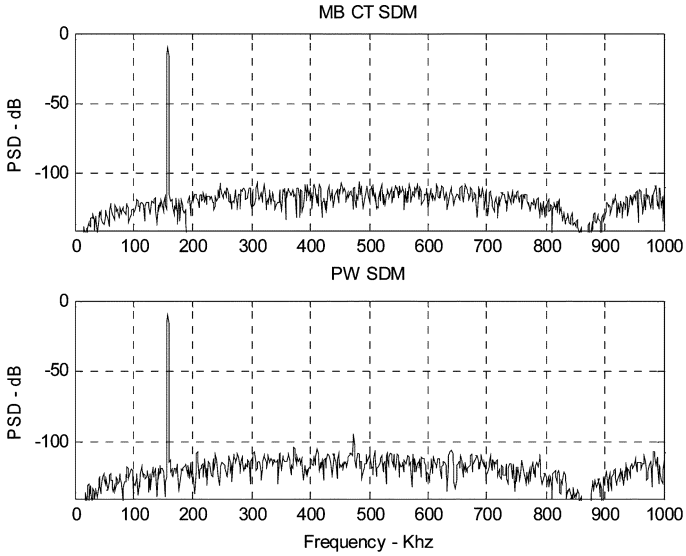

Fig. 20. Spectra of the third-order modulators $(F = 16)$.

When the MB modulator is stable, the SNDR curves of both modulators reasonably match, as it can be seen in Fig. 19. The spectra of both modulators are shown in Fig. 20 for an input amplitude of -5 dB. A third harmonic can be observed in the PW-SDM spectrum. Nevertheless, this harmonic is only visible for an input amplitude close to the full scale (-5 dB) and this harmonic does not degradate the SNDR, as shown in Fig. 19.

The better stability of the proposed modulator is due to the comparator with hysteresis and the higher output sampling rate. When the third integrator output $v(t)$ reaches the hysteresis thresholds $\pm\Delta/2$, the new state at the comparator output is quickly sampled, the DAC goes to the opposite output, and $v(t)$ is forced to change its tendency. Unlike the conventional modulator, there is an internal mechanism in the loop to stabilize the PW-SDM. Therefore, a more aggressive NTF than in the MB case can be selected.

VII. Conclusion

A new class of SDMs, called PW-SDMs, has been proposed in this paper, where the comparator in the forward loop of a conventional SDM is replaced by a comparator with hysteresis whose output is sampled at a high data rate f_s. Analytical and simulation results show that the output signal of a PW-SDM has a PW modulation with a variable frequency close to $f_{\max}(f_{\max} < f_s)$. The frequency $f_{\max}$ depends on the unity-gain frequency of the last integrator of the loop (w_{last}) and the ratio between the output level and the hysteresis of the comparator. It has been shown that the proposed PW-SDM is equivalent to a conventional MB-SDM sampled at $f_{\max}$ whose quantization step (relative to the full-scale of the MB quantizer) is given by the ratio $w_{\text{last}}/(2.f_s)$. As the frequency of the output signal in the proposed modulator is approximately constant and equal to $f_{\max}$, despite its high sampling rate, the speed requirements of its SB-DAC have been shown to be similar to those of its equivalent MB modulator. Even more, the proposed modulator has been shown to have a larger stability range and to be more robust against nonideal DAC pulses and excess loop delay than its equivalent MB-SDM. On the other hand, its digital output signal has a higher OSR and, like the conventional SB modulators, it is less robust against clock jitter. Although a high SNDR can also be obtained by simply increasing the OSR of a conventional SB-SDM, there are significant differences with the proposed PW-SDM. Analytical and simulation results show that, for a SB-SDM to provide the same SNDR as the proposed PW-SDM, it should be sampled at frequency higher than $f_{\max}$ requiring faster integrators and DAC. Besides, unlike the proposed PW-SDM, the equivalent SB-SDM suffers from stability problems and harmonic distortion tones typical of SB modulators.

Appendix

Fig. 4(a) shows the second-order version of the proposed PW-SDM. Assuming that the input signal is a dc value X and that the modulator is asynchronous (i.e., $T_s = 0$ and no DAC) with a stable and well defined output, the modulator output $y(t)$ will be a rectangular wave which takes a value V_S during T_p seconds, and a value—V_S during the rest of the period (T_n seconds). Therefore, the first integrator output $v_1(t)$ will be, once again, a triangular wave of period $T_p + T_n$. Let us note that all signals in the modulators are periodic in order to impose boundary condition in the following analysis. The second integrator output can be calculated as shown in (17), at the bottom of the page, where t_0 and t_1 are the time instants where the comparator output changes and, hence, $v_2(t_0) = \Delta/2$ and $v_2(t_1) = -\Delta/2$.

Under these conditions, the analysis of the architecture is straightforward. It can be shown that the (1)–(4) are still valid if the integrator gain w_1 is replaced by w_2. The output swing of the first integrator is

$$\begin{aligned} v_1(t_1) &= X - \frac{\Delta}{2}\cdot\frac{w_1}{w_2} \le v_1(t) \le v_1(t_0) \\ &= X + \frac{\Delta}{2}\cdot\frac{w_1}{w_2} \end{aligned} \tag{18}$$

and the output swing of the second integrator is limited by $\pm\Delta/2$. These values can be also used for a coarse estimation of the output swing of the integrators in the proposed PW-SDM.

The asynchronous third-order modulator corresponding to the architecture in Fig. 18 can be analyzed following the same procedure. Again the output waveform of the first integrator is triangular and the output of the second integrator can be

$$v_2(t) = \begin{cases} \frac{\Delta}{2} + w_2 \int_{t_0}^{t} [v_1(\tau) - V_S]d\tau, & t_0 \le t < t_0 + T_p = t_1 \\ -\frac{\Delta}{2} + w_2 \int_{t_1}^{t} [v_1(\tau) + V_S]d\tau, & t_1 \le t < t_1 + T_n = t_0 + T_p + T_n \end{cases} \tag{17}$$

calculated using (17) if coefficient b is assumed to be zero for the sake of simplicity. A new integration is necessary in order to calculate the output of the third integrator. It can be shown that the frequency of the asynchronous modulator when the input is zeroed is one of the roots of the polynomial

$$\frac{96 \cdot \Delta}{a_1 \cdot w_u^3 \cdot V_S} \cdot f_{\max}^3 - \frac{48 \cdot a_3}{a_1 \cdot w_u^2} \cdot f_{\max}^2 + 1 = 0. \tag{19}$$

The roots can be exactly calculated using numerical algorithms. However, the third term in (19) is much smaller than the rest of terms, so that

$$f_{\max} \approx \frac{a_3 \cdot w_u \cdot V_S}{2 \cdot \Delta}. \tag{20}$$

Following a reasoning similar to that of Section III, the quantization step of the equivalent third-order MB-SDM is given by expression (7) after replacing w_1 by $a_3 \cdot w_u$. The resulting quantization step is $q = a_3 \cdot w_u \cdot V_S / f_s$.

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