Multirate $\Sigma\Delta$ Modulators

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***Abstract*—New high-speed $\Sigma\Delta$ analog to digital converters (ADCs) are required for xDSL and RF receivers. As sampling frequency is upper limited by the amplifier bandwidth and power consumption, these high-speed, low-power converters operate with a small oversampling ratio. Usually, they are high-order cascade structures with a multibit quantizer in the last stage. All these approaches use a unique sampling frequency. This paper shows that multirating is a useful technique to reduce power consumption in high speed $\Sigma\Delta$ modulators. To this end, two different multirate $\Sigma\Delta$ modulators are proposed. The first one uses a low sampling frequency in the first integrator(s) of a single loop structure, while the second one uses a low oversampling frequency in the first stage(s) of a cascade converter.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS) integrated circuits, low-power electronics, $\Sigma\Delta$ modulation.**

I. Introduction

OVERSAMPLING analog-to-digital (A/D) modulators have been widely used for high-resolution applications [1]. They are suitable for very large scale integration (VLSI) signal processing because of its insensitivity to process and component variations [2]. For high performance modulators there is a tradeoff between oversampling ratio (M) and modulator order (L). First modulators used single-bit, single loop architectures with high oversampling ratio. Increasing the conversion rate may be accomplished by increasing the sampling frequency or decreasing the oversampling ratio. The sampling frequency is upper limited by the amplifier bandwidth and power consumption. Therefore, high speed low-power $\Sigma\Delta$ modulators operate with a small oversampling ratio.

High accuracy at a low oversampling ratio can be achieved either, by increasing the modulator order or by using a multibit quantizer in the oversampled loop. Single-loop high-order modulators show stability problems which can be overcome by cascading several low-order single-loop modulators. Multibit modulators offer a direct improvement over 1-bit topologies of $6b$ dB, where b is the number of bits. Besides, they alleviate the stability problems that appear in high order single-loop modulators. The major obstacle in designing multibit modulators is the high accuracy requirement on the multibit digital-to-analog converter (DAC) located in the feedback path. Several techniques have been proposed to mitigate errors caused by the feedback DAC, by using digital [3] or analog correction [4], or dynamic element matching [5].

New high performance complementary metal–oxide–semiconductor (CMOS) ADCs with high accuracy at the MS/s range are now required for xDSL and mobile terminals. For these application several $\Sigma\Delta$ modulators have been recently proposed with different topologies [6]–[11]. Usually they are high-order cascaded structures of single bit first- or second-order stages, with a multibit quantizer at the last stage of the cascade, showing that selecting the optimal modulator is a compromise between modulator order, oversampling ratio and resolution of internal quantizers.

Conventional first-order analysis shows that, for a given dynamic range (DR), power consumption of $\Sigma\Delta$ modulators does not depend on the oversampling ratio M. For switched capacitor implementations, this analysis assumes that the DR is limited by the kT/C noise of the first integrator. Increasing M has a twofold consequence on the first integrator opamp. On the one hand, the capacitor load can be decreased, as the kT/C noise is inversely proportional to M. On the other hand, the opamp has to settle faster. Both effects counteract so that power consumption does not change. Similar first-order analysis can be done for continuous-time and switched-current implementations [12].

Nevertheless, this simple analysis assumes a one-pole model of the opamp, which is only valid for low sampling frequencies. Therefore, it does not apply for new high-speed modulators, where opamps are operated near their maximum bandwidth. In that case, power consumption dramatically increases with sampling frequency because 1) parasitic capacitances become a significant fraction of the total capacitance, and 2) clock nonoverlap, and rise and fall times become a significant fraction of the clock cycle. This issue was addressed in [13], where an analysis of three different opamp topologies including first-order parasitics, showed a significant increase of the power consumption in the first integrator of a $\Sigma\Delta$ modulator for a high sampling frequency. A recent example can be seen in [7] and [10], where two $\Sigma\Delta$ modulators with similar performances were built in the same technology. The implementation in [7] used $M = 24$, while the implementation in [10] used $M = 16$, achieving more than a 70% of power saving.

Note that, concerning power consumption, only the analog portion of the modulator is considered here. To get a better estimate of the total power consumption, its digital portion should be also taken into account. Anyway, as scaling down of technologies, the contribution of the digital part to power consumption is expected to decrease.

In these approaches the oversampling ratio was unique for all the integrators. However, the use of different oversampling ratios along the structure of a $\Sigma\Delta$ modulator can alleviate some of the major problems faced in its design. As the integrators have

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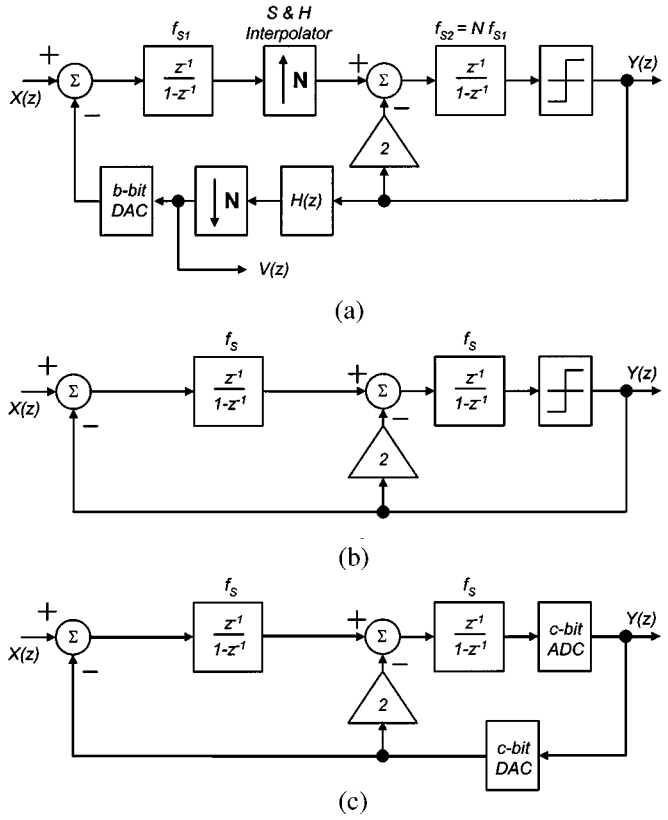

Fig. 1. Architecture of second-order ΣΔ modulators. (a) MM-ΣΔ modulator. (b) Conventional single bit architecture. (c) Conventional mulitibit architecture.

a considerable amount of gain at frequencies in the baseband, baseband noise and distorsion occurring in the integrators succeeding the first one are greatly attenuated when referred back to the modulator input. Therefore, the noise and distorsion performance of a ΣΔ modulator is primarily determined by the first integrator, which, in turn, determines the power consumption of the full converter. Concerning resolution, this paper shows that a reduction in the oversampling ratio of the first integrator(s) of a ΣΔ modulator can be compensated by an increase in the oversampling ratio of the last integrators, whose contribution to power consumption is not so significant. In this sense, this paper shows that proper selection of the oversampling ratio in each integrator of a single-loop or a cascaded-ΣΔ modulator is another architectural decision to be considered in the design of high-resolution, low-power, high-speed ΣΔ modulators.

Based on this reasoning, different architectures are proposed here which decrease the oversampling ratio in the first integrator(s) of a ΣΔ modulator at the cost of an increase in the last integrators and, in some cases, additional circuitry. The actual decrease in power consumption achieved with these architectures are not quantified here, as it is technology dependent and should be addressed in a case-by-case basis.

In [14] a new type of single-loop ΣΔ modulators was proposed where the first integrator works at a lower oversampling ratio than the rest of integrators [the second-order version is shown in Fig. 1(a)]. As the modulator output y in Fig. 1(a) has a high sampling rate, it has to be down-sampled before being fed back to the first integrator. To this end, a digital filter $H(z)$ and one DAC have to be included in the feedback path. This architecture can be also considered to be a multibit modulator where the multibit quantizer in the forward path has been replaced by a single bit one, operating at a higher frequency, by the increase in the sampling rate of the last integrator; therefore, it was called a Multibit-Multirate ΣΔ (MM-ΣΔ) Modulator.

Although MM-ΣΔ modulators achieve a reduction in the oversampling ratio of the first integrator, the presence of a multibit DAC in the feedback path introduces all drawbacks inherent to multibit architectures. Note that the filter $H(z)$ and the DAC in the feedback path appear because the output signal has to be fedback to the first integrator. This kind of feedback is not necessary between stages of cascaded structures, making them good candidates for multirating. In this paper, a new class of cascaded ΣΔ modulators, called multirate-cascade ΣΔ (MC-ΣΔ) modulators, is proposed, where the first modulator stage uses an oversampling ratio lower than the rest of stages.

In Section II MM-ΣΔ modulators are reviewed, and their performances are obtained using a new analytical model. In Section III the new MC-ΣΔ modulators are presented and their performances are estimated. These results are validated by means of simulation. All simulations have been carried out in the time domain using MATLAB-Simulink.[1]

Although most of results obtained here are useful to any implementation of ΣΔ modulators, we focus our attention in a switched-capacitor implementation.

II. MM-ΣΔ Modulator

For the sake of simplicity, the MM-ΣΔ modulator will be presented for the second-order case. Fig. 1(b) shows the architecture of a conventional second-order ΣΔ modulator. Let f_S be the sampling rate and let f_N be the input signal Nyquist frequency. The oversampling ratio is defined as $M = f_S/f_N$. Unlike the conventional ΣΔ modulator of Fig. 1(b), in the MM-ΣΔ modulator of Fig. 1(a), the first and second integrators are operated at different sampling frequencies. Therefore, this modulator has two different oversampling ratios, $M_1 = f_{S1}/f_N$ and $M_2 = f_{S2}/f_N = N \cdot M_1$, where N is the oversampling ratio increment of the second integrator.

In the MM-ΣΔ modulator, the output y has to be downsampled at rate f_{S1} before being fed back to the first integrator. To avoid aliasing, y is filtered [by means of the digital filter $H(z)$], before being decimated,. To this end, simple comb-type digital filters are used [1]. Note that, in a practical implementation, the modulator output would be taken from v, rather than from y, to take profit from the decimation process done in the feedback path. After decimation, signal v is $(b = 2\log_2 N)$-bit wide, and a b-bit DAC is required to convert it back to the analog world.

The MM-ΣΔ modulator can be also considered to be a multibit ΣΔ modulator, where the multibit quantizer in the forward path [Fig. 1(c)] has been replaced by a single bit one, operating at a higher frequency, by the increase in the clock rate of the second integrator. In Section III a relation between the word lengths in the feedback path of a MM-ΣΔ modulator

[1] MATLAB-Simulink is a registered trademark of The MathWorks, Natick, MA.

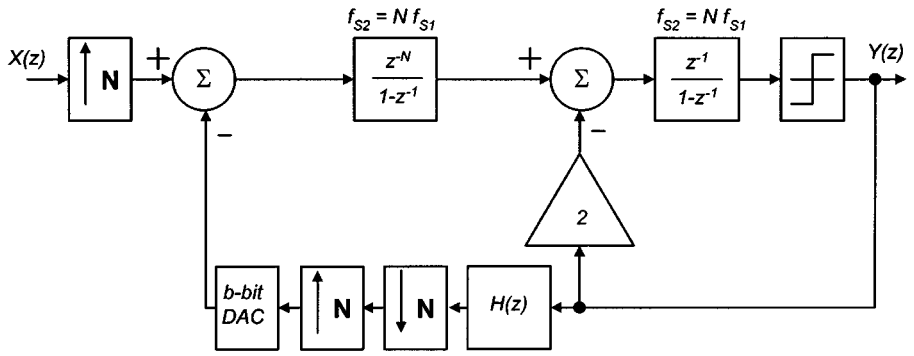

Fig. 2. Block diagram equivalent to the MM-$\Sigma\Delta$ modulator of Fig. 1(a).

and of a multibit $\Sigma\Delta$ modulator with similar performances, will be given.

For the sake of completeness, in a MM-$\Sigma\Delta$ modulator with order higher than 2, every integrator is operated at the high frequency rate f_{S2}, except the first one which is operated at the low frequency rate f_{S1}. Note that other intermediate solutions could be considered, extending the low oversampling ratio to integrators other than the first one. These intermediate solutions are not studied here and will be deferred to future research.

A. Analysis of the MM-$\Sigma\Delta$ Modulator

Let us turn again our attention to the second-order MM-$\Sigma\Delta$ modulator. The circuit in Fig. 1(a) can be shown to be equivalent to the circuit in Fig. 2. Now the first integrator of Fig. 1(a), working at the rate f_{S1}, and the sample and hold interpolator have been replaced in Fig. 2 by an integrator working at the rate f_{S2} and a N-delay.

Using a linear model for the quantizer in Fig. 2, the following expression can be obtained:

$$Y(z) = \mathrm{STF}(z) \cdot X(z^N) + \mathrm{NTF}(z) \cdot E(z) + W(z) \qquad (1)$$

where $X(z)$ is the z-transform of the subsampled input sequence and $E(z)$ is the quantization noise. The second member of expression (1) is the summation of three terms: the input signal filtered by the signal transfer function (STF), the shaped quantization noise, and an error term, $W(z)$, due to aliasing in the decimation process. The $\mathrm{STF}(z)$ and the noise transfer function $\mathrm{NTF}(z)$ are given by

$$\mathrm{STF}(z) = \frac{z^{-(N+1)}}{F(z)} \quad \text{and} \quad \mathrm{NTF}(z) = \frac{(1-z^{-1})^2}{F(z)} \qquad (2)$$

respectively. $\mathrm{STF}(z)$ and $\mathrm{NTF}(z)$ have a common denominator

$$F(z) = 1 - z^{-2} + \frac{1}{N} \cdot z^{-(N+1)} \cdot H(z). \qquad (3)$$

The error term $W(z)$ is given by

$$W(z) = -\frac{1}{N} \cdot \mathrm{STF}(z) \cdot \sum_{k=1}^{N-1} \left[H\left(z \cdot e^{-j\frac{2\pi k}{N}}\right) \cdot Y\left(z \cdot e^{-j\frac{2\pi k}{N}}\right) \right]. \qquad (4)$$

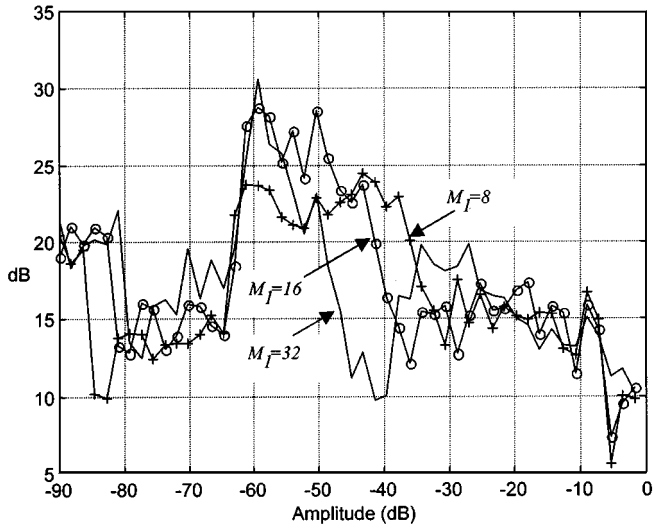

Fig. 3. Ratio between the inband power of the quantization noise and the contribution of the aliasing terms, in a MM-$\Sigma\Delta$ modulator with $N = 4$, for three different values of the low oversampling ratio M_1.

It can be shown that, for common values of N, the spectral components of $W(z)$ folded into the signal band $[0, f_N]$ are negligible, when $H(z)$ is a second-order comb-type filter, i.e.

$$H(z) = \frac{1}{N^2} \left(\frac{1 - z^{-N}}{1 - z^{-1}} \right)^2. \qquad (5)$$

Fig. 3 shows the ratio between the inband power of the shaped quantization noise and the contribution of the aliasing term, for different input signal amplitudes, in a MM-$\Sigma\Delta$ modulator with $N = 4$ and $H(z)$ given by (5). Fig. 3 has been obtained by simulation using the model of Fig. 2.

Based on the results shown in Fig. 3, the term $W(z)$ can be ignored in the baseband. Besides, as $F(e^{j0}) = 1/N$, and $dF/dz(e^{j0}) = 0$, in a first order approach, the denominator $F(z)$ can be replaced by $1/N$, then

$$Y(z) \approx N \cdot \left(z^{-(N+1)} \cdot X(z^N) + (1 - z^{-1})^2 \cdot E(z) \right). \qquad (6)$$

Note that the N factor which multiplies $X(z^N)$ in (6) cancels the attenuation introduced by the input interpolator (see Fig. 2).

Proceeding as in [1], the inband quantization noise power (QNP) is given by the expression

$$\text{QNP}(\Delta, M_1, N, 2) \approx \frac{\pi^4}{60} \cdot \frac{\Delta^2}{M_1^5 \cdot N^3} \quad (7)$$

where $\text{QNP}(\Delta, M_1, N, L)$ is the inband QNP of a Lth-order $\Sigma\Delta$ modulator with quantization step Δ, oversampling ratio M_1 in the first integrator, and $M_2 = N \cdot M_1$ in the rest.

Following a similar procedure, the inband QNP of high-order MM-$\Sigma\Delta$ modulators can be obtained

$$\text{QNP}(\Delta, M_1, N, L) \approx \frac{\pi^{2L}}{12(2L+1)} \cdot \frac{\Delta^2}{M_1^{2L+1} \cdot N^{2L-1}}. \quad (8)$$

B. Relative Performances of MM-ΣΔ Modulators

To evaluate the performances of MM-$\Sigma\Delta$ modulators, expression (9) shows the ratio between the inband QNP of a Lth-order MM-$\Sigma\Delta$ modulator with oversampling ratios M_1 and $M_2 = N \cdot M_1$, and the inband QNP of a conventional c-bit Lth-order $\Sigma\Delta$ modulator with oversampling ratio M. From (8)

$$\frac{\text{QNP}(\Delta, M_1, N, L)}{\text{QNP}(\Delta/(2^c-1), M, 1, L)} \approx \left(\frac{M}{M_1}\right)^{2L+1} \cdot \frac{(2^c-1)^2}{N^{2L-1}}. \quad (9)$$

Three cases will be considered.

a) 1-bit Lth-order conventional $\Sigma\Delta$ modulator operating at the low oversampling ratio M_1 (i.e., $c = 1, M = M_1$). In this case, the ratio between the inband QNP's falls by $3 \cdot (2L-1)$ dB, for every doubling of the oversampling ratio increment N.

b) 1-bit Lth-order conventional $\Sigma\Delta$ modulator with oversampling ratio M (i.e., $c = 1$), and a MM-$\Sigma\Delta$ modulator with $M_1 = M/2$ and $M_2 = 2 \cdot M$ (i.e., $N = 4$). According to expression (9), the inband QNP of the MM-$\Sigma\Delta$ modulator is $3 \cdot (2L-3)$ dB smaller than the inband QNP of the conventional $\Sigma\Delta$ modulator. This result shows that a lower oversampling in the first integrator can be favorably compensated by an increase in the oversampling ratio of the rest of integrators.

c) c-bit Lth-order conventional $\Sigma\Delta$ modulator operating at the low oversampling ratio M_1 (i.e., $M = M_1$). According to (9), the MM-$\Sigma\Delta$ modulator and the c-bit conventional $\Sigma\Delta$ modulator have the same inband QNP when

$$c = \log_2\left(N^{(L-0.5)} + 1\right). \quad (10)$$

If N or $L \gg 1$, this expression reduces to $c \approx (L - 0.5)\log_2 N$.

As expected, this result clearly shows that, compared to a multibit structure, the gain in resolution for MM-$\Sigma\Delta$ modulators comes from replacing the multibit quantizer in the forward path by a single bit one, operating at a higher frequency, by the increase in the oversampling ratio of last integrators.

C. Simulation Results and Discussion

Simulations reveal that a convenient order for filter $H(z)$ in the feedback path of the MM-$\Sigma\Delta$ modulator is $k = L$, and this value has been used in the simulations reported here. Fig. 4 shows the simulated signal-to-noise plus distortion ratio (SNDR) for a MM-$\Sigma\Delta$ modulator with $M_1 = 32$ and $N = 4$ (the feedback DAC resolution is $b = L \cdot \log_2 N = 4$). This architecture will be compared to other three conventional second-order modulators with different topologies and oversampling ratios.

Once again, three different cases will be considered.

a) 1-bit conventional $\Sigma\Delta$ modulator operating at the low oversampling ratio $M_1 = 32$. As expected [expression (9)], approximately 18 dB separate both SNDR curves in Fig. 4.

b) 1-bit conventional $\Sigma\Delta$ modulator with oversampling ratio $M = 64$: Expression (9) predicts 3 dB of larger SNDR for the MM-$\Sigma\Delta$ modulator. This difference is hardly appreciated in Fig. 4, except for small input signals, where second order effects seems to make the MM-$\Sigma\Delta$ modulator to perform better than predicted by our simple first-order analysis, although it should be verified in a real implementation. These effects are not completely understood yet and shall be studied in the future. Concerning power dissipation, as the oversampling ratio of the first integrator in the MM-$\Sigma\Delta$ architecture is a half of the oversampling ratio of the conventional $\Sigma\Delta$ modulator, its power consumption is expected to be smaller. On the other hand, the MM-$\Sigma\Delta$ modulator introduces an additional filter and one DAC in the feedback path, whose effects on power consumption should be carefully studied.

c) 4-bit conventional $\Sigma\Delta$ modulator operating at the low oversampling ratio (i.e., $M = M_1 = 32$). According to expression (10) a 3-bit conventional $\Sigma\Delta$ modulator should have a SNDR similar to the SNDR of the MM-$\Sigma\Delta$ modulator shown in Fig. 1(a) with $N = 4$. However, as the DAC resolution of the MM-$\Sigma\Delta$ modulator is 4 bit, a 4-bit conventional architecture has been selected for comparison. It can be seen in Fig. 4 that the 4-bit $\Sigma\Delta$ converter approximately has a 11 dB improvement in the SNDR, at least for high input signals, as predicted by (9). For small input signals, second effects mentioned above, seem to make the MM-$\Sigma\Delta$ modulator to exhibit a better SNDR. Concerning power consumption, despite the increase in the sampling ratio of the last integrators, the area and power consumption of a MM-$\Sigma\Delta$ modulator are expected to be lower than those of a conventional multibit $\Sigma\Delta$ modulator of similar performances. Note that, as the noise generated in the last stages of the $\Sigma\Delta$ modulator does not critically affect modulator performances, their capacitors are minimized so that they have a small contribution to the total power consumption. The output $V(z)$ is decimated from the lower frequency using conventional techniques. On the other hand, the multibit ADC has been removed from the forward path in the MM-$\Sigma\Delta$ modulator.

III. MC-ΣΔ Architectures

Although MM-$\Sigma\Delta$ modulators achieve a reduction in the oversampling ratio of the first integrator, they introduce a dec-

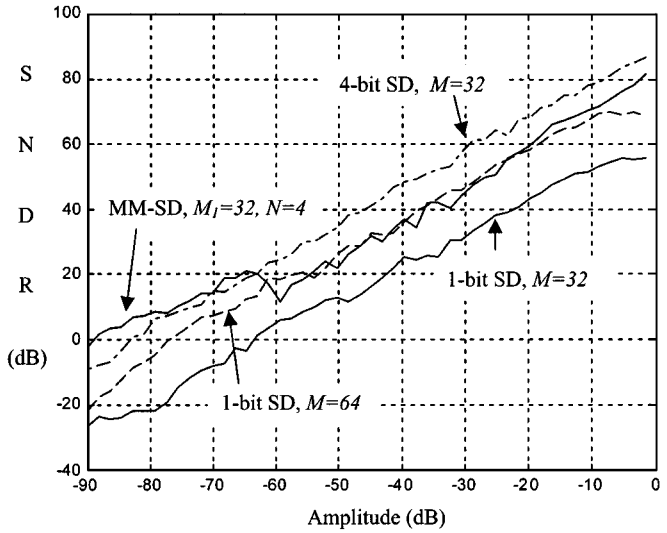

Fig. 4. Simulated SNDR versus input signal amplitude for several second-order modulators with different topologies and oversampling ratios.

imation filter and a multibit DAC in the feedback path whose inherent nonlinearities have to be compensated by means of additional hardware. A similar reduction in the oversampling ratio of the first integrators without the detrimental effects of an internal DAC can be achieved using cascade $\Sigma\Delta$ architectures.

High-order $\Sigma\Delta$ modulators can be built by cascading multiple low-order $\Sigma\Delta$ modulators [16]. In this way the stability properties of low-order (namely, first- and second-order) structures are preserved. In a cascade $\Sigma\Delta$ modulator, a measure of the error term of the ith stage is digitized in the $(i+1)$th stage, and their outputs are combined in the digital domain, in such a way that the noise of the ith stage is cancelled. To achieve cancellation, special attention has to be paid to mismatches between coefficients in the analog and digital signal flows.

Like in the integrators of single loop modulators, the noise of each succeeding stage of a cascaded modulator, when referred to the modulator input, is shaped to a higher degree than the noise of the previous stage. The higher the order of noise shaping, the greater the attenuation in the passband. Therefore, the requirements on cancellation of noise from the second stage are much less than those from the first stage. Because of noise shaping, usually only the first stage in a cascade requires special design considerations and it determines the power consumption of the full modulator.

As an example, in the design process of the 2-2-2 modulator reported in [9], using an oversampling ratio of 16, 62% of total power was consumed in the first stage, 24% in the second stage and only 14% in the third one. Furthermore, the third stage did not contribute significant thermal noise at the modulator input, and minimum sized capacitors were used.

Multirate signal processing can be also applied to reduce the power consumption of a cascade $\Sigma\Delta$ modulator. As power consumption highly increases with sampling frequency when the opamps are operated near their maximum bandwidth, a significant reduction in power consumption is expected if the first stage is operated with a smaller oversampling ratio than the rest of stages. A new class of cascade $\Sigma\Delta$ modulators, called MC-$\Sigma\Delta$ modulators, is proposed here. In a MC-$\Sigma\Delta$ modulator the first stage is operated at a low sampling frequency f_{S1}, while the rest of stages is operated at a high sampling frequency $f_{S2} = N \cdot f_{S1}$, where N is the oversampling ratio increment in the last stages of the modulator. Fig. 5 shows the 2-2 MC-$\Sigma\Delta$ modulator.

Unlike MM-$\Sigma\Delta$ modulators, in a MC-$\Sigma\Delta$ modulator the highest rated signals are not fed back to the analog circuitry working at the lowest rate. Therefore, the modulator in Fig. 5 does not require an additional decimation filter, neither a DAC.

Note that other intermediate topologies could also be considered. For instance, a different oversampling ratio could be selected for each modulator stage, just as sampling capacitors are usually scaled according to their contribution to the input referred quantization noise. These new multirate topologies are a natural extension of the MC-$\Sigma\Delta$ modulators proposed here.

A. Analysis of the MC-$\Sigma\Delta$ Modulator

The analysis of the 2-2 modulator of Fig. 5 will be made. Extension to other cascaded topologies is straightforward.

Assuming perfect matching between coefficients in the analog and digital domains, the z-transform of the modulator output is now given by

$$Y(z) \approx N \cdot z^{-2(N+1)} \cdot X(z^N) + (1-z^{-N})^2 \cdot (1-z^{-1})^2 \cdot E_2(z) \tag{11}$$

where $E_2(z)$ is the quantization noise in the second modulator stage and $X(z)$ is the z-transform of the subsampled input sequence.

Proceeding as in [1] the error cancellation filters are now given by

$$\begin{aligned} H_1(z) &= H_{1,1}(z^N) \cdot H_{1,2}(z) = (2z^{-N} - z^{-2N}) \cdot z^{-2} \\ H_2(z) &= \alpha \cdot (1 - z^{-N})^2. \end{aligned} \tag{12}$$

The filter H_1 can be implemented as a cascade of two filters: $H_{1,1}$ working at the lowest sampling frequency f_{S1}, and $H_{1,2}$ working at the highest sampling frequency f_{S2}. Note that the sample and hold interpolator placed between filters $H_{1,1}$ and $H_{1,2}$ compensates the effects of the sample and hold interpolator placed between stages in the analog domain, therefore, its transfer function has not been included in the cancellation filter H_1. Coefficient α in H_2 cancels the $1/\alpha$ coefficient that appears between stages in the analog domain. Although it can be optimized to maximize signal swing, a value of $\alpha = N$ is appropriate.

B. Simulation Results and Discussion

Considering that the low-frequency gain of the integrators in the second stage is $20\log_{10} N$ dB greater than that of integrators in the first stage, the expected theoretical improvement in the SNDR is $40\log_{10} N$ dB when compared to a classical cascade of two second-order stages where all integrators are working at the lowest rate f_{S1}. For instance, if $N = 4$ the expected improvement in the SNDR is 24 dB. This result is validated by simulation as can be seen in Fig. 6. This figure shows the SNDR for four different 2-2 cascade $\Sigma\Delta$ modulators. Note that

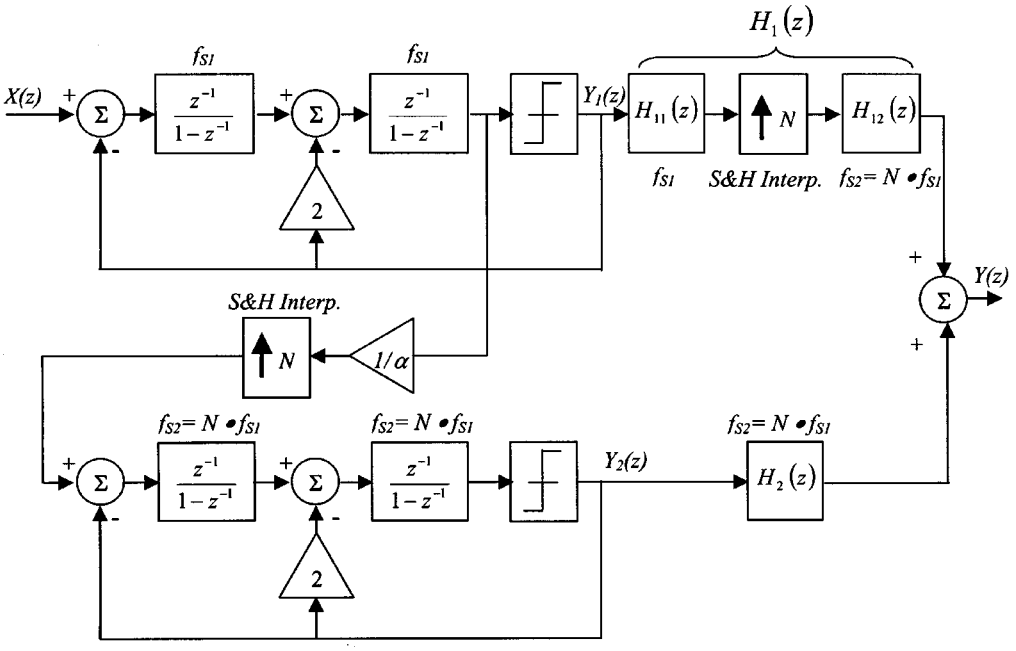

Fig. 5. New 2-2 (MC-ΣΔ) modulator.

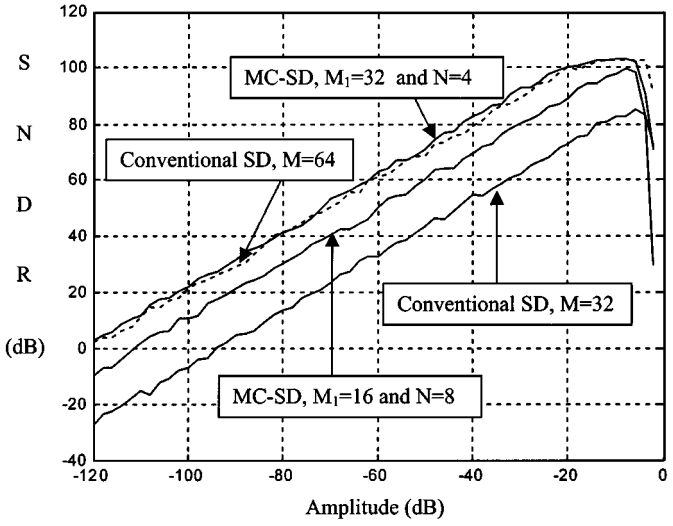

Fig. 6. SNDR versus input signal amplitude for 2-2 cascade ΣΔ moduladors.

the SNDR for a MC-ΣΔ modulator with $M_1 = 32$ and $N = 4$ is approximately equal to the SNDR of the conventional ΣΔ modulator operating at the oversampling ratio $M = 64$. This result shows that a reduction in the oversampling ratio of the first modulator stage can be compensated for a similar increase in the oversampling ratio of the last modulator stages, whose effects on power consumption are not so critical.

IV. Conclusion

New high-speed, low-power ΣΔ converters operate at a low oversampling ratio. This paper has shown that multirating is a useful technique to reduce power consumption in ΣΔ converters. As integrators have a large gain in the baseband, baseband noise and distorsion occurring in the integrators succeeding the first one are greatly attenuated when referred back to the modulator input. Therefore, the noise and distorsion performance of a ΣΔ modulator is primarily determined by the first integrator, which, in turn, determines the power consumption of the full modulator. To reduce the power consumption in the first integrator(s) of a ΣΔ modulator, two new types of ΣΔ modulators have been proposed. The first one, called MM-ΣΔ modulator, uses a low oversampling ratio in the first integrator of a single loop modulador. MM-ΣΔ modulators require an additional digital filter and one multibit DAC in the feedback path, and they can be considered to be multibit converters, whose multibit quantizer in the forward path has been replaced by a single bit one, operating at a higher frequency, by an increase in the sampling frequency of last integrators. The second type of new ΣΔ modulators, called MC-ΣΔ modulator, uses a low oversampling ratio in the first stage of a cascaded architecture. MC-ΣΔ modulators do not require additional filtering nor multibit DACs. Performances of MM-ΣΔ and MC-ΣΔ modulators have been studied and compared to those of conventional ΣΔ modulators showing that, concerning resolution, a reduction in the oversampling ratio of the first integrator(s) or stage(s) of a ΣΔ modulator can be compensated by an increase in the oversampling ratio of the last ones, whose contribution to power consumption is not so significant. These results open the way to new high-performance multirate ΣΔ modulators, where the sampling frequency of each integrator or stage is optimized to minimize power consumption.

References

[1] J. C. Candy and G. C. Temes, "Oversampling methods for A/D and D/A conversion," in *Oversampling Delta-Sigma Data Converters*. New York: IEEE Press, 1992, pp. 1–25.

[2] S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design and Simulation*. New York: IEEE Press, 1996.

[3] L. E. Larson, T. Cataltepe, and G. C. Temes, "Multi-bit oversampled Σ-Δ A/D convertor with digital error correction," *Electron. Lett.*, vol. 24, pp. 1051–1052, Aug. 1988.
[4] J. W. Fattaruso, S. Kiriaki, M. de Wit, and G. Warwar, "Self-calibration techniques for a second-order multi-bit sigma-delta modulator," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1216–1223, Dec. 1993.
[5] B. H. Leung and S. Sutarja, "Multibit sigma-delta A/D converter incorporating a novel class of dynamic element matching techniques," *IEEE Trans. Circuits Syst. II*, vol. 39, pp. 35–51, Jan. 1992.
[6] B. P. Brandt and B. A. Wooley, "A 50-MHz multibit sigma-delta modulator for 12-b 2-MHz A/D conversion," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1746–1756, Dec. 1991.
[7] Z.-Y. Chang, D. Macq, D. Haspeslagh, P. M. P. Spruyt, and L. A. G. Goffart, "A CMOS analog front-end circuit for an FDM-based ADSL system," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1449–1456, Dec. 1995.
[8] T. L. Brooks, D. H. Robertson, D. F. Kelly, A. Del Muro, and S. W. Harston, "A cascaded sigma-delta pipeline A/D converter with 1.25 MHz signal bandwidth and 89 dB SNR," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1896–1906, Dec. 1997.
[9] A. R. Feldman, B. E. Boser, and P. R. Gray, "A 13-b, 1.4 MS/s sigma-delta modulator for RF baseband channel applications," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1462–1469, Oct. 1998.
[10] F. Medeiro, B. Pérez-Verdú, and A. Rodríguez-Vázquez, "A 13-bit, 2.2-MS/s, 55-mW multibit cascade $\Sigma\Delta$ modulator in CMOS 0.7-μm single-poly technology," *IEEE J. Solid-State Circuits*, vol. 34, pp. 748–760, June 1999.
[11] J. C. Morizio, M. Hoke, T. Kocak, C. Geddie, C. Hughes, J. Perry, S. Madhavapeddi, M. H. Hood, G. Lynch, H. Kondoh, T. Kumamoto, T. Okuda, H. Noda, M. Ishiwaki, T. Miki, and M. Nakaya, "14-bit 2.2-MS/s sigma-delta ADC's," *IEEE J. Solid-State Circuits*, vol. 35, pp. 968–976, July 2000.
[12] S. Rabii and B. A. Wooley, "Appendix A: Fundamental limits," in *The Design of Low-Voltage, Low-Power Sigma-Delta Modulators*. Norwell, MA: Kluwer, 1999.
[13] ——, "Appendix B: Power dissipation versus. supply voltage and oversampling rate," in *The Design of Low-Voltage, Low-Power Sigma-Delta Modulators*. Norwell, MA: Kluwer, 1999.
[14] F. Colodro, A. Torralba, F. Muñoz, and L. G. Franquelo, "New class of multibit sigma-delta modulators using multirate architecture," *Electron. Lett.*, vol. 36, pp. 783–785, Apr. 2000.
[15] J. C. Candy, "Decimation for sigma delta modulation," *IEEE Trans. Commun.*, vol. COM-34, pp. 72–75, Jan. 1986.
[16] T. Hayashi, Y. Inabe, K. Uchimura, and A. Iwata, "A multistage delta-sigma modulator without double integration loop," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 1986, pp. 182–183.

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