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LETTER *Special Section on Nonlinear Theory and its Applications*

Low-Voltage, Low-Distortion and Rail-to-Rail CMOS Sample and Hold Circuit

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SUMMARY In this letter, we propose a sample and hold circuit (S/H circuit) with the clock boost technique and the input signal tracking technique. The proposed circuit block generates the clock with the amplitude of $V_{DD} + v_{in}$, and the clock is used to control the MOS switch. By applying this circuit to a S/H circuit, we can deal with the rail-to-rail signal with maintaining low distortion. Furthermore, the hold error caused by the charge injection and the clock feedthrough can be also reduced by using the dummy switch. The Star-HSPICE simulation results are reported in this letter.

key words: *sample hold circuit, low-voltage circuits, boost circuits, MOS analog integrated circuits, analog circuits*

1. Introduction

The portable electronic market has accomplished explosive growth, and advance in CMOS technology has led designers towards low-voltage operation and mixed-signal systems. Therefore, a date converter operated under low-voltage will be an essential component of the portable electronics. Sample and hold circuits (S/H circuit) are widely used in the discrete analog circuits and play an important role in the design of data converters. In analog switches used in the S/H circuits, rail-to-rail signal swing capability is required for maintaining high signal to noise ratio. However, it is difficult to realize it because of two issues. One is that the analog switches cannot be deeply turned on because enough overdrive voltage cannot be supplied to gates of MOS switches under the low-voltage condition. The other is that the output signal is distorted by the on-resistance, which is varied by the difference between input voltage of the MOS switch and the clock voltage. In order to overcome these issues, the clock boost technique [1], [2] and the input signal tracking technique attract [3], [4]. However, there is a problem that a hold error increases by the charge injection and clock feedthrough. This error becomes larger with using the boosted clock.

In this letter, a S/H circuit with the clock boost technique and the input signal tracking technique is proposed. The proposed circuit consists of two simple clock boosters with input tracking circuit and a dummy switch. As the results, the proposed circuit reduce the effect of charge injection and feedthrough with maintaining low-voltage, low-distortion and rail-to-rail operation. The proposed circuit is evaluated through Star-HSPICE simulation with the process parameters of CMOS 0.35 μm. The results are shown in this letter.

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2. S/H Circuit Design

The circuit diagram and the symbolic representation of the clock generator with the boost and V_{in} tracking technique are shown in Fig. 1(a) and (b), respectively. The circuit is controlled by a clock *PHI* and operates as follows. When *PHI* is high, V_{DD} is applied across C_1 since M_2 and M_3 are turned on. Simultaneously M_1 and M_4 are turned off, and M_5 is turned on. V_G results in becoming the ground level. When *PHI* is low, M_2 and M_3 are turned off, and M_1 is turned on. The voltage of the top plate of C_1 is boosted to $V_{DD} + V_{in}$ because the bottom plate of C_1 is connected to V_{in} and M_4 and M_5 are turned on and off, respectively. V_G,

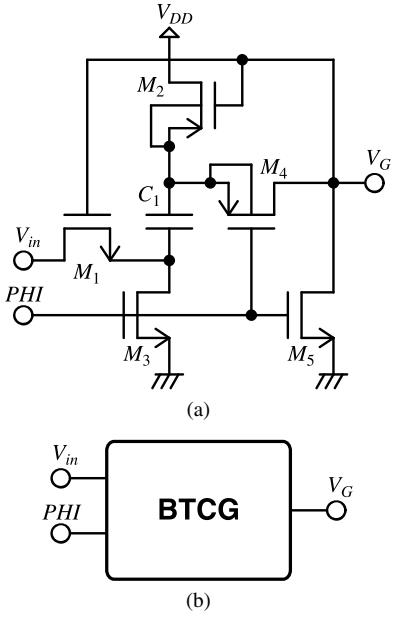

Fig. 1 Clock generator with the boost and V_{in} tracking technique. (a) Circuit diagram. (b) Symbolic representation (BTCG: Boost and V_{in} Tracking Clock Generator).

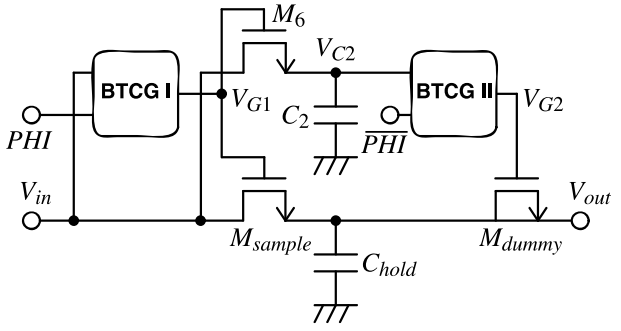

Fig. 2 Proposed S/H circuit.

which is equal to the voltage of the top plate of C_1, results in becoming $V_{DD} + V_{in}$. In this way, the circuit shown in Fig. 1(a) generates the boosted and V_{in}-tracked clock.

Next, we discuss the error of the charge injection and the clock feedthrough. These effects cause the hold error of the S/H circuit. Especially, the hold error caused by these effects is increased when the boosted clock is used. In this letter, these problems are solved with a dummy switch, which is well-known technique [5]. The channel width (W) of the dummy switch is set to half of the MOS switch, and the channel length (L) is identical. The half of the charge released by the MOS switch during its turn-off transient is stored in the parasitic capacitor, and is cancelled by charge drawn by the dummy switch. In order to achieve this cancellation, the controlled clock voltage for the dummy switch should be equal to the clock signal just before MOS switch is turn off.

Figure 2 shows the proposed S/H circuit using the clock generators shown in Fig. 1 (BTCG I and II) and the dummy switch (M_{dummy}). This circuit is controlled by the non-overlapped two phase clock (PHI and $\overline{PHI}$). In the proposed circuit, the BTCG I generates the clock signal for the MOS switch (M_{sample}), which equals to $V_{DD} + V_{in}$, and the circuit block composed by M_6, C_2 and BTCG II generates the feasible clock for M_{dummy} in order to reduce the error caused by the charge injection and the clock feedthrough.

When PHI is low, M_{sample} and M_6 are turned on, and V_{in} is applied across C_2 ($V_{C2} = V_{in}$). Simultaneously, V_{G2} becomes the ground level. When PHI is high, M_{sample} and M_6 are turned off. The V_{C2} becomes equal to voltage just before M_{sample} and M_6 are turned off, and this voltage is inputted into the BTCG II. Therefore, V_{G2} becomes equal to $V_{DD} + V_{C2}$. At this time, the channel charge of M_{sample} flows into the parasitic capacitances of M_{dummy}. In this way, the error caused by the charge injection and the clock feedthrough can be cancelled. In this way, we can archive the low-voltage, low-distortion and rail-to-rail S/H circuit.

3. Simulation Results

The proposed circuit has been evaluated through Star-HSPICE simulation with the device parameters of 0.35 μm standard CMOS process. In the proposed circuit, V_{DD} is 1.5 V. The other detailed settings are shown in Table 1.

Table 1 Design parameters of Fig. 2.

Circuit Block	Device Name	Value
BTCG I	W/L of M_3	5μm/0.5μm
	W/L of M_2	10μm/0.5μm
	W/L of M_1, M_4, M_5	15μm/0.5μm
	C_1	1.5 pF
BTCG II	W/L of M_1, M_3, M_5	5μm/0.5μm
	W/L of M_2	10μm/0.5μm
	W/L of M_4	15μm/0.5μm
	C_1	3.0 pF
—	W/L of M_6, M_{dummy}	5μm/0.5μm
	W/L of M_{sample}	10μm/0.5μm
	C_2, C_{hold}	1.0 pF

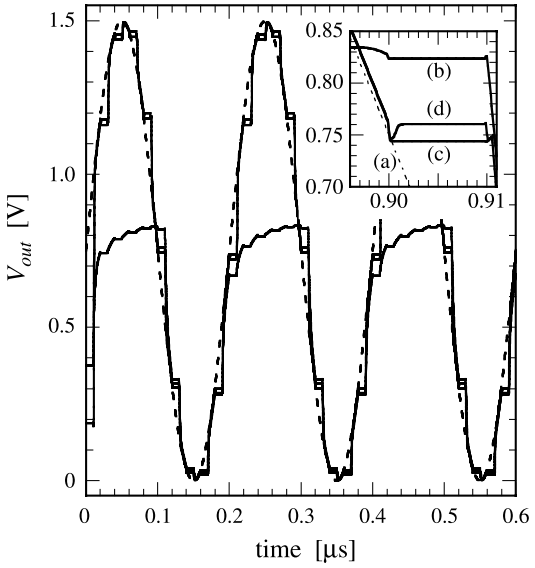

Fig. 3 Simulation results. (a) Input signal, (b) conventional S/H circuit, (c) the proposed S/H circuit without the dummy switch and (d) the proposed S/H circuit with the dummy switch (Fig. 2).

Figure 3 show the simulation results of the conventional circuit, the proposed circuit without the dummy switch and the proposed circuit with the dummy switch (Fig. 2) under the condition of the rail-to-rail input signal. From this figure, we can find that the proposed S/H circuit can operate well. Furthermore, we can find that the proposed S/H circuit with the dummy switch holds the V_{in} correctly with reducing the hold error. Figure 4 shows the relation between total harmonic distortion (THD) and amplitude of V_{in} when the frequencies of V_{in} (f_{in}) are 2.5 MHz and 5.0 MHz. When the amplitude of V_{in} and f_{in} are 1.5 V_{p-p} and 2.5 MHz, respectively, THD of the proposed S/H circuit is 0.19%. Moreover, THD was approximately 1% when the amplitude of V_{in} and f_{in} were 1.5 V_{p-p} and 9.1 MHz, respectively. We could find that THD was increase with increase of f_{in} through the simulations. Figure 5 shows the relation between the hold error and amplitude of V_{in}. When the amplitude of V_{in} and f_{in} are 1.0 V_{p-p} and 2.5 MHz, respectively, we can find that the hold error is 1.8 mV. Using the proposed S/H circuit with the dummy switch, we can see that the hold

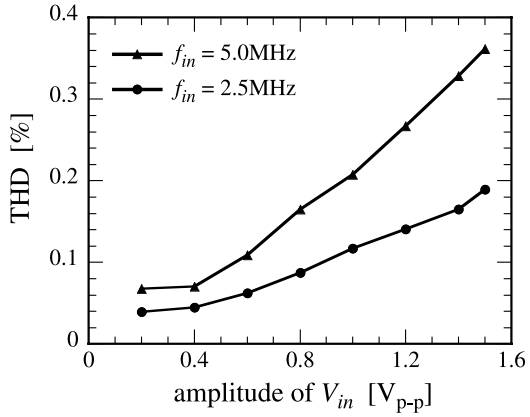

Fig. 4 Simulated THD under the condition that the frequency of V_{in} (f_{in}) are 5.0 MHz and 2.5 MHz.

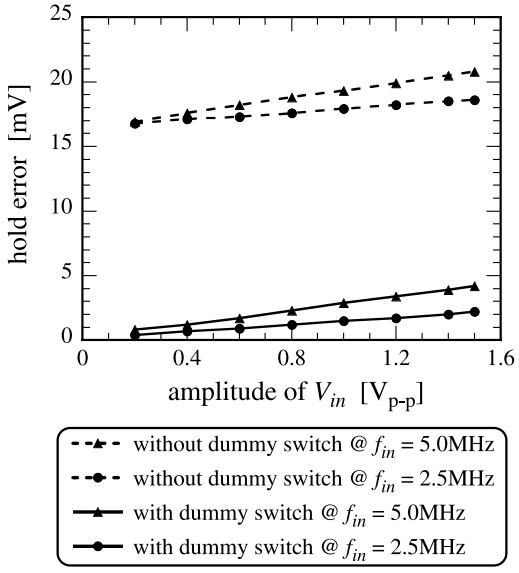

Fig. 5 Simulated hold error.

error can be reduced to 1/10 from Fig. 5.

4. Conclusions

In this letter, we have proposed a low-voltage, low-distortion and rail-to-rail CMOS S/H circuit with the clock boost technique and the V_{in} tracking technique. From the Star-HSPICE simulation, we have found that the S/H circuit could be operated at V_{DD} of 1.5 V. Furthermore, THD of the proposed S/H circuit was 0.19% under the rail-to-rail input condition with f_{in} of 2.5 MHz. Moreover, we have found that the hold error could be reduced to 1/10 by using the dummy switch.

Acknowledgments

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