A 60-MHz 150-μV Fully-Differential Comparator

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(Invited Paper)

Abstract

The overall performance of two-step flash A/D converters hinges on the second-stage fine comparator. This paper descibes the design of a 60 MHz fully differential comparator, intended for use in a 12-bit two-step flash converter. The comparator consists of four pre-amplifier stages followed by a regenerative latch. It uses a combination of output offset cancelation and input offset cancelation to acheive 150 mV resolution. The comparator is designed to operate from a $2.5V$ supply, has an active area of 522 μm^2, and consumes 247 μW of power.

I. Introduction

In the design of the fine comparator for a CMOS two-step flash A/D converter, the main design issues are offset cancelation and fast amplification of differential inputs. This paper describes a 60 MHz comparator circuit that consists of four cascaded low-gain amplifiers followed by a regenerative latch. The circuit is fully differential in order to mimimize sensitivity to coupling noise. The circuit compares an input with a reference voltage of $1.2\ V$, and must tolerate overdrive of up to $0.4\ V$ without errors.

Figure 1 shows a block diagram of the comparator circuit. Conceptually, the circuit consists of a first amplifier stage, followed by a capacitor for output offset storage, followed by another amplifier stage that uses the same capacitor for input offset storage. However, each amplifier stage actually consists of two cascaded low-gain amplifiers in order to achieve higher speed. Because the two second-stage amplifiers are connected in the unity feedback configuration during the offset store period, we must ensure that the circuit is stable. One pair of capacitors is used for the offset storage of all amplifiers in order to minimize die area.

The converter is intended for use in a 12-bit two-step flash A/D converter with $1.6\ V$ input range. Thus, the amplifiers must provide enough gain to overcome the uncompensated offset of the amplifiers in addition to the offset of the regenerative at an input differential of 200 μV. The total required gain, assuming ideal offset cancelation and with some information about worst-case offsets, is

$$Gain \geq \frac{V_{offset,\ 2\ cascaded\ amps} + V_{offset,\ latch}}{200\ \mu\ V} = \frac{12.4\ mV + 19.7\ mV}{200 \mu V} = 160. \quad (1)$$

The required dc gain per amplifier is then 3.6. The design goal was for each amplifier to have a gain of roughly 4 to allow for a offset cancelation errors.

In the beginning stages of design, architectures that perform offset cancelation of the regenerative latch were considered, such as the Wu comparator [3] or the first-stage comparator of Razavi [2]. However, such approaches would have required more complexity. Design options considered within the comparator and latch sections of the circuit, which will be discussed later.

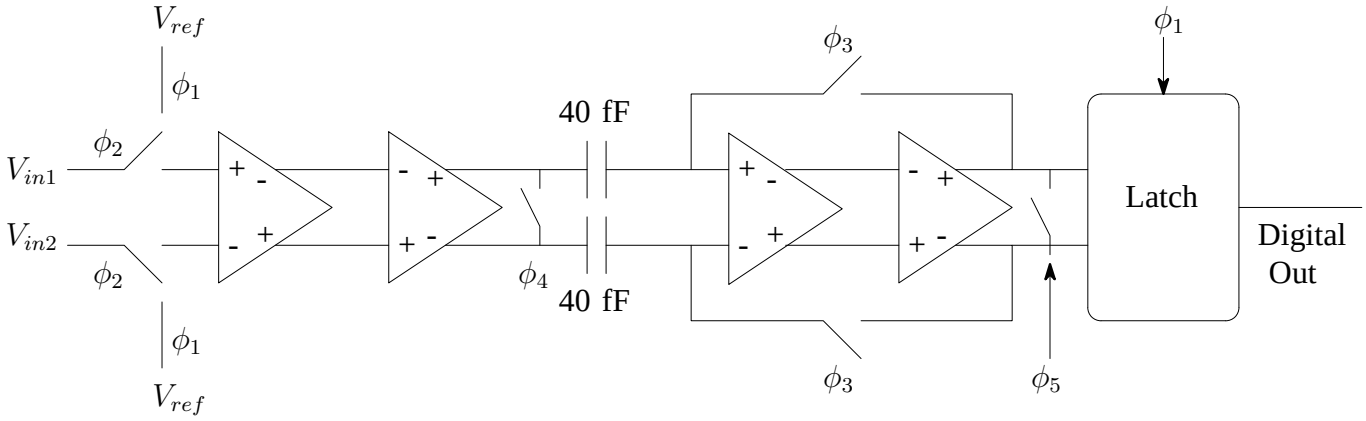

Fig. 1. Comparator Block Diagram

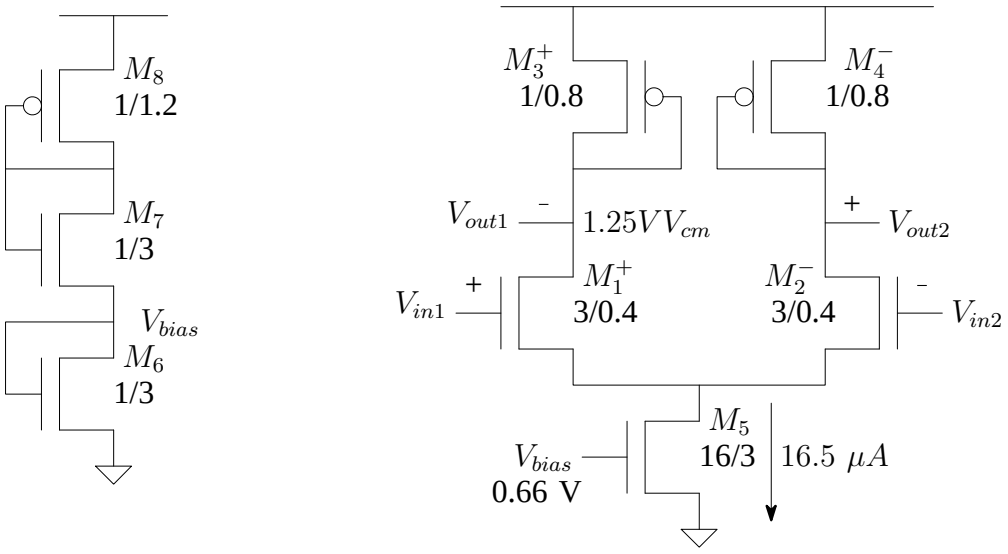

Fig. 2. Op-Amp Circuit

II. Architecture

A. Op-Amp

In order to maximize the speed of our comparator, the op-amp is a low-gain differential pair with diode connected loads. This identical op-amp is used for all four amplifier blocks in the design. Figure 2 shows the topology of our op-amp. Note that device sizes are assumed to be in μm. Common mode feedback is not necessary because the diode connected loads cause the output voltages to nominally sit at $V_{dd} - (V_{gs} - V_{th}) = 1.25\ V$. Note that the common mode output voltage sits near the common mode reference input of $1.2\ V$, ensuring that all four op-amps will have nearly identical operating points. Transistor M_5 has a large length – $3\mu m$ – in order to obtain a stiff current source.

The differential gain of a diode-connected single stage op-amp is given by

$$A = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{\mu_n \frac{W_1}{L_1}}{\mu_p \frac{W_3}{L_3}}} = 4.69. \tag{2}$$

In actuality, the DC gain of the op-amp (measured with a $200\ \mu V$ differential step input) was determined to be 3.99, yielding a total gain of 250 for the four op-amps in cascade.

The bandwidth (BW) of the amplifier $BW \sim \frac{g_{m,\ n}}{C_{load}}$. Increasing the width of the input transistor M_1 increases the gain because $g_{m,M_1} \sim \sqrt{W_1}$, but also increases the input capacitance (that the previous op-amp drives) because $C_{input} \sim W_1$. Therefore the bandwidth goes as $\frac{1}{\sqrt{W_1}}$, making it advantageous to use narrow input transistors.

The worst-case input-referred offset of a single amplifier with $8\ mV$ transistor offsets is $9.9\ mV$, so the worst-case input referred offset of two op-amps in cascade is

$$V_{os,\ combined} = V_{os,\ single} \frac{A+1}{A} = 12.4\ mV. \tag{3}$$

The threshold mismatch polarities that produce the worst-case input referred offset are marked in Figure 2 with $+$ or $-$ signs next to the transistor name, e.g. M_1^+.

The possibility of using PMOS bleeder transistors in parallel with the diode-connected PMOS loads was considered as a way to obtain more gain, or alternatively, to allow narrower input transistors with the same gain. However, increasing the gain proved unnecessary and the bleeder transistors added extra parasitic capacitance at the output, eliminating any bandwidth advantage.

B. Latch

A regenerative latch patterned after Song et. al. [1] was selcted for the latch. It is similar to the Yukawa latch [4] but has the advantage of having no static power dissipation. Figure 3 shows the topology of our latch circuit. The outputs are pre-charged when ϕ_1 is low, removing possible memory effects at the expense of extra power. The regeneration from the cross-coupled transistors, both NMOS and PMOS, make the latch fast. A potential downside of the latch architecture is that the data from

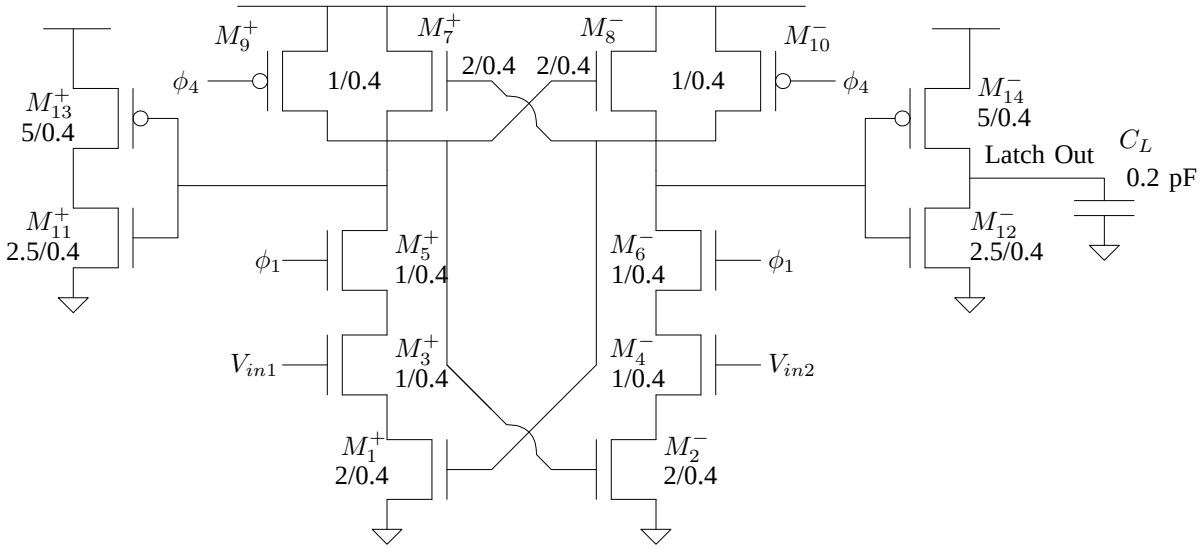

Fig. 3. Latch Circuit

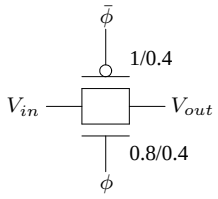

Fig. 4. Complementary Switch

the latch is only valid while ϕ_1 is high. Symmetric buffer inverters were added to the regenerative nodes, both to increase the speed of switching the load capacitance and also to reduce systematic offset (only one side drives the load capacitance).

The worst-case input-referred offset of a single amplifier with $8\ mV$ transistor offsets is $19.7\ mV$. The worst-case arrangement was determined by simulation and is labeled just as in Figure 2.

Originally the latch and output buffer were designed with relatively wide transistors, which made it extremely fast at driving the output load. However, the duration of ϕ_1 is greater than ϕ_2 and the latch output is valid during ϕ_1 in our semi-pipelined architecture (where the latched output resulting from an input during ϕ_2 is valid during the subsequent ϕ_1, which is the offset cancelation phase). Therefore transistor widths in the latch were reduced in order to consume less power; the latched output takes longer to reach its valid state but is still valid for half of the total clock cycle as required.

C. Switches

Switches are used to select different inputs, enable or disable feedback, and to short outputs together to hasten overdrive recovery. The voltages that the switches pass are typically near $1.2\ V$ in magnitude, or mid-supply. Thus, complementary switches were used to minimize switch resistance, as shown in Figure 4. An added benefit is that complementary switches partially cancel charge injection, which is a substantial source of error, particularly at the input because any differential error gets amplified as if it were a signal. At one particular input voltage, charge injection cancelation is perfect, but at other input voltages the cancelation is less complete. The width of the NMOS transistor was selected to make this *magical voltage* about $1.2\ V$, reducing the circuit's sensitivity to voltage-dependent charge injection.

D. Bias Circuit

The bias circuit consists of three diode-connected transistors, as shown in Figure 2. It consumes about $1\ \mu A$ of current.

E. Timing

The comparator utilizes timing that is a variant of a two-phase non-overlapping clocking scheme with some additional clocks to reduce transients. Figure 5 shows the timing waveforms that we use in our circuit. During ϕ_1, the offset voltages of the op-amps are stored on the same capacitor pair and the regenerative latch makes a decision about the input differential during the previous ϕ_2 cycle. Within ϕ_1, the offset voltage of the first stage op-amps are stored first. Next, ϕ_3 goes high, and the offset

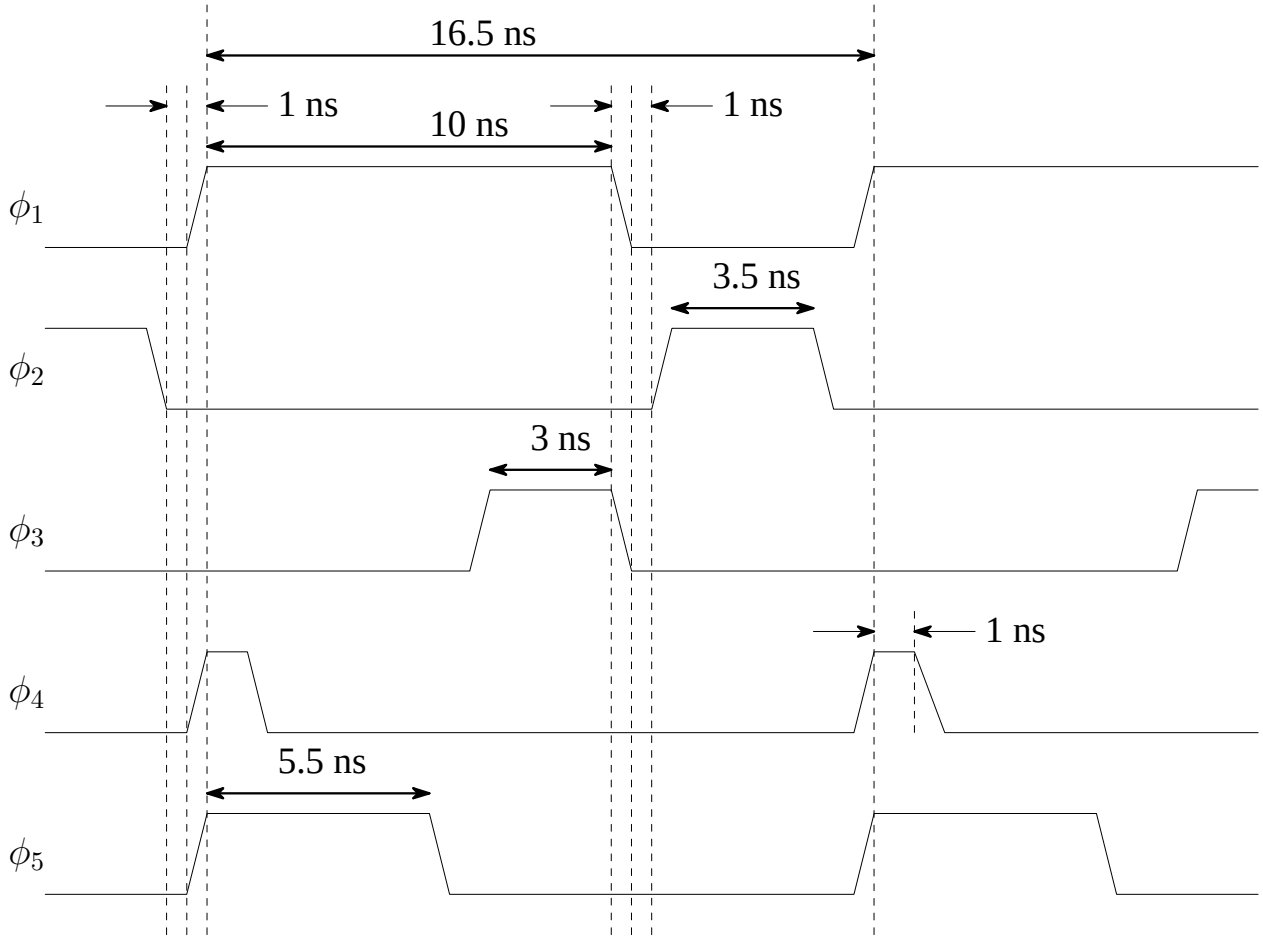

Fig. 5. Timing Waveforms

voltage of the second stage of op-amps are stored. By storing the offset voltages of the first and second stages in succession, the duration of the offset storage period is reduced because co-settling instabilities are avoided. During ϕ_2, the input differential voltage is amplified. Clocks ϕ_4 and ϕ_5 serve to reduce transients in the circuit, by shorting the outputs of the first and second stage, respetively, in order to achieve a faster overdrive recovery.

Figure 6 shows a scheme whereby the clocks for our comparator could be generated. Assume that reference clocks ϕ_{ref1} and ϕ_{ref2} (which are identical in form to those in Figure 5 but time-shifted) are provided. Clocks ϕ_1 and ϕ_2 are generated from ϕ_{ref1} and ϕ_{ref2} respectively by passing them through two inverters with a delay identical to the AND gate used to generate the other clocks. The two inverters used to generate ϕ_3 have a delay of 7 ns. The inverters used to generate ϕ_4 and ϕ_5 have delays of 1 ns and 5.5 ns respectively.

III. Performance Evaluation and Robustness

The performance of the comparator was mainly determined by correct behavior in an overdrive recovery test where an input differential of 0.4 V was applied followed by a small differential voltage of ± 150 μV or ± 200 μV. The latched output was compared with the expected value for all four possible cases (overdrive to small differential), with correct performance meaning that the comparator's outputs were correct for all these cases.

The robustness of the circuit against process variations was a key element in the design. A listing of robustness considerations is as follows:

The two cascaded op-amps in the unity feedback configuration are slightly underdamped; when ϕ_3 closes the feedback switches, there is about 50 mV of ripple at the latch input, which dies out within a few nanoseconds. Because the input of the capacitors has mostly settled before ϕ_3 goes high and because these inputs are shorted at the beginning of ϕ_1, this ripple is independent of the inputs.

Even though the offset storage capacitors are merely 40 fF, capacitor mismatch or absolute capacitor value does not affect the operation of the circuit. The comparator operates properly with up to 20% mismatch of the capacitors from the specified value over all corners. This is expected because the capacitors are simply used to store charge, never to transfer charge between two locations or integrate charge.

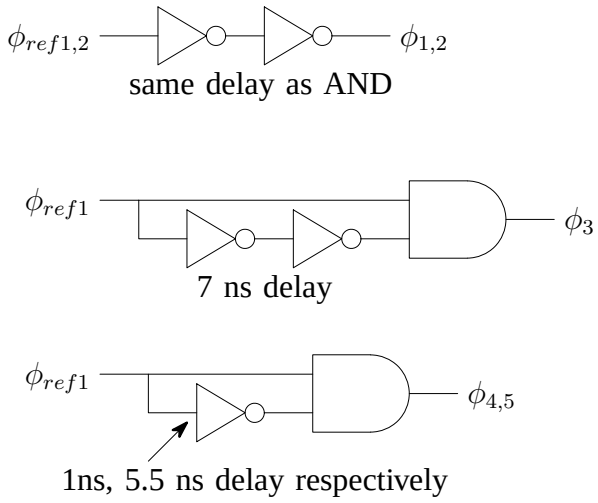

Fig. 6. Clock Generation Scheme

There are adequate overdrive voltages on the bias network of Figure 2. Transistors M_6, M_7, and M_8 respectively have overdrive voltages of $202\ mV$, $187\ mV$, and $203\ mV$, ensuring stability of the bias network against threshold variations.

The circuit exceeds the requirement for resolving a $200\ \mu V$ differential on the input as given in Equation 1, as it reliably resolves $150\ \mu V$.

Some $\frac{kT}{C}$ noise is expected to be injected onto the capacitors, of standard deviation $322\ \mu V$; thus the input-referred $\frac{kT}{C}$ noise is $20\ \mu V$.

Worst-case transistor threshold mismatch (the notation was described above in Section II-A) was included in all simulations. For each subcircuit, the thresholds were modified incrementally to determine the worst-case total input-referred offset. The offsets of the latch and op-amp were already discussed. Threshold mismatch in the switches was also account, and results in a slight skew between the signals passed by the transistors. This skew is only several picoseconds, and did not have a noticible effect on the circuit performance.

$0.5\ ns$ separates the non-overlapping clocks ϕ_1 and ϕ_2. Thus, the circuit can tolerate up to $0.5\ ns$ clock skew. Simulations were also performed in which the other clock signals were skewed by $0.5\ ns$, both in relation to each other and to ϕ_1 and ϕ_2. Not all possible situations were simulated, but the ones which were expected to be most troubling were. The circuit performed correctly in these simulations.

IV. Limitations and Potential Improvements

The performance of the comparator circuit is limited by the time it takes for the offset store phase. The first portion of this time, when the output offset store of the first stage of amplifiers is taking place, is limited by how fast the output current of the first stage amplifiers can drive the parasitic bottom-plate capacitance of the capacitors. The second portion of the offset store phase is limited by the settling time after closing the feedback switch around the second amplifier stage (as noted above, there is a slight underdamped settling). So the conversion speed might be improved by giving more current to the first-stage amplifiers and replacing the two second-stage amplifiers by a single, high-gain, amplifier to avoid instabilities. Another limitation of our circuit is that ϕ_1 and ϕ_2 are not symmetric and thus are not as easy to generate as symmetric clocks. If they were required to be symmetric, the comparator would run at about $50\ MHz$.

V. Performance Summary

Technology	EE315 $0.4\ \mu m$ CMOS
Resolution	$150\ \mu V$
Speed	$60\ MHz$
Active Area	$252\ \mu m^2$
Capacitor Area	$92\ \mu m^2$
Power Dissipation	$247\ \mu W$
Differential Input Range	$\pm\ 0.8V$
Input Capacitance (each input)	$5.5\ fF$

VI. Conclusion

The comparator design presented here acheives high speed ($60\ MHz$) with relatively low area ($\sim\ 350\ \mu m^2$) and modest power dissipation ($\sim 250\ \mu W$). Compared with the Razavi second-stage flash comparator described in [2], the design presented here is 12 times as fast and consumes only 30% of the current, with about the same number of transistors. However, it is difficult to compare the performance directly because Razavi's comparator was implemented in $1\ \mu m$ technology, and this one in $0.4\ \mu m$ technology. If a particular application does not require such high speeds, then the power dissipation can be decreased dramatically.

Acknowledgment

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