# Osnovi digitalne elektronike IR

vežba 1

Odsek za elektroniku

Elektrotehnički fakultet,
Univerzitet u Beogradu

2018/2019

# Plan Rada

- 22.04. - I Čas (Uvod)
- 06.05. - II Čas (Rad sa portovima)
- 13.05. - III Čas (Serijska komunikacija)
- 27.05. - IV Čas (AD Konverzija i tajmeri)

# Pregled

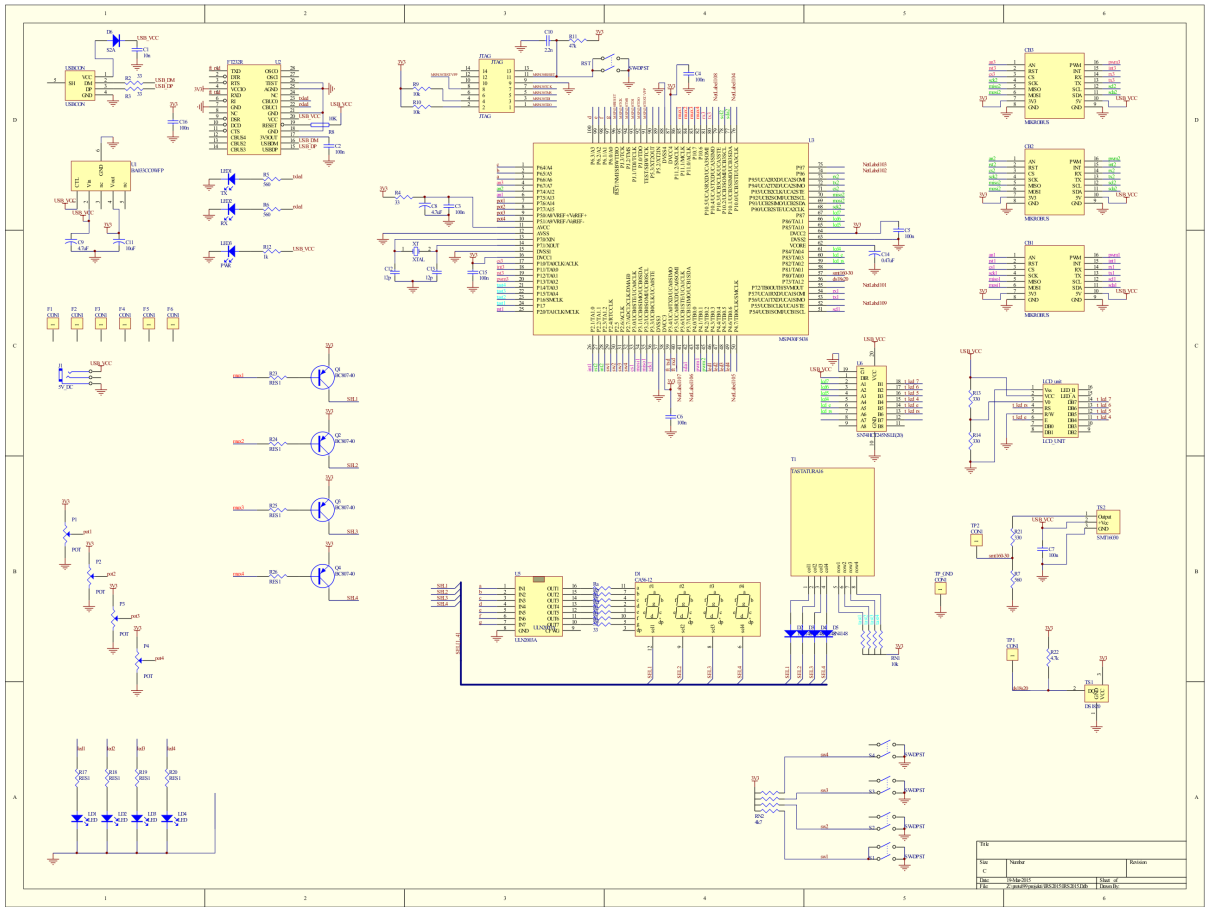
# Razvojno okruženje

Za potrebe razvoja softvera koristi se razvojno okruženje *Code Composer Studio v6*. *Free* verzija koja podržava pisanje svih aplikacija koje će biti razvijane u okviru kursa se može download-ovati sa sajta `http://www.ti.com/tool/ccstudio`

U okviru paketa integrisani su editor, asembler, C kompajler kao i FET emulator.

# Razvojni sistem

Detaljna šema sistema dostupna je na:
`http://tnt.etf.rs/~oe4irs/RS_MSP430F5438A_sch.pdf`



# Osobine MSP430 familije

Familija mikrokontrolera optimizovana za aplikacije sa baterijskim napajanjem

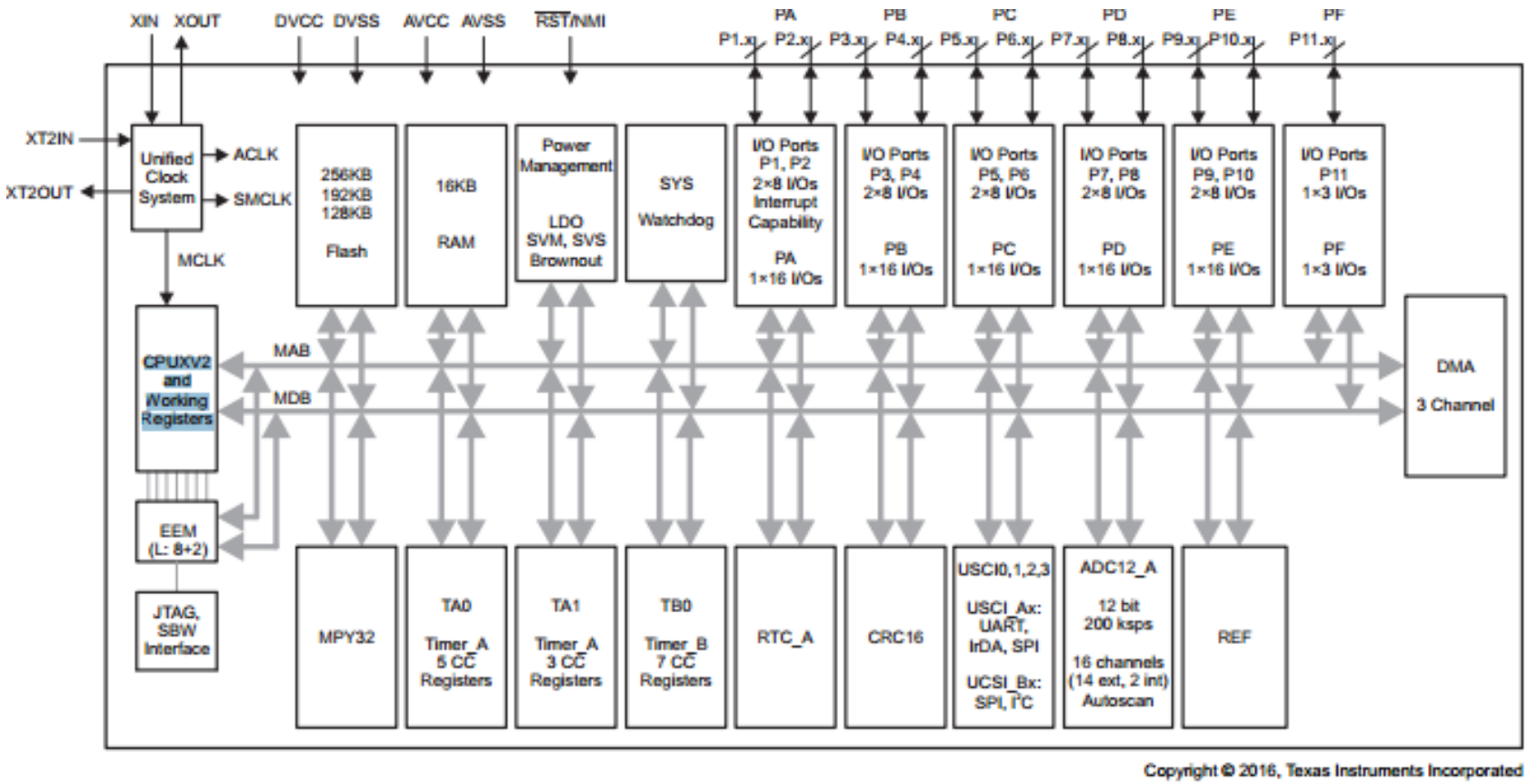
Veliki broj integrisanih periferija (tajmeri, komparatori, AD i DA konvertori, UART...)

16-/20-bitno procesorsko jezgro sa RISC arhitekturom

Podrška za JTAG

# MSP430x 1/2

Familija MSP430 se deli na nekoliko podfamilija: MSP430x5xx, MSP430x6xx... Mi radimo sa mikrokontrolerom MSP430F5438A, koji spada u podfamiliju **MSP430x5xx**



# MSP430x 2/2

MSP430F5438A ima

- 256kB flash-a
- 16kB SRAM-a
- 3 16-bitna tajmera
- DMA Kontroler
- 12-bitni A/D konvertor sa 16 ulaza
- 4 USCI (Universal Serial Communication Interface)
- 87 GPIO pinova...

# Detaljne informacije 1/2

## Datasheet

Detaljne informacije o mikrokontroleru MSP430F5438A
`http://www.ti.com/lit/gpn/msp430f5438a`

## User's guide

Detaljne informacije o familiji MSP430x5xx
`http://www.ti.com/lit/pdf/slau208`

## Erratasheet

Lista poznatih problema i grešaka sa mikrokontrolerom MSP430F5438A `http://www.ti.com/lit/pdf/slaz290`

# Detaljne informacije 2/2

Website, uvek ažuran: `http://www.ti.com/product/msp430f5438a`

www.ti.com/product/msp430f5438a

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My technical documents

- MSP430x5xx and MSP430x6xx Family User's Guide (...
- Autoswitching Power Mux (Rev. A)

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## MSP430F5438A (ACTIVE) ★★★★★ 8 reviews

16-Bit Ultra-Low-Power Microcontroller, 256KB Flash, 16KB RAM, 12 Bit ADC, 4 USCIs, 32-bit HW Multi

MSP430F543xA, MSP430F541xA Mixed Signal Microcontroller (Rev. D)
MSP430F5438A Device Erratasheet (Rev. M)
MSP430x5xx and MSP430x6xx Family User's Guide (Rev. N)

Description & parametrics | Technical documents | Tools & software | Sample & buy | Compare | Quality & packaging | Support & community

Description | Features | Diagrams | Related end equipment | Parametrics | Companion parts | Customer reviews

### Description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3.5 µs (typical).

View more

### Features

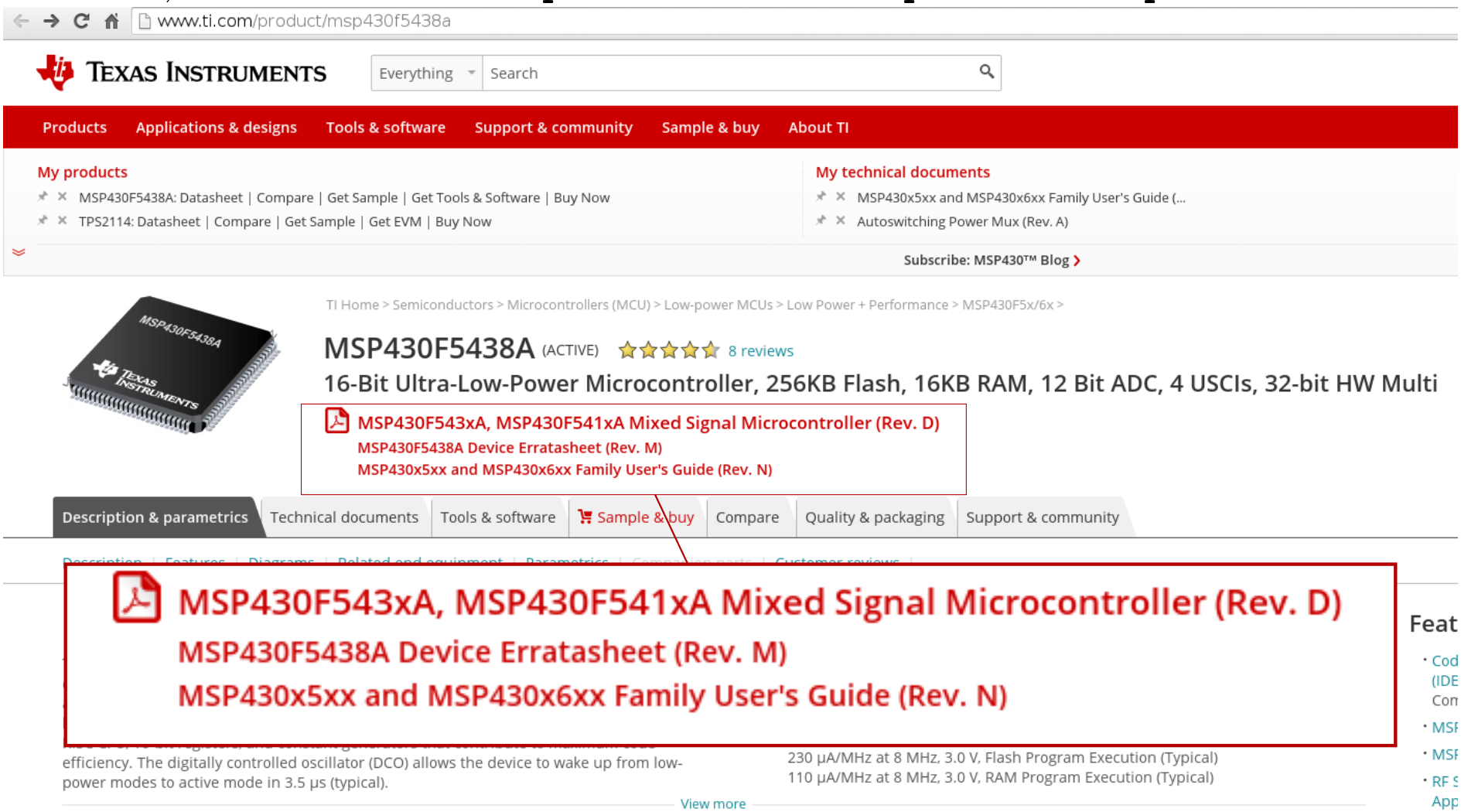
- Low Supply Voltage Range: 3.6 V Down to 1.8 V
- Ultralow-Power Consumption
  - Active Mode (AM):
    All System Clocks Active
    230 µA/MHz at 8 MHz, 3.0 V, Flash Program Execution (Typical)
    110 µA/MHz at 8 MHz, 3.0 V, RAM Program Execution (Typical)

### Feat

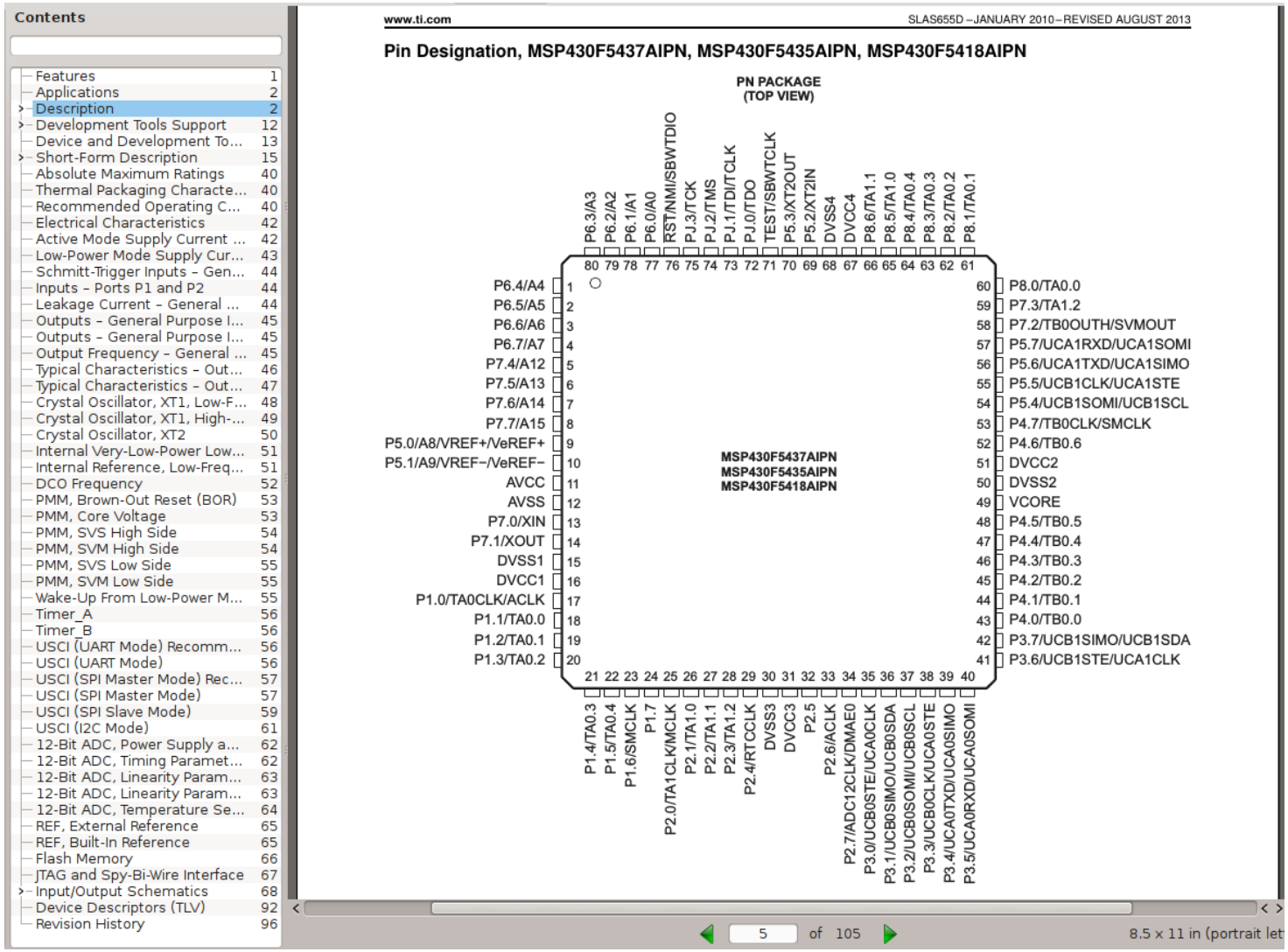
- Cod (IDE Com
- MSF
- MSF
- RF S App

# Detaljne informacije 2/2

Website, uvek ažuran: `http://www.ti.com/product/msp430f5438a`



# Datasheet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55 P5.5/UCB1CLK/UCA1STE
54 P5.4/UCB1SOMI/UCB1SCL
53 P4.7/TB0CLK/SMCLK
52 P4.6/TB0.6
51 DVCC2
50 DVSS2
49 VCORE
48 P4.5/TB0.5
47 P4.4/TB0.4
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27 P2.2/TA1.1
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# User's guide

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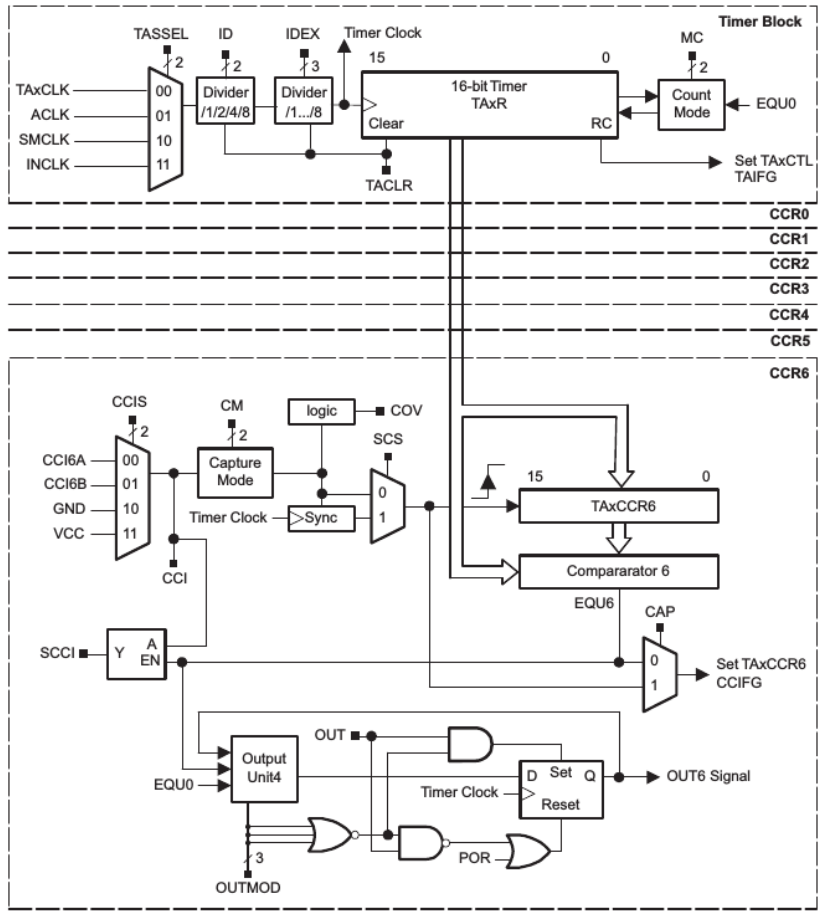



**Figure 17-1. Timer_A Block Diagram**

# Memorija

Adresni prostor je jedinstven za program, podatke i periferije, i njemu se pristupa preko zajedničkih adresnih i linija podataka (MAB i MDB)

Veličina celokupnog adresnog prostora je 1 MB

Von Neumann arhitektura

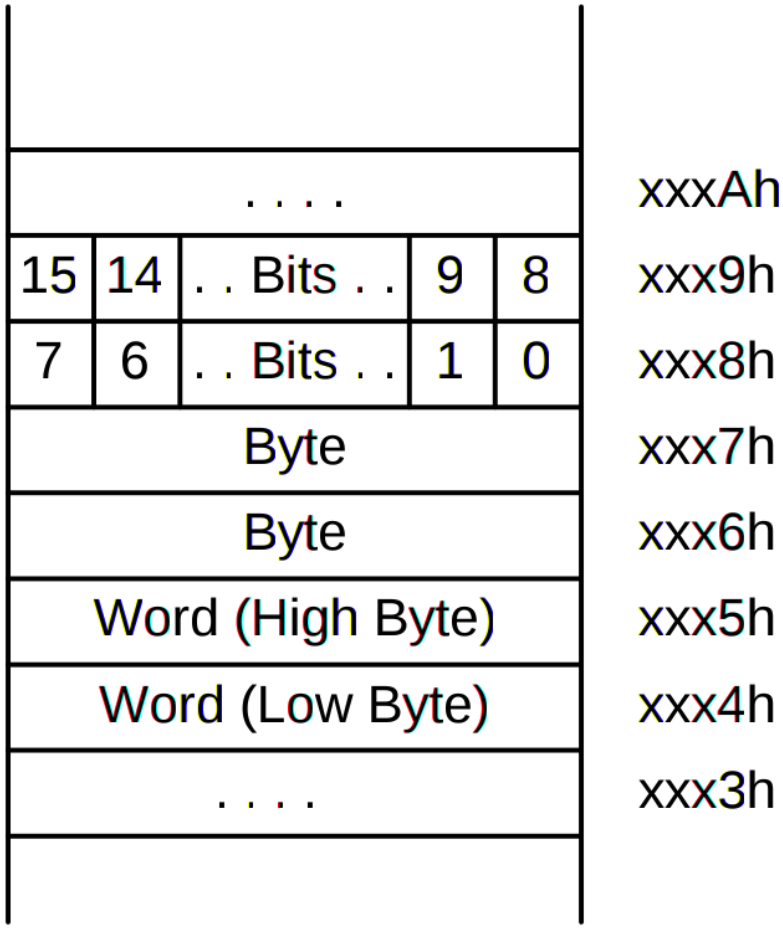
# Adresni prostor MSP430F5438A

| | | MSP430F5419A<br>MSP430F5418A | MSP430F5436A<br>MSP430F5435A | MSP430F5438A<br>MSP430F5437A |
|---|---|---|---|---|
| Memory (flash)<br>Main: interrupt vector<br>Main: code memory | Total Size<br>Flash<br>Flash | 128 KB<br>00FFFFh–00FF80h<br>025BFFh–005C00h | 192 KB<br>00FFFFh–00FF80h<br>035BFFh–005C00h | 256 KB<br>00FFFFh–00FF80h<br>045BFFh–005C00h |
| Main: code memory | Bank D | N/A | 23 KB<br>035BFFh–030000h | 64 KB<br>03FFFFh–030000h |
| | Bank C | 23 KB<br>025BFFh–020000h | 64 KB<br>02FFFFh–020000h | 64 KB<br>02FFFFh–020000h |
| | Bank B | 64 KB<br>01FFFFh–010000h | 64 KB<br>01FFFFh–010000h | 64 KB<br>01FFFFh–010000h |
| | Bank A | 41 KB<br>00FFFFh–005C00h | 41 KB<br>00FFFFh–005C00h | 64 KB<br>045BFFh–040000h<br>00FFFFh–005C00h |
| RAM | Size | 16 KB | 16 KB | 16 KB |
| | Sector 3 | 4 KB<br>005BFFh–004C00h | 4 KB<br>005BFFh–004C00h | 4 KB<br>005BFFh–004C00h |
| | Sector 2 | 4 KB<br>004BFFh–003C00h | 4 KB<br>004BFFh–003C00h | 4 KB<br>004BFFh–003C00h |
| | Sector 1 | 4 KB<br>003BFFh–002C00h | 4 KB<br>003BFFh–002C00h | 4 KB<br>003BFFh–002C00h |
| | Sector 0 | 4 KB<br>002BFFh–001C00h | 4 KB<br>002BFFh–001C00h | 4 KB<br>002BFFh–001C00h |
| Information memory (flash) | Info A | 128 B<br>0019FFh–001980h | 128 B<br>0019FFh–001980h | 128 B<br>0019FFh–001980h |
| | Info B | 128 B<br>00197Fh–001900h | 128 B<br>00197Fh–001900h | 128 B<br>00197Fh–001900h |
| | Info C | 128 B<br>0018FFh–001880h | 128 B<br>0018FFh–001880h | 128 B<br>0018FFh–001880h |
| | Info D | 128 B<br>00187Fh–001800h | 128 B<br>00187Fh–001800h | 128 B<br>00187Fh–001800h |
| Bootstrap loader (BSL) memory (Flash) | BSL 3 | 512 B<br>0017FFh–001600h | 512 B<br>0017FFh–001600h | 512 B<br>0017FFh–001600h |
| | BSL 2 | 512 B<br>0015FFh–001400h | 512 B<br>0015FFh–001400h | 512 B<br>0015FFh–001400h |
| | BSL 1 | 512 B<br>0013FFh–001200h | 512 B<br>0013FFh–001200h | 512 B<br>0013FFh–001200h |
| | BSL 0 | 512 B<br>0011FFh–001000h | 512 B<br>0011FFh–001000h | 512 B<br>0011FFh–001000h |
| Peripherals | Size | 4KB<br>000FFFh–000000h | 4KB<br>000FFFh–000000h | 4KB<br>000FFFh–000000h |

# Memorijska mapa periferija

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|---|---|---|
| Special Functions (see Table 13) | 0100h | 000h-01Fh |
| PMM (see Table 14) | 0120h | 000h-010h |
| Flash Control (see Table 15) | 0140h | 000h-00Fh |
| CRC16 (see Table 16) | 0150h | 000h-007h |
| RAM Control (see Table 17) | 0158h | 000h-001h |
| Watchdog (see Table 18) | 015Ch | 000h-001h |
| UCS (see Table 19) | 0160h | 000h-01Fh |
| SYS (see Table 20) | 0180h | 000h-01Fh |
| Shared Reference (see Table 21) | 01B0h | 000h-001h |
| Port P1, P2 (see Table 22) | 0200h | 000h-01Fh |
| Port P3, P4 (see Table 23) | 0220h | 000h-00Bh |
| Port P5, P6 (see Table 24) | 0240h | 000h-00Bh |
| Port P7, P8 (see Table 25) | 0260h | 000h-00Bh |
| Port P9, P10 (see Table 26) | 0280h | 000h-00Bh |
| Port P11 (see Table 27) | 02A0h | 000h-00Ah |
| Port PJ (see Table 28) | 0320h | 000h-01Fh |
| TA0 (see Table 29) | 0340h | 000h-02Eh |
| TA1 (see Table 30) | 0380h | 000h-02Eh |
| TB0 (see Table 31) | 03C0h | 000h-02Eh |
| Real Timer Clock (RTC_A) (see Table 32) | 04A0h | 000h-01Bh |
| 32-Bit Hardware Multiplier (see Table 33) | 04C0h | 000h-02Fh |
| DMA General Control (see Table 34) | 0500h | 000h-00Fh |
| DMA Channel 0 (see Table 34) | 0510h | 000h-00Ah |
| DMA Channel 1 (see Table 34) | 0520h | 000h-00Ah |
| DMA Channel 2 (see Table 34) | 0530h | 000h-00Ah |
| USCI_A0 (see Table 35) | 05C0h | 000h-01Fh |
| USCI_B0 (see Table 36) | 05E0h | 000h-01Fh |
| USCI_A1 (see Table 37) | 0600h | 000h-01Fh |
| USCI_B1 (see Table 38) | 0620h | 000h-01Fh |
| USCI_A2 (see Table 39) | 0640h | 000h-01Fh |
| USCI_B2 (see Table 40) | 0660h | 000h-01Fh |
| USCI_A3 (see Table 41) | 0680h | 000h-01Fh |
| USCI_B3 (see Table 42) | 06A0h | 000h-01Fh |
| ADC12_A (see Table 43) | 0700h | 000h-03Eh |

# Organizacija RAM memorije



# MSP430X CPU

## Osnovne karakteristike

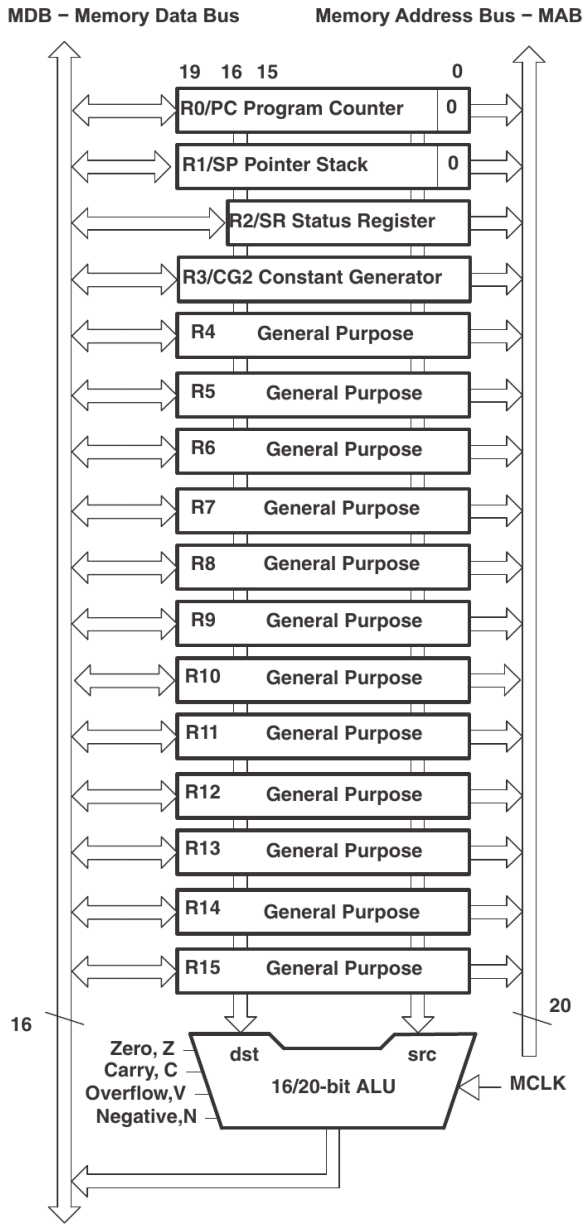
- RISC arhitektura sa 27 instrukcija i sedam načina adresiranja (Ortogonalna arhitektura)
- 20-bitna adresna magistrala i 16-bitna magistrala podataka
- Registar fajl sa 16 20-bitnih registara direktno povezanih na ALU
- Izvršavanje instrukcija koje se obraćaju registrima u jednom ciklusu
- Sve instrukcije mogu da adresiraju kako reči tako i bajtove
- Direktan transfer podataka iz jednog u drugi deo memorije bez upotrebe registara

# MSP430X Načini adresiranja

| As, Ad | Addressing Mode | Syntax | Description |
|---|---|---|---|
| 00, 0 | Register | Rn | Register contents are operand. |
| 01, 1 | Indexed | X(Rn) | (Rn + X) points to the operand. X is stored in the next word, or stored in combination of the preceding extension word and the next word. |
| 01, 1 | Symbolic | ADDR | (PC + X) points to the operand. X is stored in the next word, or stored in combination of the preceding extension word and the next word. Indexed mode X(PC) is used. |
| 01, 1 | Absolute | &ADDR | The word following the instruction contains the absolute address. X is stored in the next word, or stored in combination of the preceding extension word and the next word. Indexed mode X(SR) is used. |
| 10, – | Indirect Register | @Rn | Rn is used as a pointer to the operand. |
| 11, – | Indirect Autoincrement | @Rn+ | Rn is used as a pointer to the operand. Rn is incremented afterwards by 1 for .B instructions, by 2 for .W instructions, and by 4 for .A instructions. |
| 11, – | Immediate | #N | N is stored in the next word, or stored in combination of the preceding extension word and the next word. Indirect autoincrement mode @PC+ is used. |

## CPU

- `PC` - programski brojač
- `SP` - pokazivač steka
- `SR` - statusni registar
- `CG1/CG2` - generator konstanti
- `Rn` - registri opšte namene



# PC (R0) - programski brojač

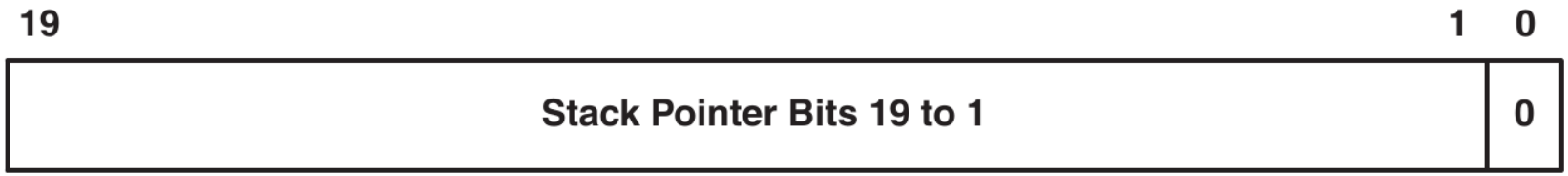
- 20-bitni registar mapiran u registar fajlu
- Može mu se pristupati direktno kao i svakom drugom od 15 registara
- Najniži bit je uvek nula jer se sve instrukcije sastoje od 2, 4, 6 ili 8 bajtova

# Primer pristupanja PC-u

```
MOV.W   #LABEL,PC   ; Branch to address LABEL (lower 64KB)

MOVA    #LABEL,PC   ; Branch to address LABEL (1MB memory)

MOV.W   LABEL,PC    ; Branch to address in word LABEL
                    ; (lower 64KB)

MOV.W   @R14,PC     ; Branch indirect to address in
                    ; R14 (lower 64KB)

ADDA    #4,PC       ; Skip two words (1MB memory)
```

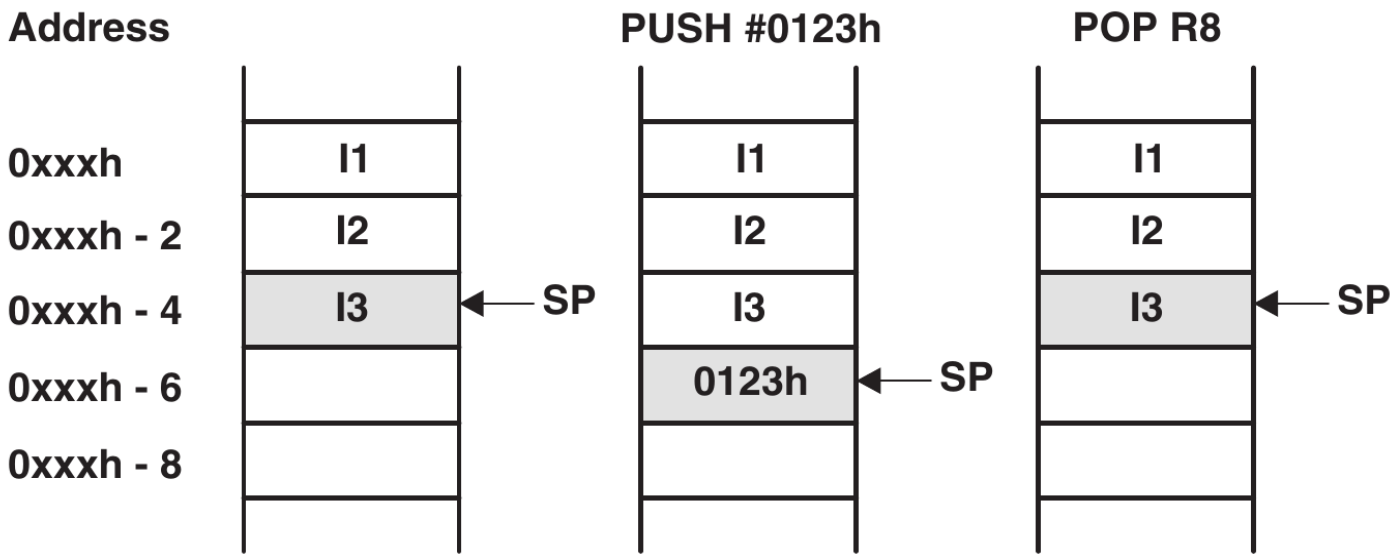
# SP (R1) - pokazivač steka

- Kao i svi registri u registar fajlu direktno je dostupan svim instrukcijama
- Kao i programski brojač ukazuje samo na parne adrese (najniži bit je uvek nula)
- Ukazuje na poslednju zauzetu lokaciju
- Stek raste od viših prema nižim lokacijama



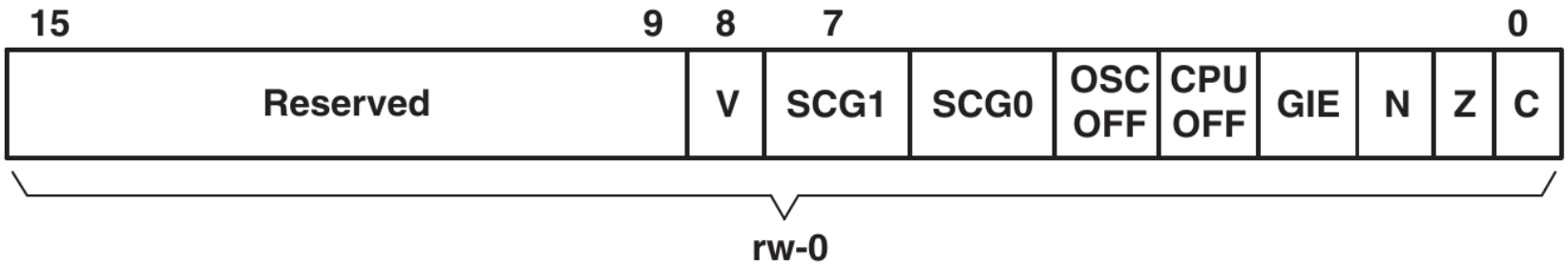
# Primer upotrebe SP-a

```
MOV.W    2(SP),R6        ; Copy Item I2 to R6
MOV.W    R7,0(SP)        ; Overwrite TOS with R7
PUSH     #0123h          ; Put 0123h on stack
POP      R8              ; R8 = 0123h
```



# SR (R2) - statusni registar

- Jedini 16-bitni registar
- Sadrži sledeće flegove čije se stanje ažurira kao posledica izvršavanja određenih instrukcija:
  - `N` - rezultat je negativan broj
  - `Z` - rezultat je 0
  - `C` - rezultat je različit od 0
  - `V` - došlo je do *overflow*-a
- Mapirani flegovi za
  - globalna dozvola maskirajućih prekida - `GIE`
  - low-power modove rada - `SCG1`, `SCG0`, `OSCOFF`, `CPUOFF`



# CG1/CG2 - generator konstanti

Šest često korišćenih konstanti se generišu pomoguću generatora konstanti - registara `R2` (`CG1`) i `R3` (`CG2`)

Ne koriste se posebne instrukcije

Ne postoji dodatna kodna reč za konstante

Nema dodatnog pristupa memoriji za dohvatanje konstante

Asembler automatski koristi generator konstanti ako je neka od šest kostanti neposredni izvorni (*source*) operand

Podržane konstante: 0, $\pm 1$, $+2$, $+4$, $+8$

# R4-R15 registri opšte namene

Ovim registrima se može pristupati na sve načine i mogu se koristiti u svim modovima adresiranja

Svaki registar može da sadrži podatak, adresu podatka u memoriji, ili indeks pri indirektnom adresiranju

Svakom registru se može pristupati kao 8-bitnom, 16-bitnom ili 20-bitnom podatku

# Set instrukcija

Instrukcijski set obuhvata 27 osnovnih i 24 emulirane instrukcije

Instrukcije mogu imati jedan ili dva operanda, a mogu biti i bez operanada

Razlikuju se varijante instrukcija koje mogu da se koriste samo na najnižih 64kB memorijskog prostora (`MSP430` varijanta) i koje mogu da se koriste na celih 1MB memorijskog prostora (`MSP430X` varijanta)

# Unified Clock System 1/2

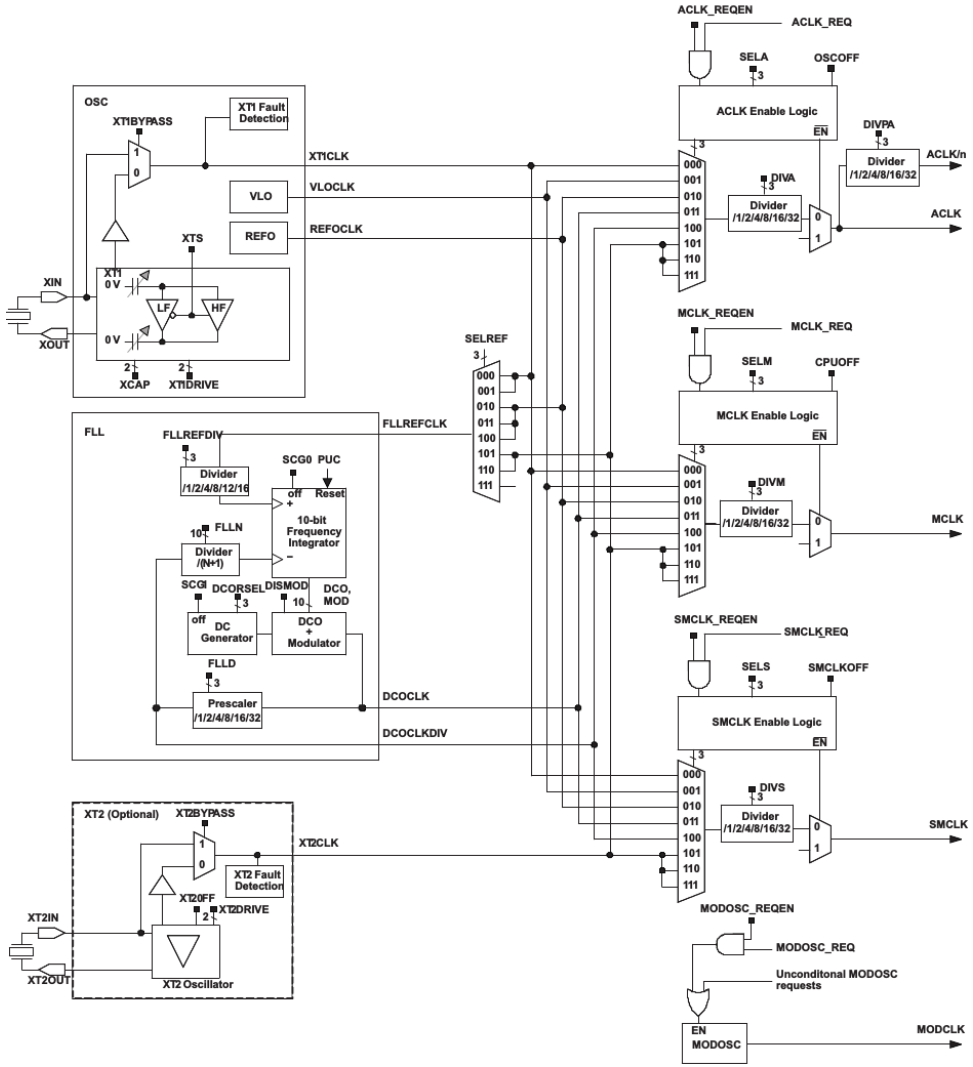
## Unutar mikrokontrolera na raspolaganju su 3 taktna signala

- `MCLK` - takt za procesor
- `SMCLK` - takt za periferije
- `ACLK` - pomoćni takt za periferije

## Izvorni na osnovu kojih se generišu taktni signali

- `XT1CLK` oscilator koji može da radi sa sporim i brzim kristalom, sa integrisanim promenljivim kondenzatorima
- `VLOCLK` - interni oscilator male potrošnje i tipične učestanosti 10 kHz
- `REFOCLK` - interni trimovan oscilator tipične učestanosti 32768 Hz
- `DCOCLK` - interni digitalno kontrolisani oscilator koji može da se stabilizuje pomoću FLL (Frequency Locked Loop)
- `XT2CLK` - opcioni dodatni oscilator visoke učestanosti

# Unified Clock System 2/2



# Sistemski reset i inicijalizacija 1/3

## BOR – brownout reset

- pri dovođenju napajanja
- niska vrednost signala na $\overline{\texttt{RST}}$/NMI pinu
- wakeup događaj u LPMx.5 modu
- softverski BOR događaj

## POR – power-on reset

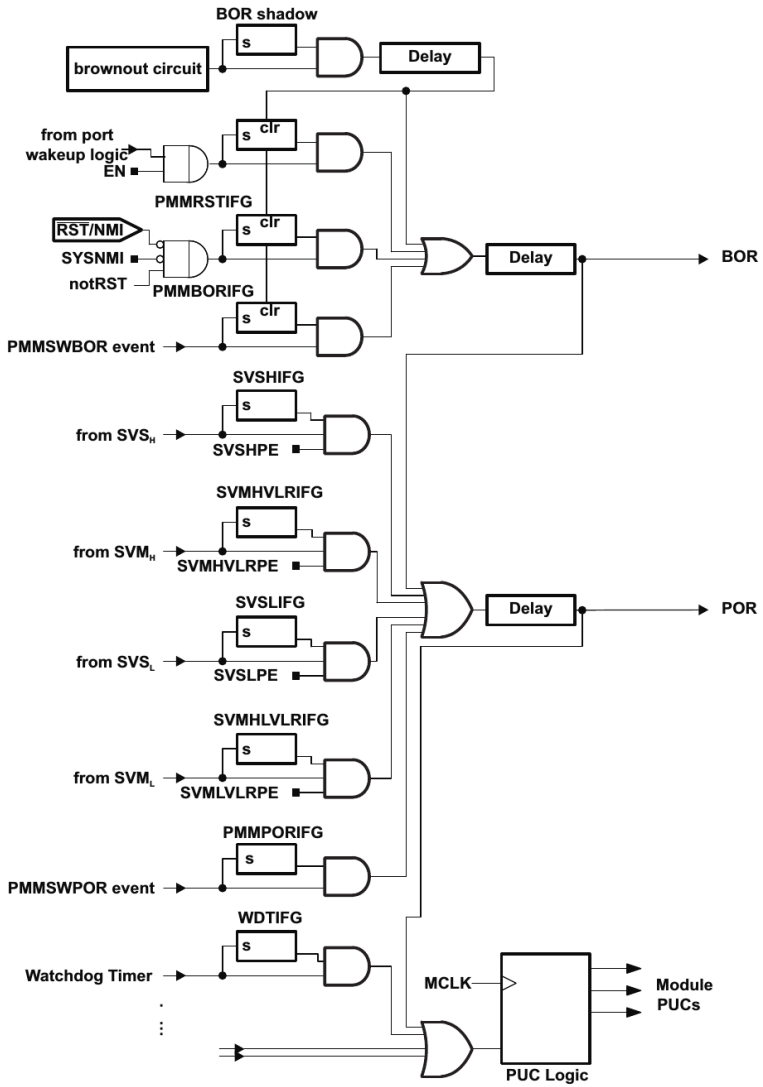
- pri pojavi BOR signala
- pri signalu od internog supervizora napajanja
- softverski POR događaj

# Sistemski reset i inicijalizacija 2/3

## PUC – power-up clear

- pri pojavi POR signala
- po isteku vremena watchdog tajmera
- pri nedozvoljenom pristupu watchdog tajmeru
- pri nedozvoljenom pristupu flash memoriji
- pri nedozvoljenom pristupu Power Management modulu

# Sistemski reset i inicijalizacija 3/3



# Inicijalna stanja po reset-u (BOR)

Svi I/O pinovi su konfigurisani kao ulazni

Ostale periferije i registri su inicijalizovani kao što je navedeno u User's Guide-u

Statusni registar (`SR`) je resetovan

Watchdog tajmer je u aktivan i radi u watchdog modu

U programski brojač `PC` učitava se adresa sadržana u reset vektoru na adresi `0xFFFE`

# Neophodna inicijalizacija softvera

Inicijalizovati pokazivač steka (`SP`)

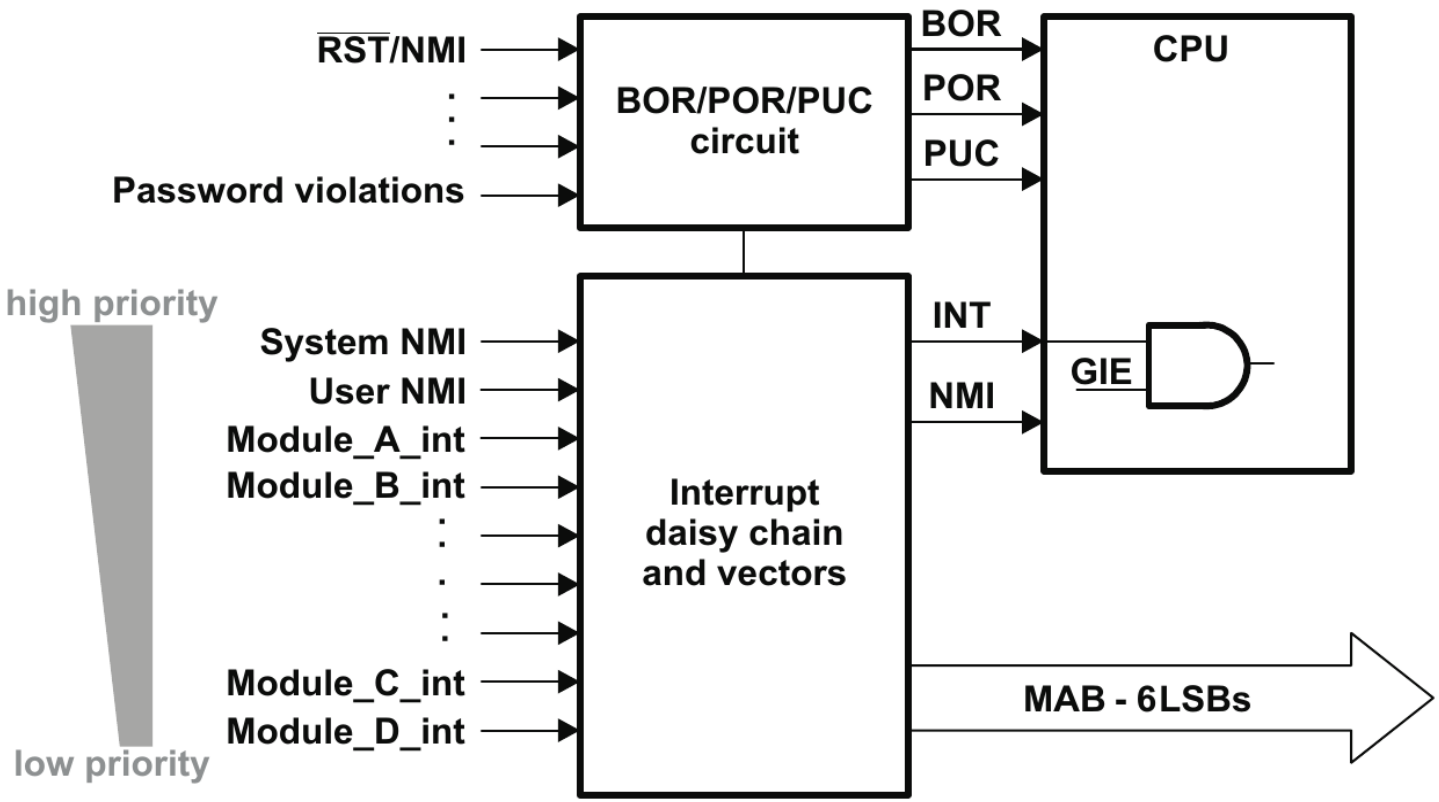
Inicijalizovati watchdog tajmer prema zahtevima korisničke aplikacije

Konfigurisati periferije (i portove) prema zahtevima korisničke aplikacije

# Prekidi

Pored sistemskog reseta postoje još dve vrste prekida

- NMI prekid (*(non)maskable interrupt*)
- Maskirajući prekidi (*maskable interrupts*)



# NMI prekid 1/3

## Sistemski NMI

- Modul za upravljanje potrošnjom (PMM)
- Pristup nepostojećoj memoriji
- JTAG mailbox događaj

## Korisnički NMI

- Ivica na $\overline{\texttt{RST}}$/NMI pinu kada je konfigurisan u NMI modu
- Greška oscilatora
- Signal greške u pristupu flash memoriji (pristup u toku izvršavanja ranije iniciranog brisanja ili upisa)

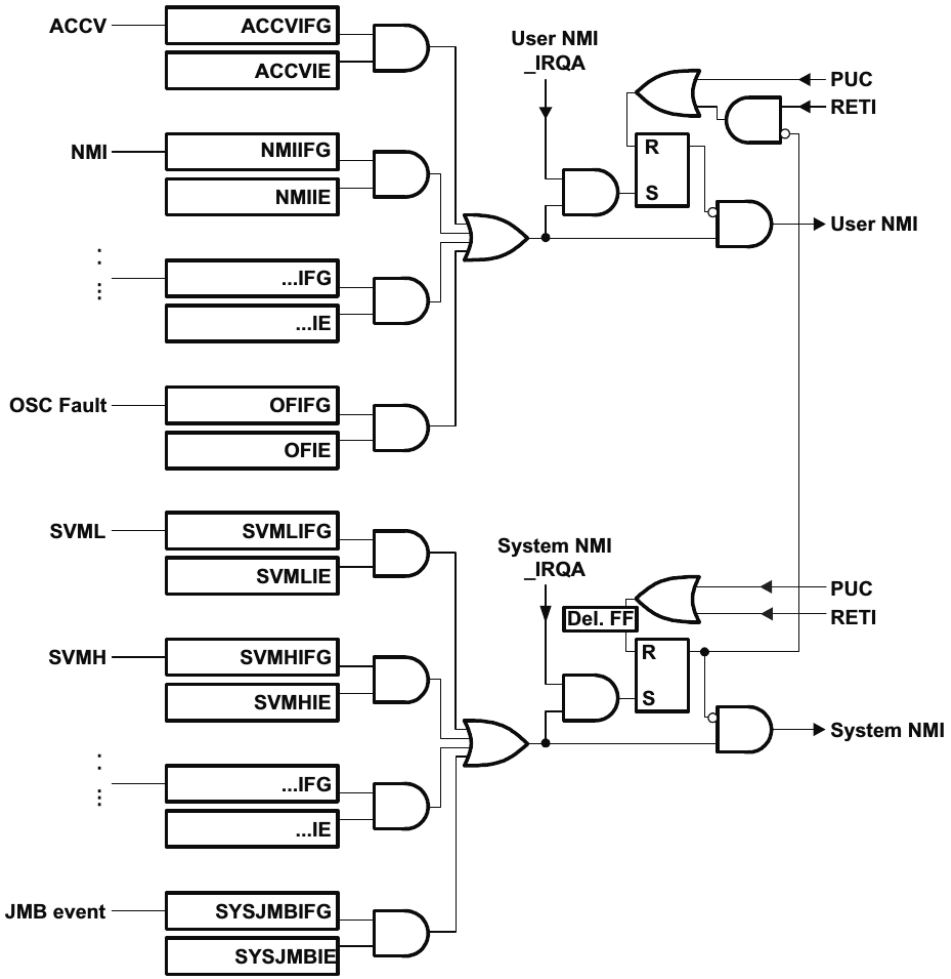
# NMI prekid 2/3

NMI prekid je uslovno nemaskirajući jer se ne maskira `GIE` bitom u `SR`, ali se svaki od izvora prekida može maskirati

Prekidni vektor za sistemski NMI je na adresi `0xFFFC` a za korisnički na `0xFFFA`

Unutar prekidne rutine se poliranjem odgovarajućih flegova može utvrditi koji od događaja je izazvao prekid

# NMI prekid 3/3



# Maskirajući prekidi

Postoji do 61 različiti maskirajući prekid koji se u zavisnosti od konkretnog mikrokontrolera dodeljuje različitim periferijama

- `MSP430F5438A` podržava 20 maskirajućih prekida

Prekidi se prioritiraju

Globalno maskiranje prekida se vrši pomoću bita `GIE` u `SR`

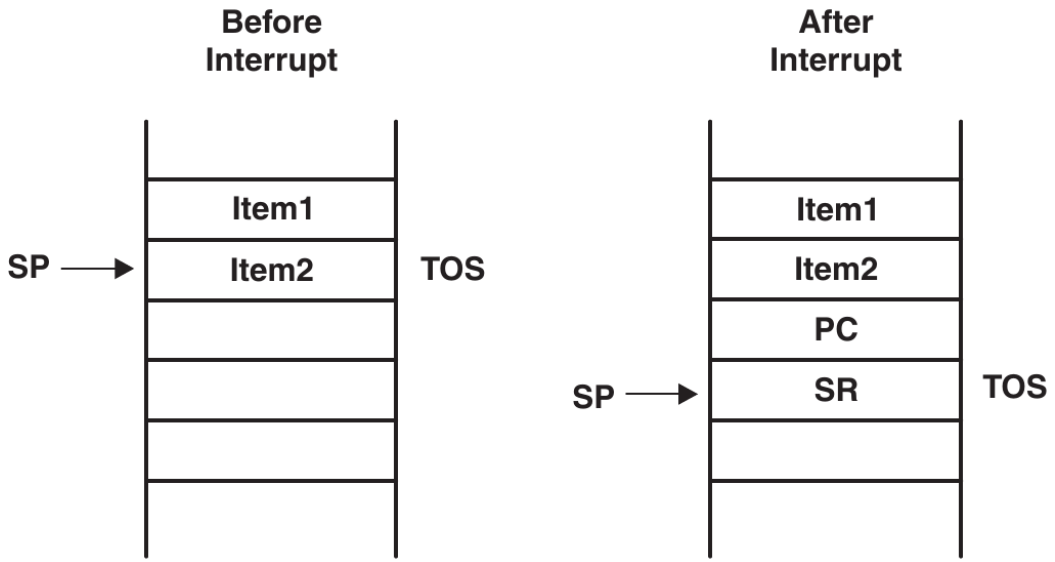
Svaki pojedinačni izvor maskirajućeg prekida je moguće dodatno maskirati odgovarajućim bitom u registru periferije

Više izvora prekida koji su povezani na isti ulaz u tabeli prekida povezani su u *daisy-chain*

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| **System Reset**<br>Power-Up<br>External Reset<br>Watchdog Time-out, Password Violation<br>Flash Memory Password Violation<br>PMM Password Violation | WDTIFG, KEYV (SYSRSTIV)(1) (2) | Reset | 0FFFEh | 63, highest |
| **System NMI**<br>PMM<br>Vacant Memory Access<br>JTAG Mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1) | (Non)maskable | 0FFFCh | 62 |
| **User NMI**<br>NMI<br>Oscillator Fault<br>Flash Memory Access Violation | NMIIFG, OFIFG, ACCVIFG (SYSUNIV)(1) (2) | (Non)maskable | 0FFFAh | 61 |
| TB0 | TBCCR0 CCIFG0 (3) | Maskable | 0FFF8h | 60 |
| TB0 | TBCCR1 CCIFG1 to TBCCR6 CCIFG6, TBIFG (TBIV)(1) (3) | Maskable | 0FFF6h | 59 |
| Watchdog Timer_A Interval Timer Mode | WDTIFG | Maskable | 0FFF4h | 58 |
| USCI_A0 Receive and Transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV)(1) (3) | Maskable | 0FFF2h | 57 |
| USCI_B0 Receive and Transmit | UCB0RXIFG, UCB0TXIFG (UCB0IV)(1) (3) | Maskable | 0FFF0h | 56 |
| ADC12_A | ADC12IFG0 to ADC12IFG15 (ADC12IV)(1) (3) | Maskable | 0FFEEh | 55 |
| TA0 | TA0CCR0 CCIFG0(3) | Maskable | 0FFECh | 54 |
| TA0 | TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1) (3) | Maskable | 0FFEAh | 53 |
| USCI_A2 Receive and Transmit | UCA2RXIFG, UCA2TXIFG (UCA2IV)(1) (3) | Maskable | 0FFE8h | 52 |
| USCI_B2 Receive and Transmit | UCB2RXIFG, UCB2TXIFG (UCB2IV)(1) (3) | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1) (3) | Maskable | 0FFE4h | 50 |
| TA1 | TA1CCR0 CCIFG0(3) | Maskable | 0FFE2h | 49 |
| TA1 | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1) (3) | Maskable | 0FFE0h | 48 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV)(1) (3) | Maskable | 0FFDEh | 47 |
| USCI_A1 Receive and Transmit | UCA1RXIFG, UCA1TXIFG (UCA1IV)(1) (3) | Maskable | 0FFDCh | 46 |
| USCI_B1 Receive and Transmit | UCB1RXIFG, UCB1TXIFG (UCB1IV)(1) (3) | Maskable | 0FFDAh | 45 |
| USCI_A3 Receive and Transmit | UCA3RXIFG, UCA3TXIFG (UCA3IV)(1) (3) | Maskable | 0FFD8h | 44 |
| USCI_B3 Receive and Transmit | UCB3RXIFG, UCB3TXIFG (UCB3IV)(1) (3) | Maskable | 0FFD6h | 43 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV)(1) (3) | Maskable | 0FFD4h | 42 |
| RTC_A | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1) (3) | Maskable | 0FFD2h | 41 |
| Reserved | Reserved(4) | | 0FFD0h | 40 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

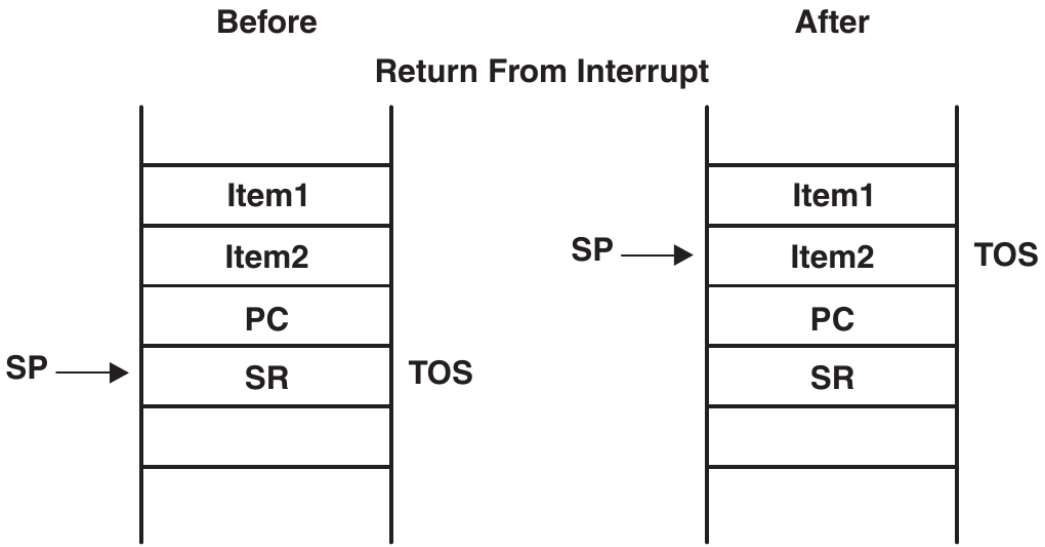
# Prihvatanje zahteva za prekid

- Završava se izvršavanje trenutne instrukcije
- `PC` i `SR` se prebacuju na stek
- Zabranjuju se svi maskirajući prekidi
- U `SR` se pored aritmetičkih brišu i flegovi koji označavaju *low-power* modove tako da se prekid uvek izvršava u aktivnom modu
- U `PC` se učitava vrednost iz tabele prekida (`IVT`)

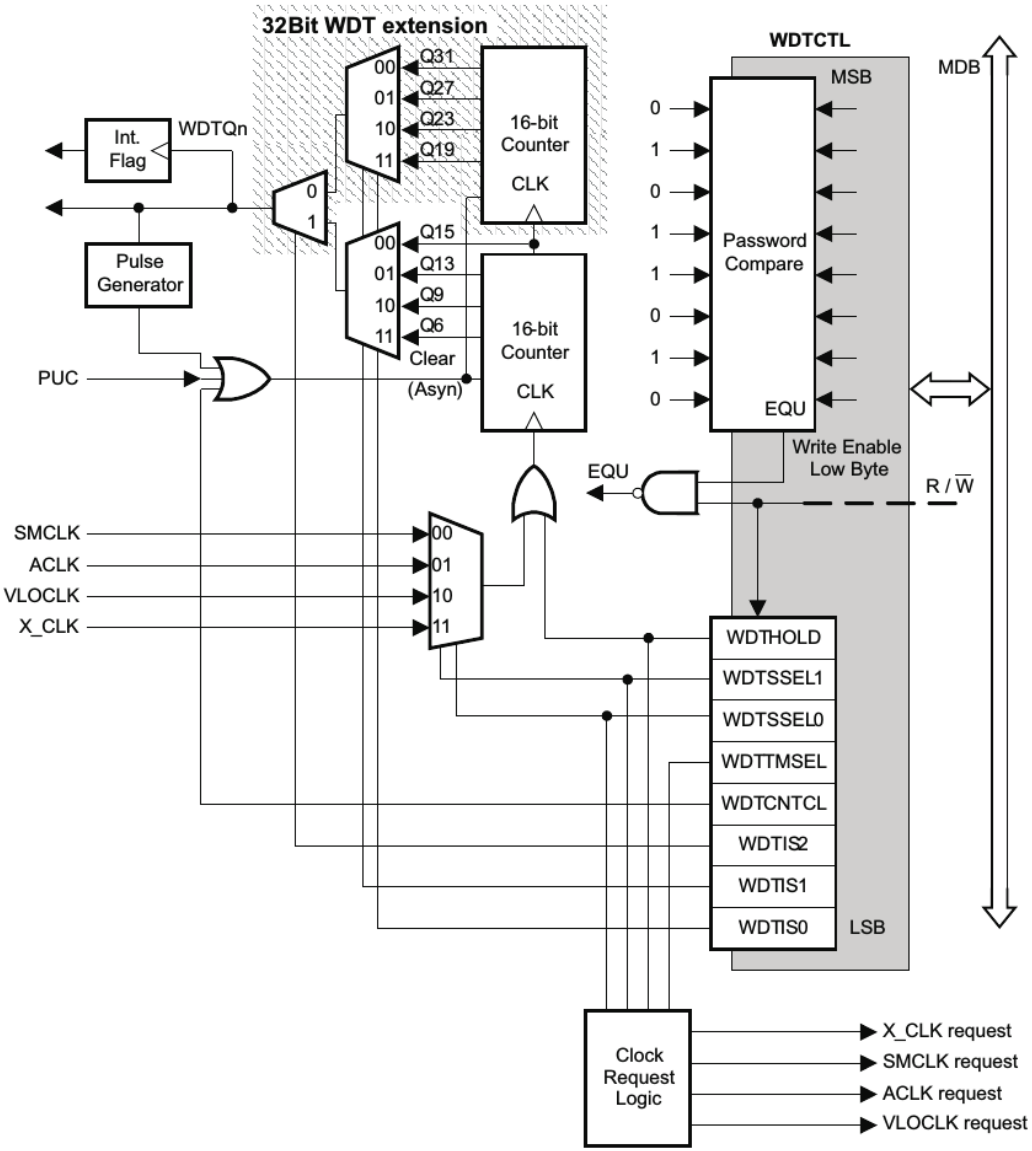


# Povratak iz prekidne rutine

- Povratak se izvršava instrukcijom `RETI`
- Sa steka se restauriraju `PC` i `SR` tako da se izvršenje programa nastavlja gde je prekinuto
- Sistem se automatski vraća u režim rada pre prihvatanja zahteva za prekid, jer se flegovi koji to određuju nalaze u `SR`



# WDT - Watchdog Timer 1/2



# WDT - Watchdog Timer 2/2

Može da se koristi kao klasičan WDT ili kao tajmer koji generiše periodične prekide

U slučaju da se koristi u WDT modu izaziva PUC prekid

U slučaju da se koristi u "interval" modu izaziva poseban maskirajući prekid

WDT se kontroliše preko jednog 16-bitnog registra (`WDTCTL`)

`WDTCTL` registru se pristupa kao celoj reči u jednoj instrukciji. Svaki upis u `WDTCTL` registar mora imati viši bajt `0x5A`, inače se u protivnom izaziva NMI prekid. Svako čitanje `WDTCTL` kao rezultat ima viši bajt `0x69`

Kraj prvog dela...