ЕЛЕКТРИЈАДА 2017

ELECTRONICS II - Test questions

(correct answer +5, incorrect answer -2, no answer (N) 0)

1. There is a tri-state buffer where internal delays can be ignored. Right after z state is set, the output voltage level will be:

A. VDD/2 where VDD is supply voltage
B. High or low, depending on the state before z state is set
C. Indefinite
D. High
E. Low

2. In CMOS ICs, PMOS transistor is usually configured as:

A. No potential is given to substrate
B. Substrate is connected to source
C. Substrate is connected to drain
D. The highest potential is given to substrate
E. The lowest potential is given to substrate

3. There is an inverter which has a passive capacitive load. If supply voltage increases,

A. Rise will increase, fall will decrease
B. Fall will increase, rise will decrease
C. Output transition time will decrease
D. Output transition time will increase, as during switching the load must be charged by larger ΔU voltage
E. Output transition time will remain the same, as ΔU will increase, but charging current will also increase

4. In order to prevent latch-up in CMOS circuits it is necessary to:

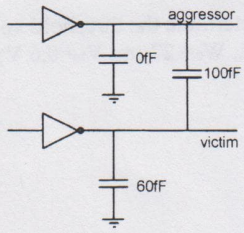
A. Increase the parasitic capacitances between the buses of output buffer's parasitic bipolar transistors
B. Increase the gain of parasitic bipolar transistors
C. Put the drains of n and p transistors as close as possible
D. Put n+ guard ring around n+ source/drain
E. Put p+ guard ring around n+ source/drain and put n+ guard ring around p+ source/drain

5. Assuming kn=2kp, in what case the output transition time of two input NOR cell will be approximately equal?

A. Wp=Wn
B. Wp=2Wn
C. Wp=4Wn
D. Wp=6Wn
E. Wp=8Wn

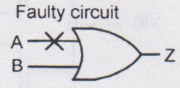
6. For the shown circuit, define victim line effective capacitance for delay calculation in case of aggressor line switching in opposite direction.

A. 160fF
B. 210fF
C. 260fF
D. 110fF
E. 150fF



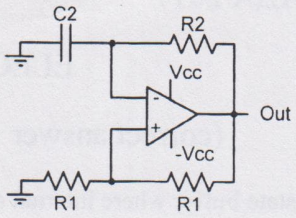
7. Find the set of all input patterns for detection of the stuck-at-0 fault on the input line A of the logical gate Z = A or B depicted below:

A. {(0, 0)}
B. {(1, 0)}
C. {(1,0), (0, 1)}
D. {(0, 0), (0, 1), (1,0)}
E. The correct answer is missing



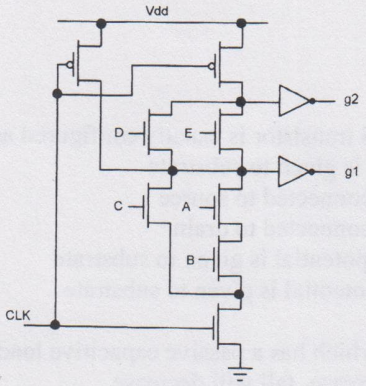
8. The change of which element of this generator will lead to the change of frequency of output signal?

A. only: R1 and Vcc
B. only: R2
C. only: C2
D. only: R2 and C2
E. R1, R2, C2 and Vcc



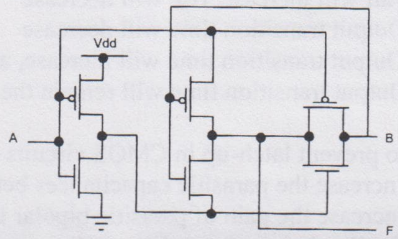
9. What logic function does the circuit implement?

A. g1=(A+B)C, g2=(A+B)C+ED
B. g1=AB+C, g2=(AB+C)(E+D)
C. g1=AB+C, g2=(AB+C)ED
D. g1=AB⊕C, g2=(AB⊕C)ED
E. g1=AB+C, g2=(AB+C) (E⊕D)



10. What is the logic function performed by this circuit?

A. F=A+B
B. F=A&B
C. F=!A+!B
D. F=A⊕B
E. F=A⊕!B



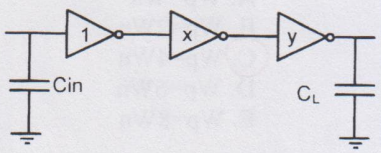
ELECTRONICS II - Problems

1. The first inverter of the presented buffer is of minimal size, input capacitance is C_{in}=10 fF, delay 70 ps. The load capacitance of the buffer is C_L=20 pf.

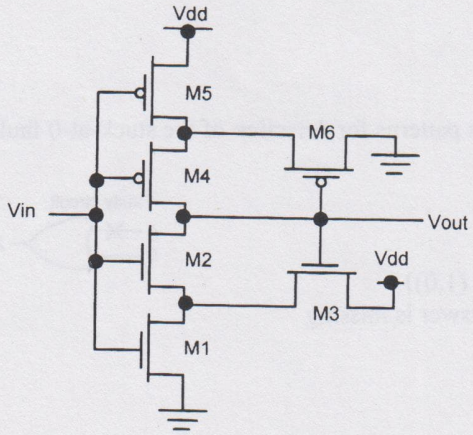
a) (10) Define the sizes of the other two inverters with respect to the minimal one. Use the condition to get minimum delay, consider that input capacitances are proportional to sizes. Define the total delay.

b) (10) Add any number of inverters to get minimum delay. Define the total delay.

c) (5) Define the power consumption of the circuit if the supply voltage is 2.5V, operating frequency 200 MHz.



2. (25) Determine the threshold voltages of the Schmitt trigger given in the figure if W_1=9μm, W_2=18μm, W_3= 7μm, W_4=54μm, W_5=27μm, W_6= 22μm; V_{tn}=0,6 V; V_{tp}=-0,7 V; Ln=0,4 μm; Lp=0,4μm, VDD=3,3 V.



ЕЛЕКТРИЈАДА 2017

SOLUTIONS

ELECTRONICS II - Test questions

(correct answer +5, incorrect answer -2, no answer (N) 0)

1. There is a tri-state buffer where internal delays can be ignored. Right after z state is set, the output voltage level will be:

B. High or low, depending on the state before z state is set

2. In CMOS ICs, PMOS transistor is usually configured as:

D. The highest potential is given to substrate

3. There is an inverter which has a passive capacitive load. If supply voltage increases,

C. Output transition time will decrease

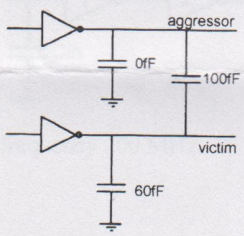
4. In order to prevent latch-up in CMOS circuits it is necessary to:

C. Put the drains of n and p transistors as close as possible

5. Assuming kn=2kp, in what case the output transition time of two input NOR cell will be approximately equal?

C. Wp=4Wn

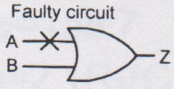
6. For the shown circuit, define victimline effective capacitance for delay calculation in case of aggressor line switching in opposite direction.



C. 260fF

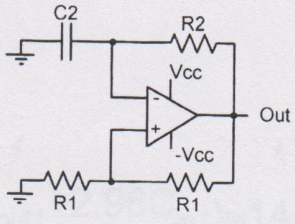
7. Find the set of all input patterns for detection of the stuck-at-0 fault on the input line A of the logical gate Z = A or B depicted below:

B. {(1, 0)}



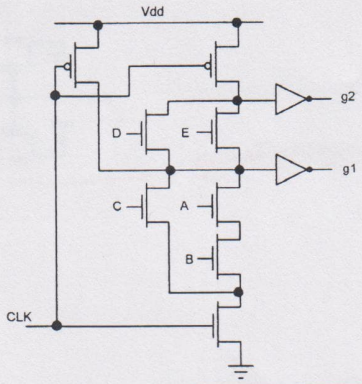
8. The change of which element of this generator will lead to the change of frequency of output signal?

D. only: R2 and C2



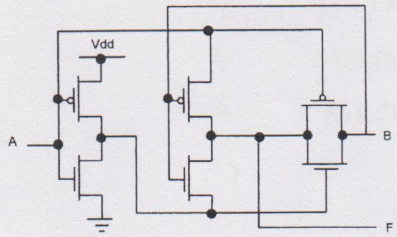
9. What logic function does the circuit implement?

B. g1=AB+C, g2=(AB+C)(E+D)



10. What is the logic function performed by this circuit?

D. F=A⊕B



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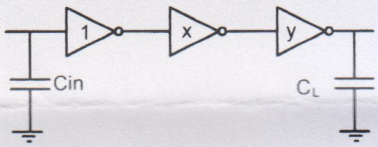


a) (10) Define the sizes of the other two inverters with respect to the minimal one. Use the condition to get minimum delay, consider that input capacitances are proportional to sizes.

b) (10) Add any number of inverters to get minimum delay. Define the total delay.

c) (5) Define the power consumption of the circuit if the supply voltage is 2.5V, operating frequency 200 MHz.

a. $A = (C_L/C_{in1})^{1/N}$

$A=(20\cdot10^3/10)^{1/3}=12.6$ ... 4

$(W/L)_1=1, (W/L)_2=12.6, (W/L)_2=158.7$ 2 = 1+1

$t_d=0.7N(R_{n1}+R_{p1})(C_{out1}+AC_{in1})=2.1R_1(C_{out1}+12.6C_{in1})\approx26.5R_1C_{in1}$ 4

2 2,65 ns

100ps

b. $N=\ln(C_L/C_{in1})=\ln(20\cdot10^3/10)=7.6$ 3

$N=7$ 3

$A=(20\cdot10^3/10)^{1/7}=2.96$ 2

$(W/L)_1=1, (W/L)_2=A^2,\ldots, (W/L)_7=A^7$ 1

1,45ns

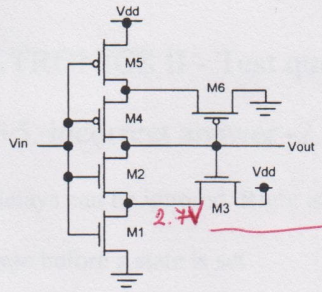
$t_d=0.7N(R_{n1}+R_{p1})(C_{out1}+AC_{in1})=4.9R_1(C_{out1}+2.96C_{in1})\approx14.5R_1C_{in1}$ 1

100ps

c. $P=V_{DD}^2F\ C_{in1}\Sigma(A+A^2+..+A^7)$ = 37,56 mW 5

3pos

2. (25) Determine the threshold voltages of the Schmitt trigger given in the figure if W_1=9μm, W_2=18μm, W_3= 7μm, W_4=54μm, W_5=27μm, W_6= 22μm; V_{tn}=0,6 V; V_{tp}=-0,7 V; Ln=0,4 μm; Lp=0,4μm, VDD=3,3 V.



→ у тренутку проводења

For V_{SPH}:

When Vin low and $V_{in} > V_{tn}$, $V_{out}=V_{oh}$, M3 is ON and saturated. (убеди) 4 M1/M5

M2 is OFF and there is not positive feedback. 4 M3/M6

Feedback starts when M2 is change state to ON, i.e. $V_{in}-V_{dM1}=V_{tn}$. 4 M2/M4

In this situations M1 is saturated: $V_{dsM1} = V_{gsM1}-V_{tn}=V_{in}-V_{tn}$

$$I_{D3} = \frac{k_3}{2}(V_{DD} - V_{dM1} - V_{tn})^2 = I_{D1} = \frac{k_1}{2}(V_{in} - V_{tn})^2$$

$$V_{dM1} = V_{in} - V_{tn}$$

$$(V_{DD} - V_{in})^2 = \frac{k_1}{k_3}(V_{in} - V_{tn})^2$$

.....

Symmetric situations is for V_{SPL}

$$V_{SPH} = \frac{VDD + \sqrt{\frac{W_1 L_3}{W_3 L_1}}V_{tn}}{1 + \sqrt{\frac{W_1 L_3}{W_3 L_1}}} = \frac{3{,}3 + \sqrt{\frac{9}{7}}0{,}6}{1 + \sqrt{\frac{9}{7}}} = 1{,}865\ V$$

10

$$V_{SPL} = \frac{(VDD - V_{tp})\sqrt{\frac{W_5 L_6}{W_6 L_5}}}{1 + \sqrt{\frac{W_5 L_6}{W_6 L_5}}} = \frac{(3{,}3 - 0{,}7)\sqrt{\frac{27}{22}}}{1 + \sqrt{\frac{27}{22}}} = 1{,}366\ V$$

* провера засићења и тријодне области, покаша се 3 граница